

XX1000-BD Rev. V5

Features

- Excellent Broadband Mixer Driver
- Single Ended Fed Doubler with Distributed Buffer
 Amplifier
- Excellent LO Driver for MACOM Receivers
- +15 dBm Output Drive
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant

Applications

- Point-to-Point Radio
- Microwave
- LMDS
- SATCOM
- VSAT

Description

This single ended fed (no external balun required) 7.5 - 25.0 / 15.0 - 50.0 GHz GaAs MMIC doubler has a 15 dBm output drive and is an excellent LO doubler that can be used to drive fundamental mixer devices. It is also well suited to drive MACOMs' XR1002 receiver device.

This MMIC uses a GaAs pHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process.

Pad Configuration¹

Functional Block Diagram

Pad	Function	Description
1	RF_{IN}	RF Input
2	V _D 1	Drain Voltage Stage 1
3	V _D 2	Drain Voltage Stage 2
4	RF _{OUT}	RF Output
5	V _G 2	Gate Voltage Stage 2
6	V _{SS}	Source Supply Voltage
7	V _G 1	Gate Voltage Stage 1

1. Backside metal is RF, DC and thermal ground.

Ordering Information

Part Number	Package	
XX1000-BD-000V	vacuum release gel paks	
XX1000-BD-EV1	evaluation board	

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Parameter	Units	Min.	Тур.	Max
Output Frequency Range	GHz	15	_	50
Input Return Loss	dB	_	12	_
Output Return Loss	dB	_	12	_
Harmonic Gain	dB	_	13	_
Fundamental Rejection	dBc		20	_
Saturated Output Power	dBm	_	15	_
RF Input Power	dBm	-10	_	+10
Output Power @ 0 dBm P _{IN}	dBm	_	13	_
Drain Bias Voltage (V _D 1,2)	VDC	_	5.0	5.5
Gate Bias Voltage (V _G 1)	VDC	-1.2	-0.6	+0.1
Gate Bias Voltage (V _G 2)	VDC	-1.2	0.0	+0.1
Quiescent Drain Current (I_D 1,2) (V_D = 5 V, V_G 1 = -0.6 V, V_G = 0 V Typical) ²	mA	_	210	_
Source Voltage (V _{SS})	VDC	-5.5	-5.0	-2.0
Source Current (I _{ss})	mA	25	50	60

2. Adjust V_G1 to set 70 mA $I_{DQ}1$, adjust V_G2 to set 140 mA $I_{DQ}2$.

Absolute Maximum Ratings³

Parameter	Absolute Maximum	
Drain Voltage (V _D 1, V _D 2)	+6 V	
Source Voltage (V _{SS})	-6 V	
Drain Current ($I_D 1 + I_D 2$)	320 mA	
Source Current (I _{SS})	60 mA	
Gate Bias Voltage (V_G1)	+0.3 V	
Gate Bias Voltage (V _G 2)	+0.1 V	
RF Input Power	+12 dBm	
Storage Temperature	-65°C to +165°C	
Operating Temperature	-55°C to MTTF Table	
Channel Temperature	MTTF Table	

3. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

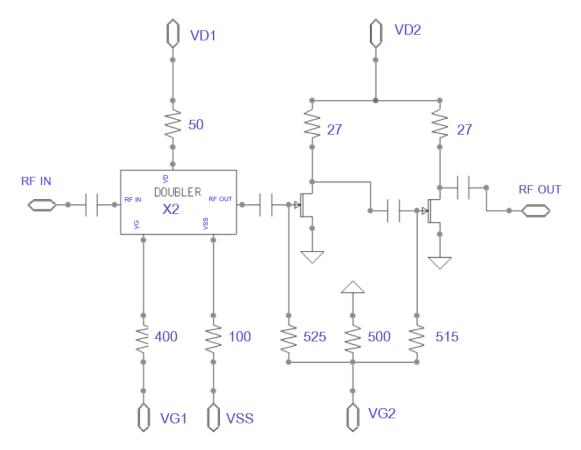
electronic devices sensitive These are to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 2 devices.

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Block Diagram & Schematics



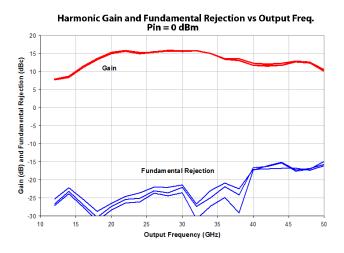
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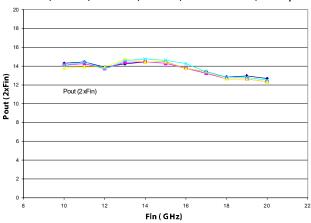


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Typical Performance Curves



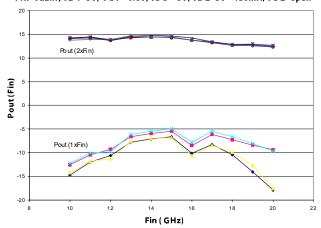
XX1000-BD_4_sa mples: Po ut (2xFin) vs. Fin (GHz) Pin=0dBm , VD 1=5V, VG 1=-0.6V, VS S=-5V, VD 2=5V ~150mA, VG 2=open



Pin = -8 to +6 dBm 20 Pout (2xFin) , Pin (dBm)=-8 15 , Fin (dBm)=-6 -, Rn (dBm)=-4 10 -, Pin (dBm)=2 -, Pin (dBm)=4 5 t (dBm) 0 , Pin (dBm)=6 , Pin (dBm)=-8 Pout -, Pin (dBm)=-6 -, Pin (dBm)=-4 -Pout (Fin) -10 -, Pin (dBm)=-2 -, Pin (dBm)=0 -15 →, Pin (dBm)=2 →, Pin (dBm)=4 -20 , Pin (dBm)=6 -25 8 10 12 14 16 18 20 22 Fin (GHz)

XX1000-BD: Pout (2xFin) and Pout (Fin) vs. Fin (GHz)

XX1000-BD_4_s amples: Pout (Fin) vs.Fin (GHz) Pin=0dBm, VD 1=5V, VG 1=-0.6V, VS S=-5V, VD 2=5V ~150mA, VG 2=open

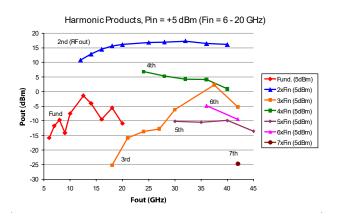


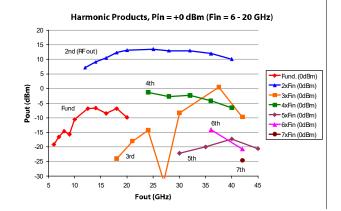
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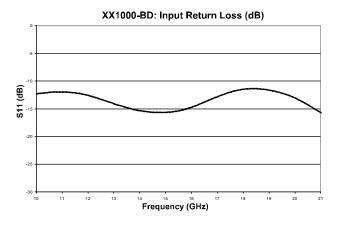


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Typical Performance Curves (cont.)







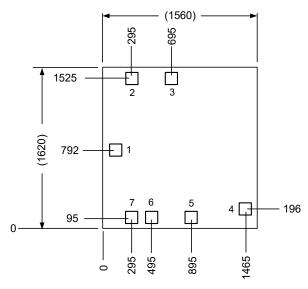
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Bond Pad Size (µm)

Pad	X	Y
1 - 7	100	100

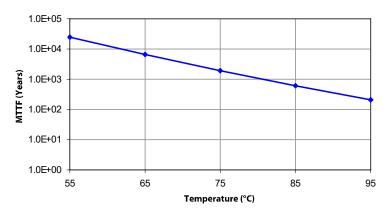
Unless otherwise specified, all dimensions are μm with a tolerance of ±5 $\mu m.$

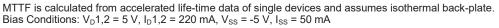
Die thickness is $110 \pm 10 \ \mu$ m.

Bond pad / backside metallization: Gold

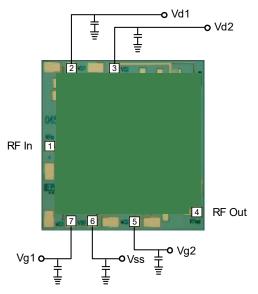
Die size reflects final cut dimensions.

MTTF vs. Back-plate Temperature (°C)





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Bypass Capacitors - See App Note [2]



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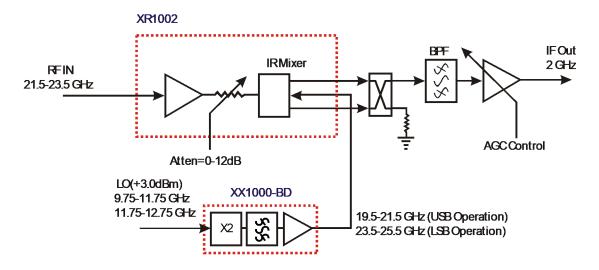
App Note [1] Biasing -

It is recommended to separately bias each doubler stage with fixed voltages of $V_D 1, 2 = 5$ V, $V_{SS} = -5$ V and $V_G 1 = -0.6$ V. The typical DC currents are $I_D 1 = 80$ mA, $I_D 2 = 140$ mA and $I_{SS} = 50$ mA. $V_G 2$ can be used for active control biasing of $V_D 2$, or it can be left open and $V_D 2$ will self bias at approximately 140 mA. Maximum output power is achieved with $V_{SS} = -5$ V and $I_{SS} = 50$ mA but the device will operate with reduced bias to $V_{SS} = -2$ V and $I_{SS} = 25$ mA. It is also recommended to use active biasing on $V_D 2$ with $V_G 2$ to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage for $V_G 2 = -0.1$ V. Typically the gate is protected with silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -

For individual stage bias (recommended for doubler applications) - Each DC pad (V_D 1,2, V_{SS} and V_G 1,2) needs to have DC bypass capacitance (~100 - 200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 μ F) is also recommended.

Typical Application



MMIC based 18 - 34 GHz Double / Receiver Block Diagram (changing LO and IF frequencies as required allows the design to operate as high as 34 GHz.

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