# XR1019-QH

## Receiver
## 27 - 34 GHz

Rev. V2

### Features

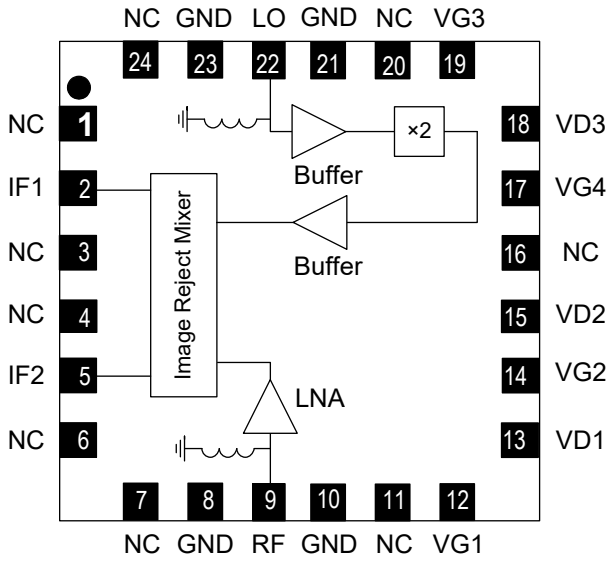
- Integrated LNA, Mixer and LO Multiplier
- 2.5 dB Noise Figure
- 13.0 dB Conversion Gain
- Lead-Free 4 mm 24-lead QFN Package
- 100% RF, DC and NF Testing
- RoHS* Compliant and 260°C Reflow Compatible

### Description

The XR1019-QH is a 27.0-34.0 GHz QFN packaged receiver that has a noise figure of 2.5 dB and 13 dB conversion gain. The device integrates an LNA, image reject mixer and LO multiplier and buffer amplifier within a fully molded 4×4 mm QFN package. The image reject mixer eliminates the need for a band pass filter after the LNA to remove thermal noise at the image frequency. I and Q mixer outputs are provided and an external 90 degree hybrid is required to select the desired sideband.

This device is specifically designed for Point to Point radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

### Functional Schematic




### Pin Configuration [2]

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 2 | IF1 Output | 15 | Drain<br>LNA Stage 2 |
| 5 | IF2 Output | 17 | Mixer Bias |
| 8 | Ground | 18 | Drain, LO Buffer |
| 9 | RF Input | 19 | Gate, LO Buffer |
| 10 | Ground | 21 | Ground |
| 12 | Gate<br>LNA Stage 1 | 22 | LO Input |
| 13 | Drain<br>LNA Stage 2 | 23 | Ground |
| 14 | Gate<br>LNA Stage 2 | 1,3,4,6,7,<br>11,16,20,24 | Not Connected |

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

### Ordering Information[1]

| Part Number | Package |
|---|---|
| XR1019-QH-0G00 | bulk quantity |
| XR1019-QH-0G0T | tape and reel |
| XR1019-QH-EV1 | evaluation module |

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

## Electrical Specifications: 27 - 34 GHz (RF), $T_A$ = +25°C

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Frequency Range (LO) | GHz | 12.5 | - | 18.0 |
| Frequency Range (IF) | GHz | DC | - | 2.0 |
| Conversion Gain (CG) | dB | - | 13 | - |
| Noise Figure (NF) | dB | - | 2.5 | - |
| Input Third Order Intercept (IIP3) | dBm | - | -2 | - |
| Image Rejection | dBc | - | 20 | - |
| LO Input Drive | dBm | 3 | 4 | 9 |
| 2×LO to RF Isolation | dBm | - | -25 | - |
| RF Input Return Loss | dB | - | 10 | - |
| LO Input Return Loss | dB | - | 10 | - |
| IF Return Loss | dB | - | 12 | - |
| Drain Bias Voltage ($V_D$1,2,3) | VDC | - | 3 | - |
| Gate Bias Voltage ($V_G$1,2,3)[3] | VDC | - | -0.35 | - |
| Gate Bias Voltage ($V_G$4)[4] | VDC | -3.8 | -3.0 | -2.0 |
| Supply Current ($I_D$1) | mA | - | 7.5 | - |
| Supply Current ($I_D$2) | mA | - | 30 | - |
| Supply Current ($I_D$3) | mA | - | 90 | - |
| Supply Current ($I_G$4) | mA | - | 10 | - |

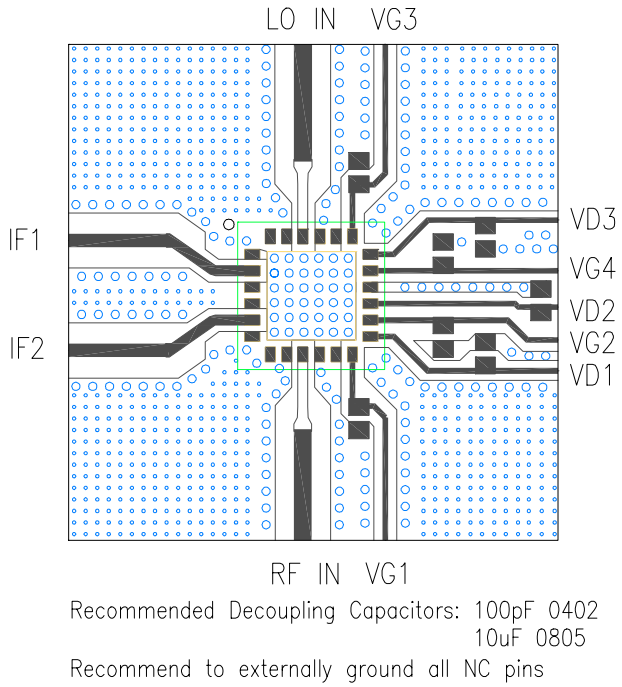
3. $V_G$1,2 and 3 are adjusted to achieve constant drain current regulation.
4. $V_G$4 provides mixer bias and is fixed at -3.0 V.

## Absolute Maximum Ratings [5,6]

| Parameter | Absolute Maximum |
|---|---|
| Supply Voltage ($V_D$1,2,3) | +4.3 V |
| Supply Current ($I_D$1,2,3) | 200 mA |
| Gate Bias Voltage ($V_G$1,2,3) | -1.7 V min., 0 V max. |
| Gate Bias Voltage ($V_G$4) | -4 V |
| RF Input Power | +5 dBm |
| LO Input Power | +13 dBm |
| Storage Temperature (Tstg) | -65°C to +150°C |
| Operating Temperature (Ta) | -55°C to +85°C |
| Channel Temperature (Tch) | +150ºC |
| ESD-Machine Model | Class A |
| ESD-Human Body Model | Class 1A |
| Moisture Sensitivity Level | MSL3 |

5. Operation of this device above any one of these parameters may cause permanent damage.
6. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

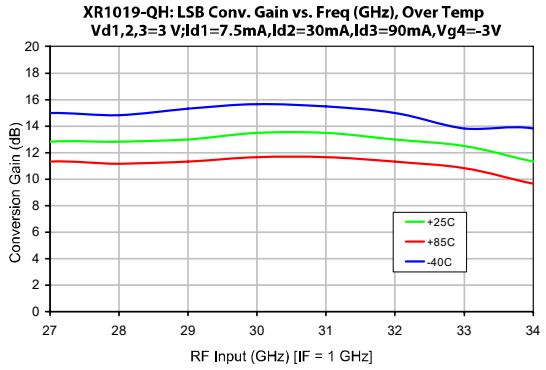
## Recommended Board Layout

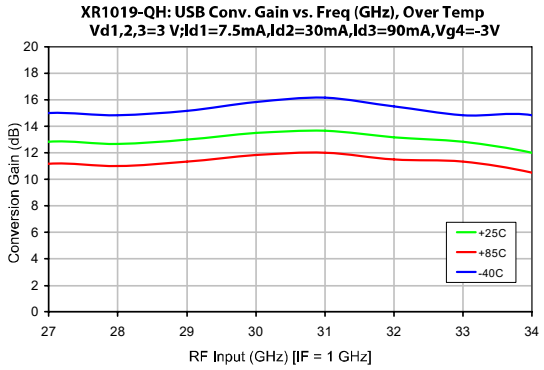


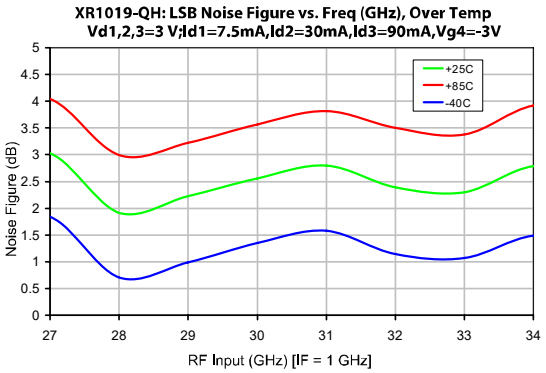

**App Note [1] Biasing** - As shown in the Pin Designations table, the device is operated by biasing $V_D$1,2,3 at 3.0 V with 7.5, 30, 90 mA respectively. Additionally, a fixed voltage bias of -3 V is required for mixer bias. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.35 V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

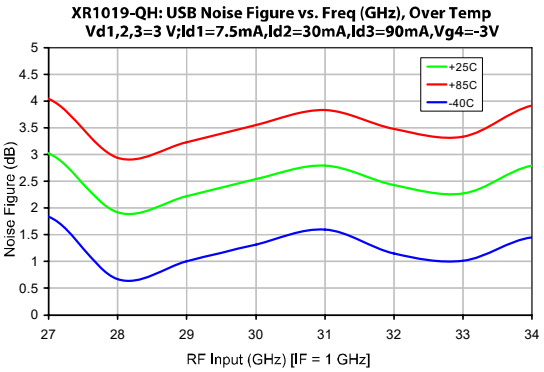
**App Note [2] Board Layout** - As shown in the board layout, it is recommended to provide 100 pF decoupling caps as close to the bias pins as possible, with additional 10 µF decoupling caps.

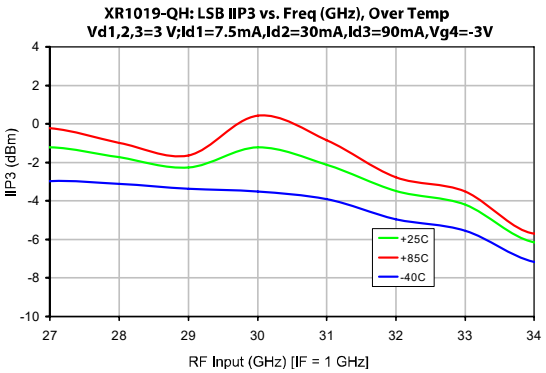
## Typical Performance Curves

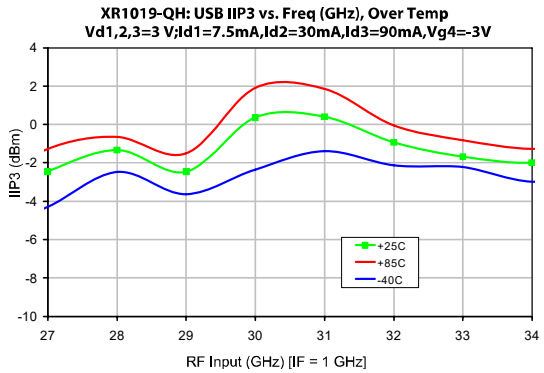


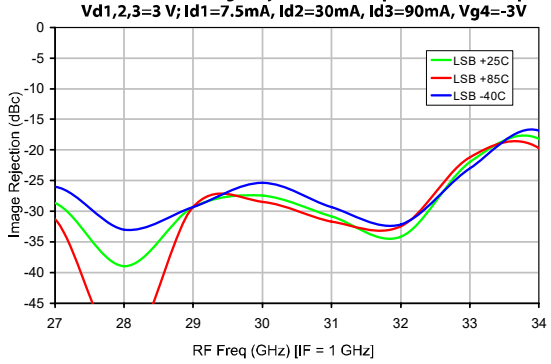



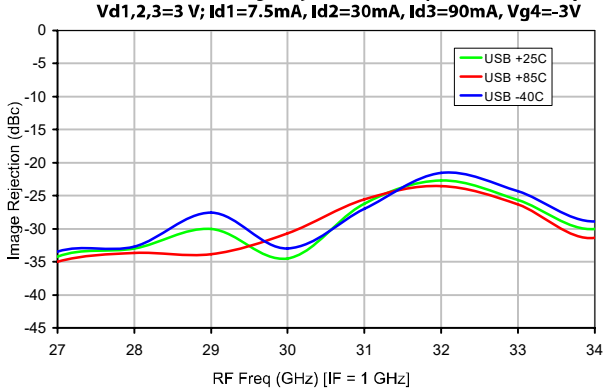



## Typical Performance Curves (cont.)

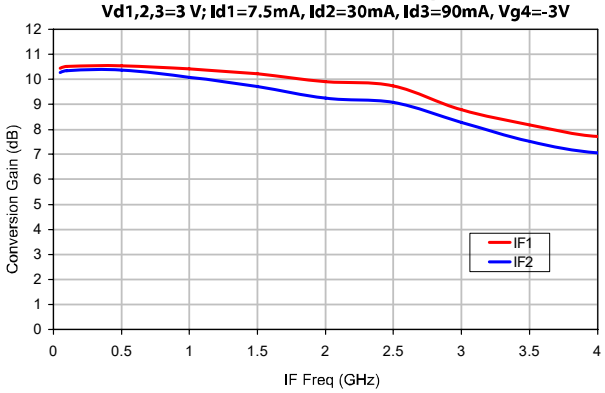
**XR1019-QH: LSB Image Rejection vs. Freq (GHz), Over Temp**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**



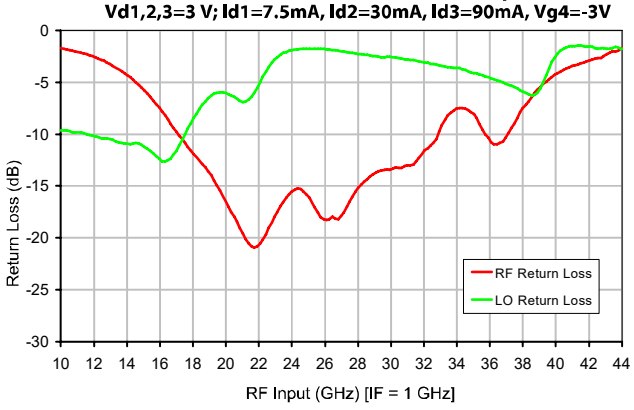

**XR1019-QH: USB Image Rejection vs. Freq (GHz), Over Temp**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**



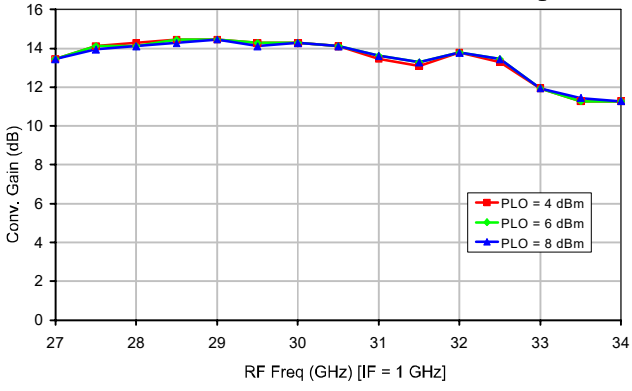

**XR1019-QH: Conv. Gain vs IF Freq (GHz)**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**



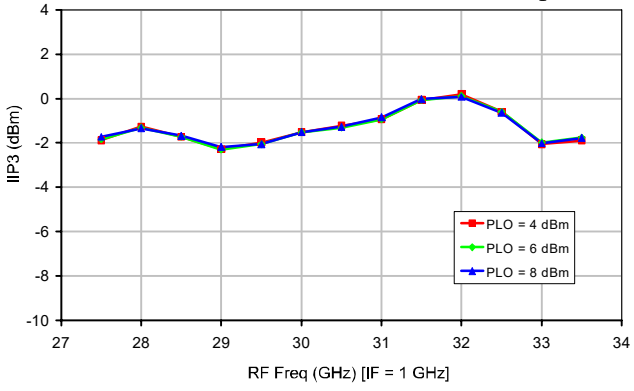

**XR1019-QH: RF and LO Return Loss vs. Freq (GHz)**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**



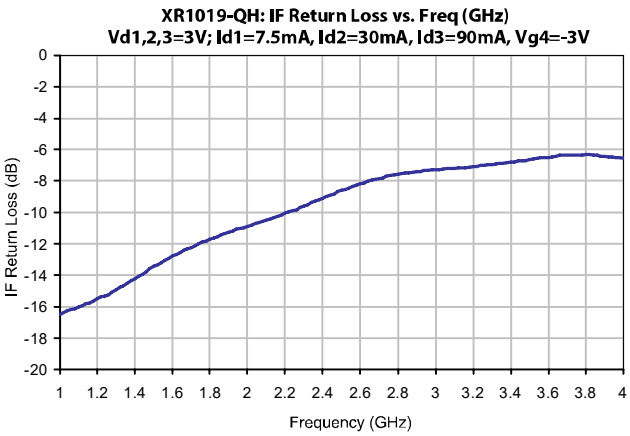

**XR1019-QH: USB Conv. Gain vs Freq (GHz), Varying LO Power**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**

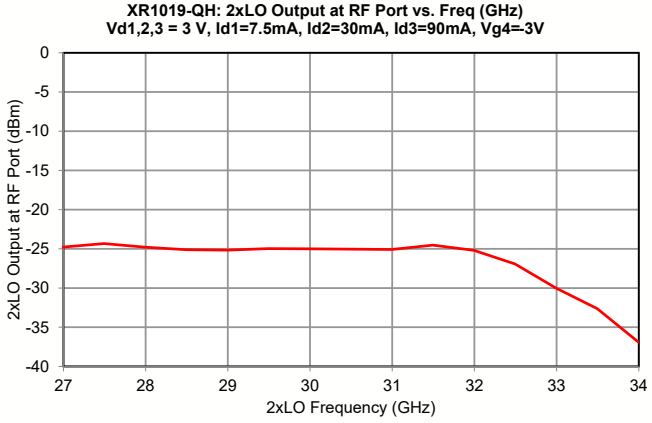



**XR1019-QH: USB IIP3 vs Freq (GHz), Varying LO Power**
**Vd1,2,3=3 V; Id1=7.5mA, Id2=30mA, Id3=90mA, Vg4=-3V**

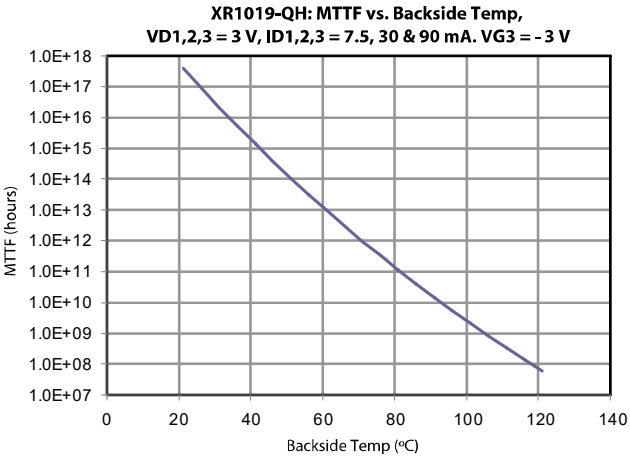


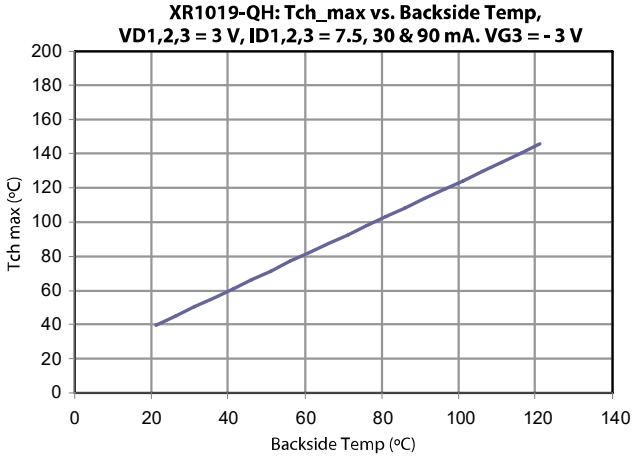
## Typical Performance Curves (cont.)



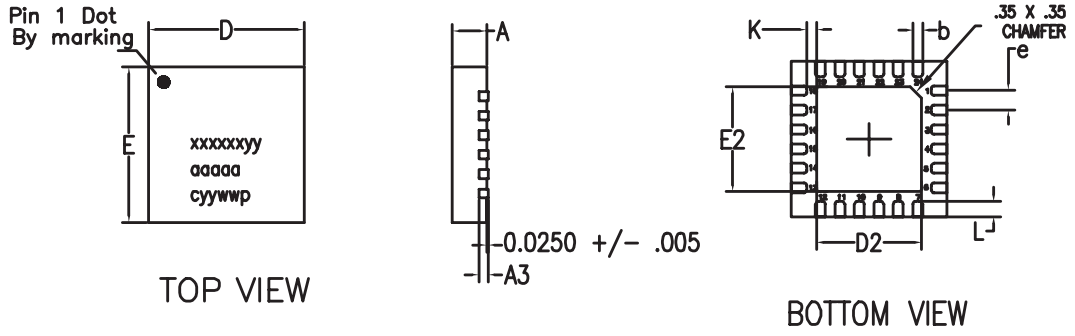

## MTTF




MTTF is calculated from accelerated life-time data of single devices and assumes an isothermal back-plate.

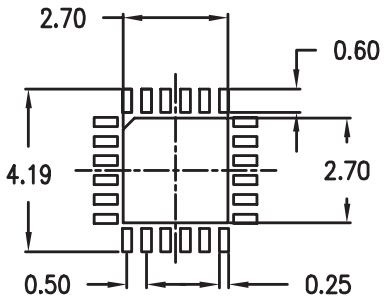
## *Lead-Free 4* mm 24-Lead PQFN†




MARKINGS:
PIN 1/BOM REV/Pb FREE SYM
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE

NOTES:
1. DIMENSIONS ARE IN MM.

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




| | MIN | TYP | MAX |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A3 | | 0.20 REF | |
| b | 0.20 | 0.25 | 0.30 |
| K | 0.20 | – | – |
| D | | 4.00 BSC | |
| E | | 4.00 BSC | |
| e | | 0.50 | |
| D2 | 2.45 | 2.60 | 2.75 |
| E2 | 2.45 | 2.60 | 2.75 |
| L | 0.20 | 0.30 | 0.40 |

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.