

Buffer Amplifier 35 - 45 GHz

Rev. V1

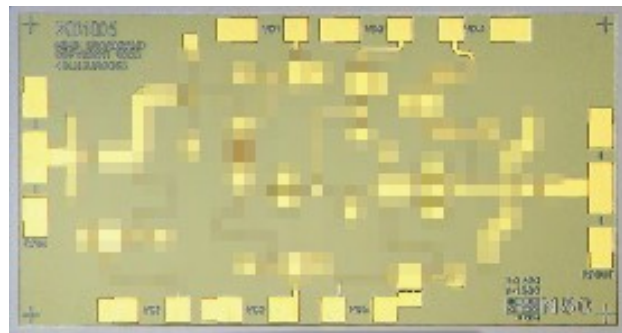
Features

- High Dynamic Range
- Excellent LO Driver/Buffer Amplifier
- Low Noise or Power Bias Configurations
- 23.0 dB Small Signal Gain
- 2.7 dB Noise Figure at Low Noise Bias
- +16 dBm P1dB Compression at Power Bias
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's three stage 35.0-45.0 GHz GaAs MMIC buffer amplifier has a small signal gain of 23.0 dB with a noise figure of 2.7 dB across the band. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	180 mA
Gate Bias Voltage (Vg)	+0.3 V
Input Power (Pin)	+5 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to MTTF Table ¹
Channel Temperature (Tch)	MTTF Table ¹

1. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Ordering Information

Part Number	Package
XB1005-BD-000V	"V" - vacuum release gel paks
XB1005-BD-EV1	evaluation module

Electrical Specifications: 35-45 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11) ³	dB	4.0	8.0	-
Output Return Loss (S22) ³	dB	9.0	17.0	-
Small Signal Gain (S21) ³	dB	20.0	23.0	27.0
Gain Flatness ($\Delta S21$)	dB	-	+/-1.0	-
Reverse Isolation (S12) ³	dB	35.0	45.0	-
Noise Figure (NF) ⁴	dB	-	2.7	3.5
Output Power for 1dB Compression Point (P1dB) ^{1,2,3}	dBm	-	+16.0	-
Output Third Order Intercept Point (OIP3) ^{1,2,3}	dBm	-	+26.0	-
Saturated Output Power (Psat) ^{1,2,3}	dBm	+16.0	+18.0	-
Drain Bias Voltage (Vd1,2,3)	VDC	-1.2	+3.5	+4.5
Gate Bias Voltage (Vg1,2,3)	VDC	-	-0.4	+0.1
Supply Current (Id) (Vd=3.5 V, Vg=-0.4 V Typical)	mA	-	50	154

1. Optional low noise bias Vd1,2,3=3.5 V, Id=50 mA will typically yield 3-4 dB decreased P1dB and OIP3.
2. Measured using constant current.
3. Unless otherwise indicated Min/Max over 35.0-45.0 GHz and biased at Vd=4.5 V, Id1=28 mA, Id2=42 mA, Id3=84 mA.
4. Unless otherwise indicated Min/Max over 35.0-45.0 GHz and biased at Vd=3.5 V, Id1=9 mA, Id2=16 mA, Id3=25 mA.

Handling Procedures

Please observe the following precautions to avoid damage:

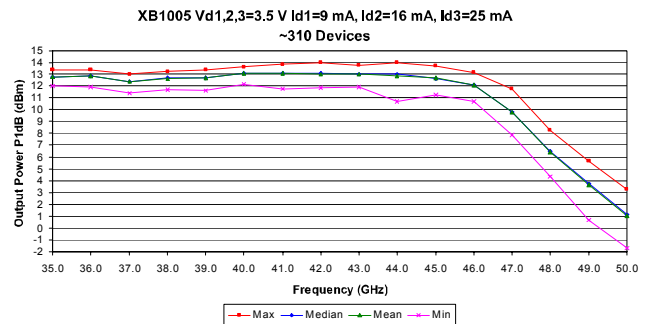
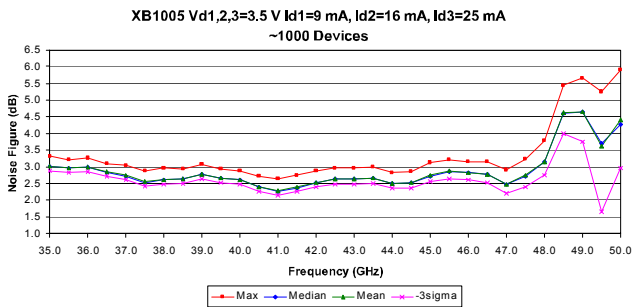
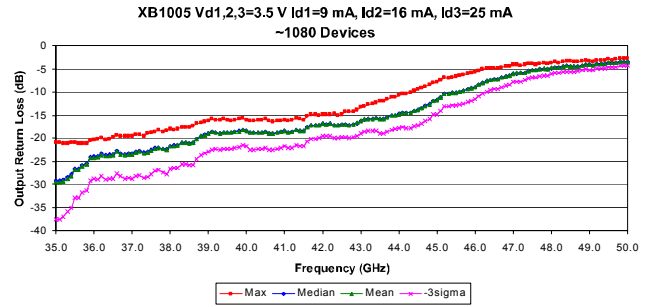
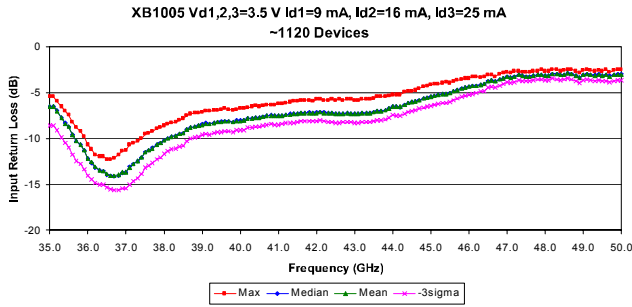
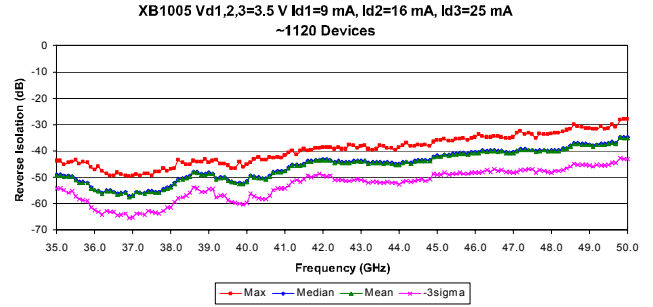
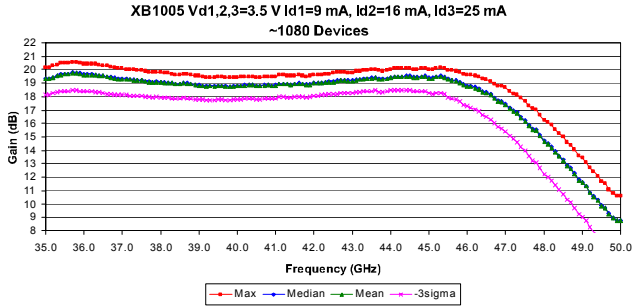
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

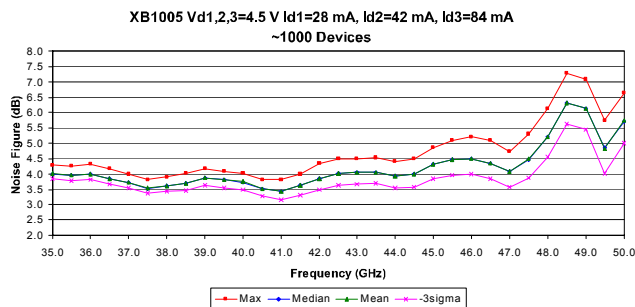
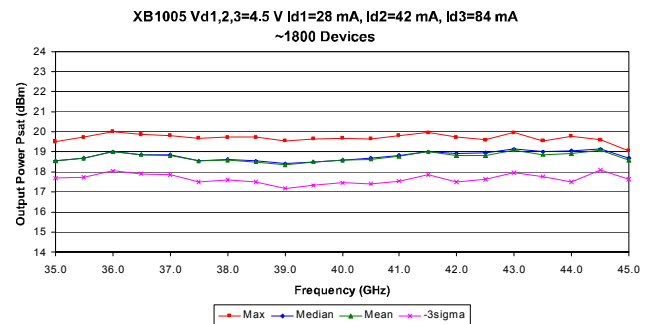
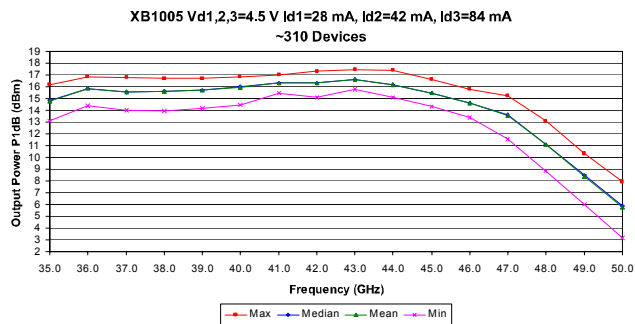
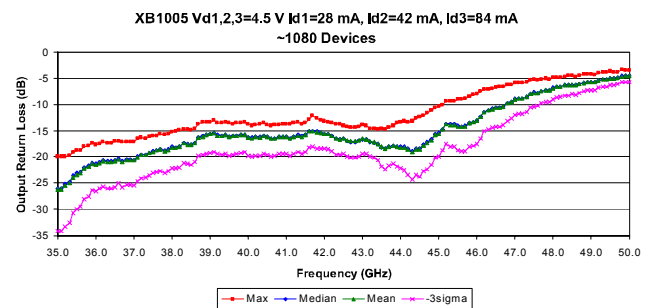
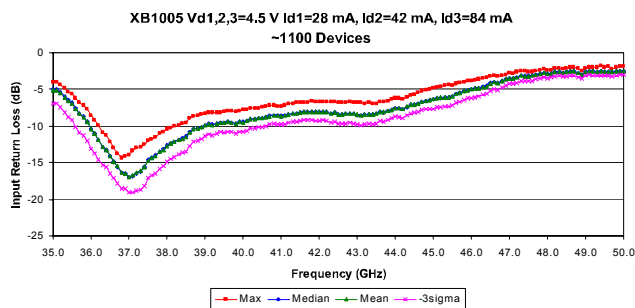
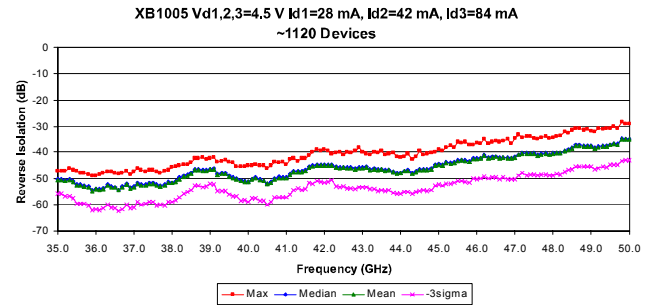
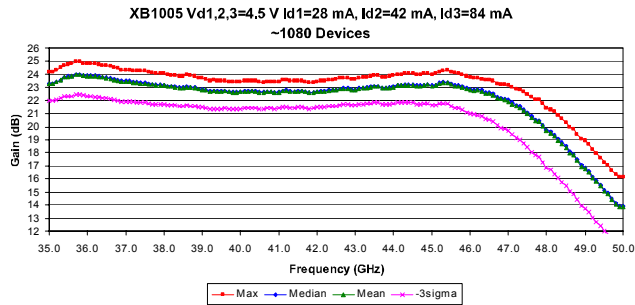
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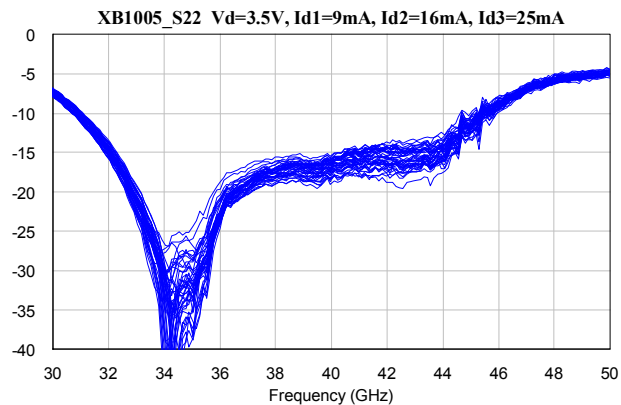
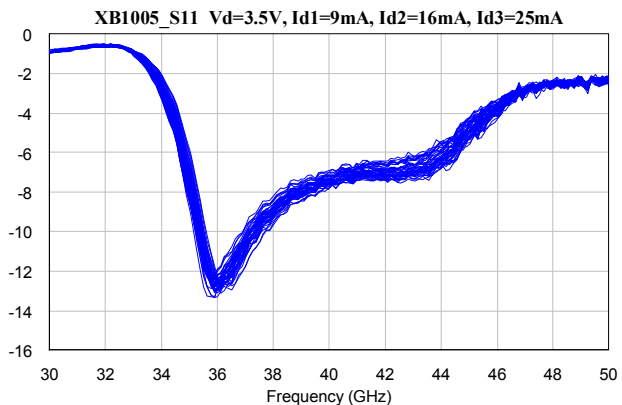
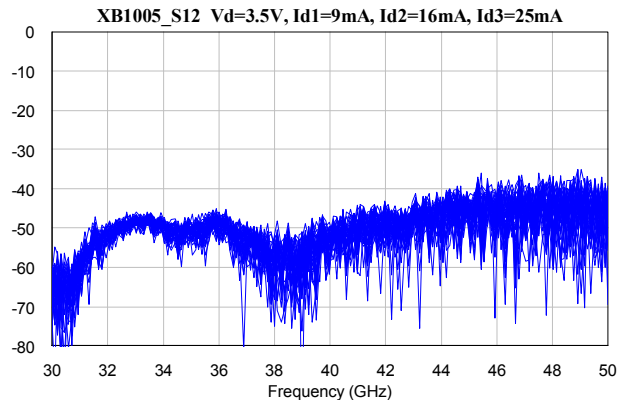
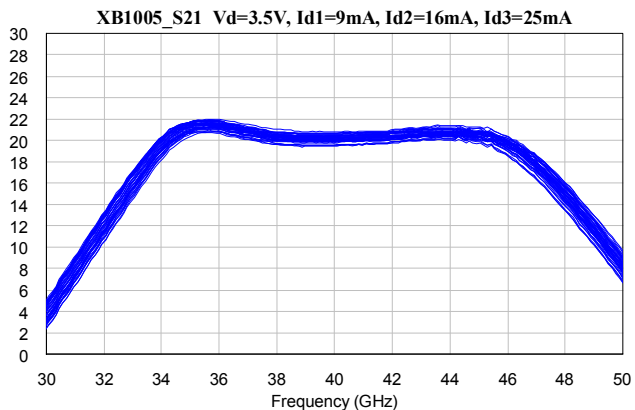
Typical Performance Curves



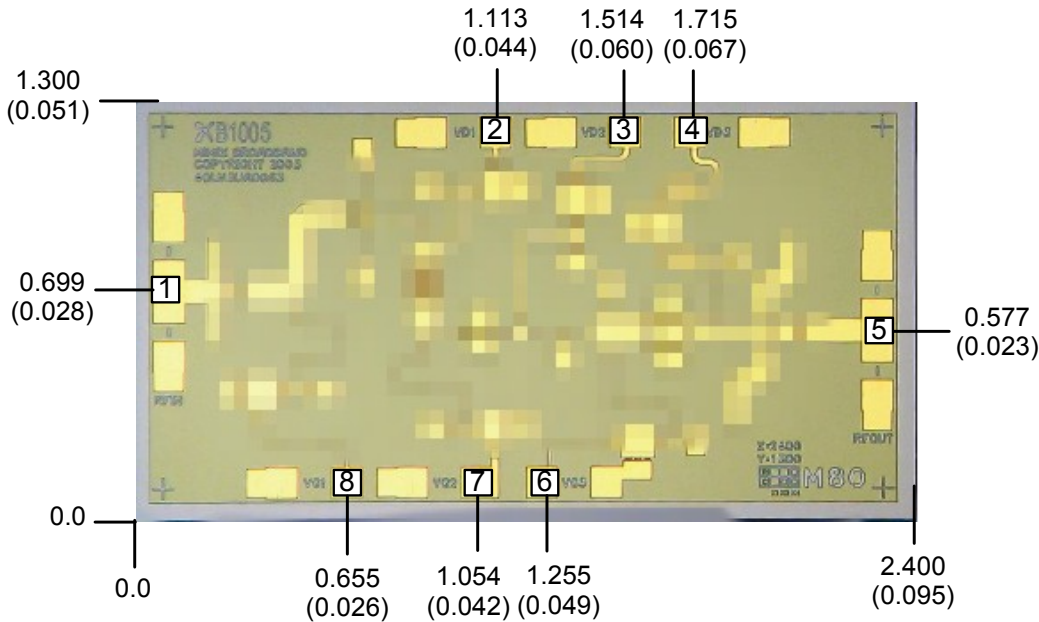
Typical Performance Curves (cont.)



Typical Performance Curves (cont.)



Mechanical Drawing

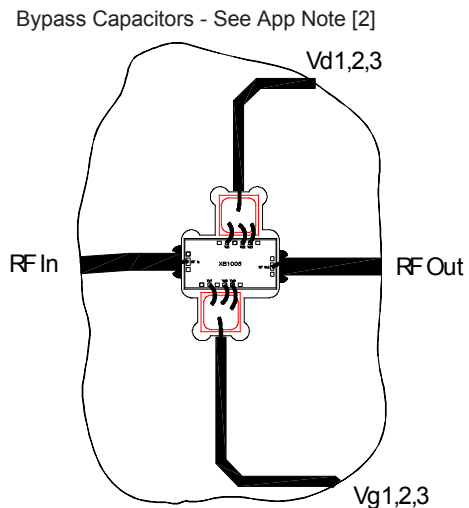
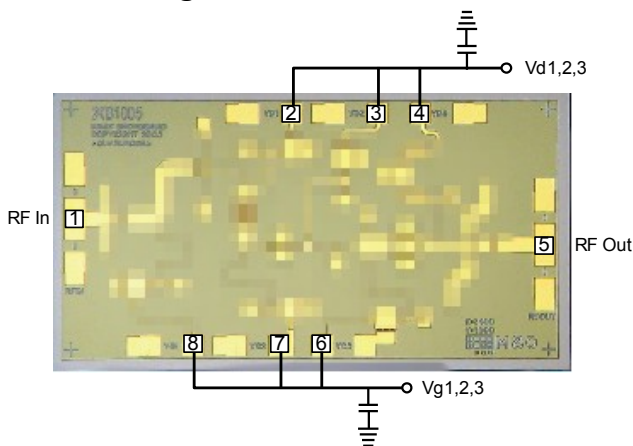


(Note: Engineering designator is 40LN3UA0063)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
 Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
 All DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
 Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
 Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 1.931 mg.

Bond Pad #1 (RF In)	Bond Pad #3 (Vd2)	Bond Pad #5 (RF Out)	Bond Pad #7 (Vg2)
Bond Pad #2 (Vd1)	Bond Pad #4 (Vd3)	Bond Pad #6 (Vg3)	Bond Pad #8 (Vg1)

Bias Arrangement



MTTF Tables

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	82.9 deg Celsius	159.3° C/W	8.36E+10	1.20E-02
75 deg Celsius	105.0 deg Celsius	171.3° C/W	5.382E+09	1.86E-01
95 deg Celsius	126.8 deg Celsius	182.0° C/W	4.796E+08	2.09E+00

Bias Conditions: Vd1=Vd2=Vd3=3.5 V, Id1=9 mA, Id2=16 mA, Id3=25 mA

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	157.3 deg Celsius	147.6° C/W	3.00E+07	3.34E+01
75 deg Celsius	184.0 deg Celsius	157.3° C/W	3.07E+06	3.26E+02
95 deg Celsius	210.1 deg Celsius	166.1° C/W	4.21E+05	2.37E+03

Bias Conditions: Vd1=Vd2=Vd3=4.5 V, Id1=28 mA, Id2=42 mA, Id3=84 mA

App Note [1] Biasing - As shown in the bonding diagram, this device can be operated with all three stages in parallel, and can be biased for low noise performance or high power performance. Low noise bias is nominally Vd=3.5V, Id=50mA. More controlled performance will be obtained by separately biasing Vd1, Vd2 and Vd3 each at 3.5V, with Id1=9mA, Id2=16mA, Id3=25mA. Power bias may be as high as Vd=4.5V, Id=154mA with all stages in parallel, or most controlled performance will be obtained by separately biasing Vd1, Vd2 and Vd3 each at 4.5V, with Id1=28mA, Id2=42mA, Id3=84mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.4V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -

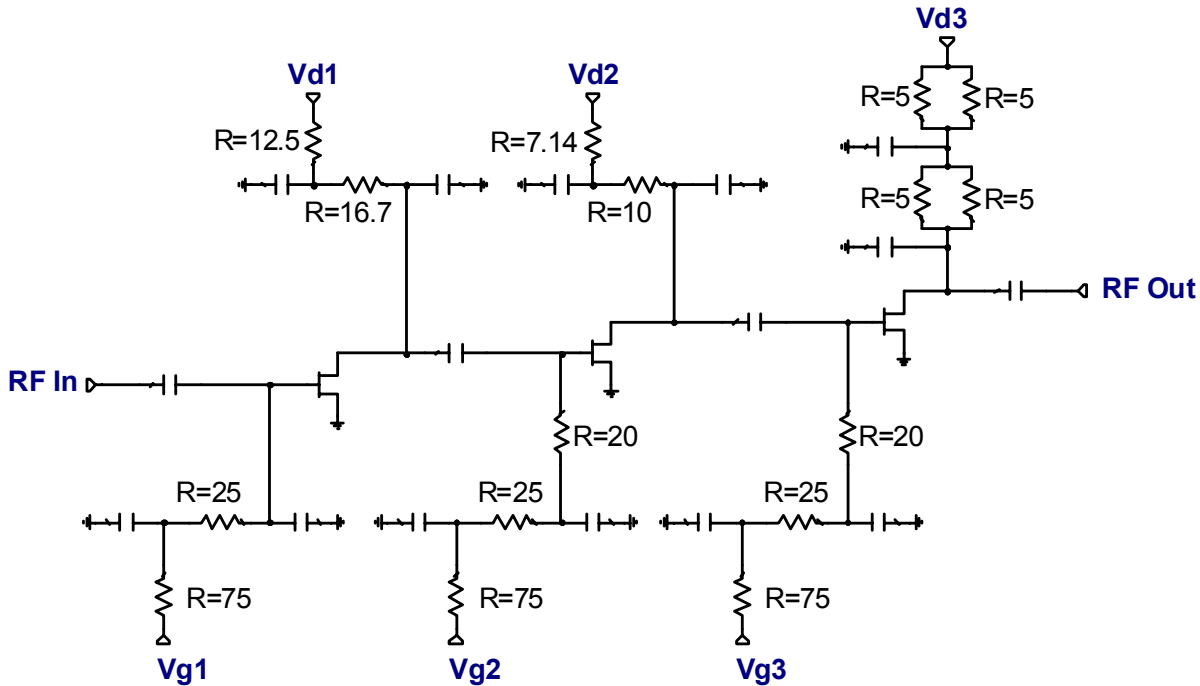
For Parallel Stage Bias (Recommended for general applications) -- The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors (~100-200 pf) can be combined. Additional DC bypass capacitance (~0.01 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads.

For Individual Stage Bias (Recommended for Saturated Applications) -- Each DC pad (Vd1,2,3 and Vg1,2,3) needs to have DC bypass capacitance (~100-200 pf) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

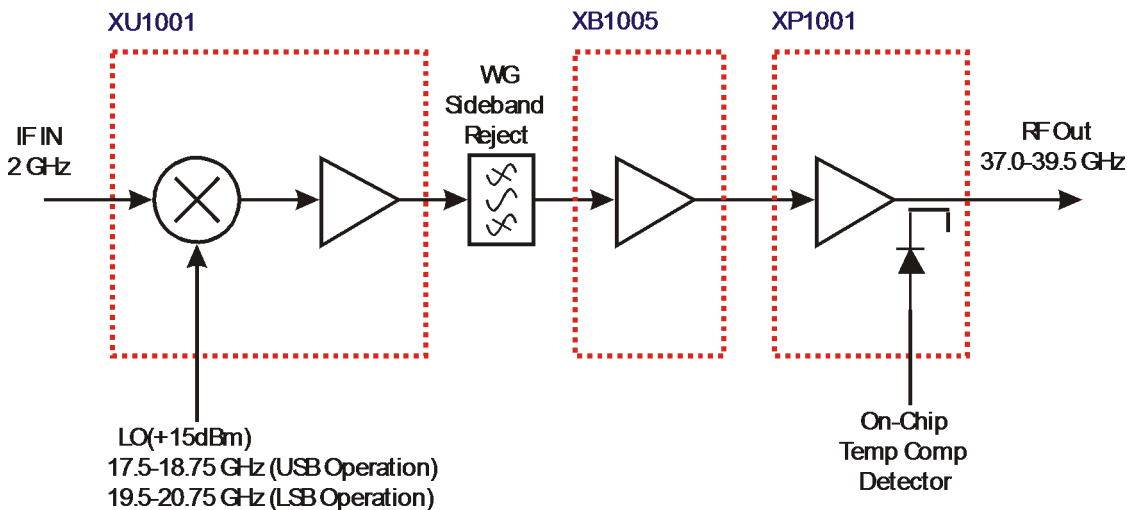
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Device Schematic



Typical Application



M/A-COM Tech MMIC-based 36.0-40.0 GHz Transmitter Block Diagram
(Changing LO and IF frequencies as required allows design to operate as high as 40 GHz)

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