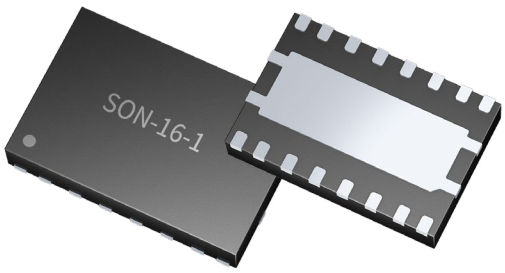
PTVA120252MT

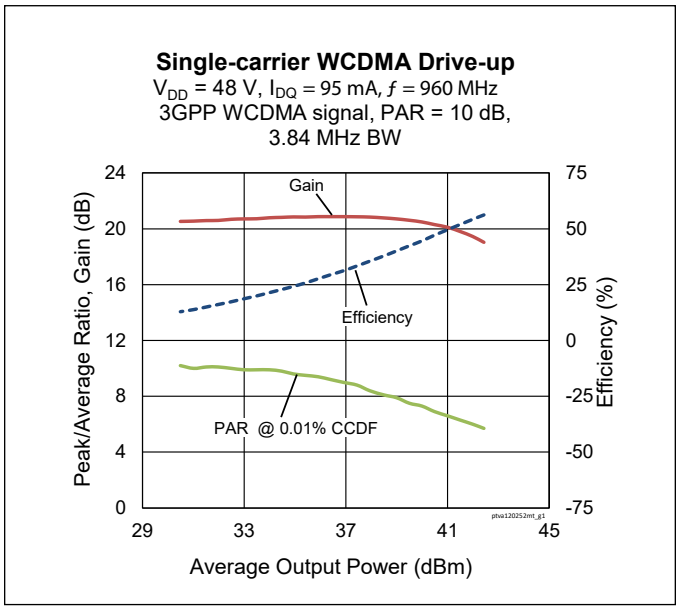
Thermally-Enhanced High Power RF LDMOS FET
25 W, 48 V, 500 – 1400 MHz



Package Types: PG-SON-16

Description

The PTVA120252MT LDMOS FET is a 25-watt LDMOS FET designed for use in power amplifier applications in the 500 MHz to 1400 MHz frequency band. Features include high gain and a thermally-enhanced, surface-mount package. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Unmatched
- Target CW performance 960 MHz, 48 V, combined outputs
  - Output power at P_{1dB} = 25 W
  - Gain = 19.8 dB
  - Efficiency = 64%
- Capable of handling 10:1 VSWR @ 48 V, 20 W CW output power
- Integrated ESD protection
- Human Body Model class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in a the production test fixture)
V_{DD} = 48 V, I_{DQ} = 87 mA, P_{OUT} = 5.5 W average, f = 960 MHz, 3GPP WCDMA signal, 3.84 MHz bandwidth, 10 dB PAR @0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Linear Gain	G_{ps}	18.5	19.5	—	dB
Drain Efficiency	η_D	28	31.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–33.5	–31	dBc

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics (each side)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	105	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current	I_{DSS}	—	—	1	µA	V_{DS} = 50 V, V_{GS} = 0 V
		—	—	10		V_{DS} = 105 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	1		V_{GS} = 10 V, V_{DS} = 0 V
On-State Resistance	$R_{DS(on)}$	—	2.8	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
Operating Gate Voltage	V_{GS}	3	3.65	4	V	V_{DS} = 48 V, I_{DQ} = 85 mA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	–6 to +12	
Operating Voltage	V_{DD}	0 to +55	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance	$R_{\theta JC}$	2.6	°C/W	T_{CASE} = 70°C, 25 W CW

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTVA120252MT V1 R1K	PTVA120252MTV1-R1K	PG-SON-16, plastic package	Tape & Reel, 1000 pcs

Typical RF Performance (data taken in production test fixture)

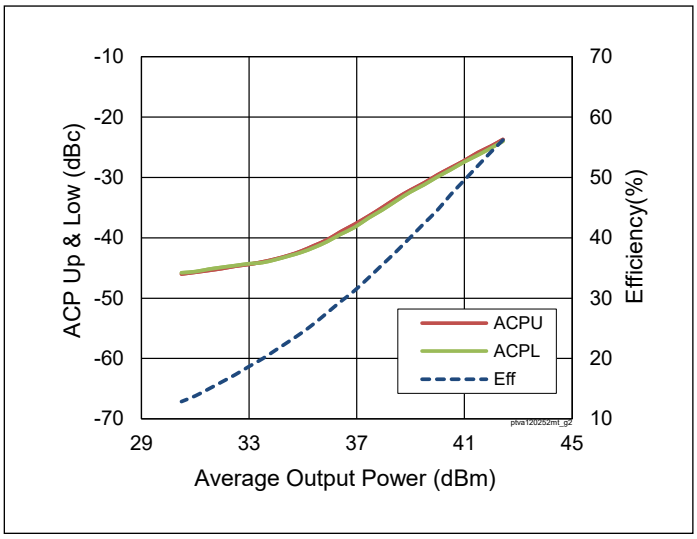


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, I_{DQ} = 95 mA, f = 960 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz

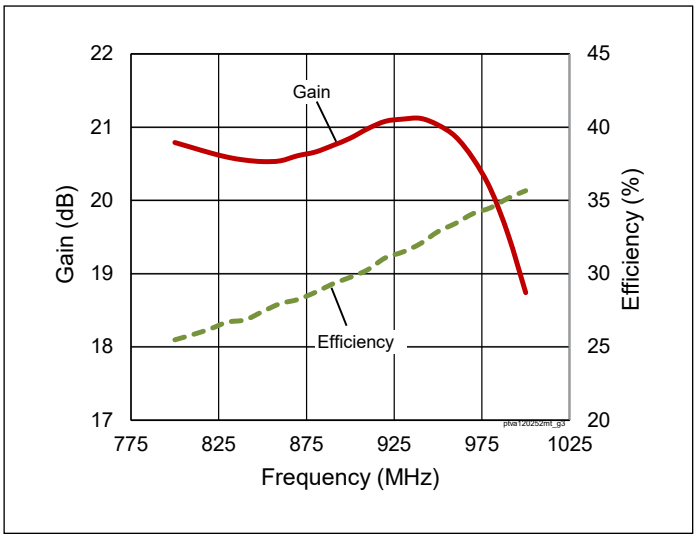


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, I_{DQ} = 95 mA, P_{OUT} = 37.4 dBm,
3GPP WCDMA signal, PAR = 10 dB

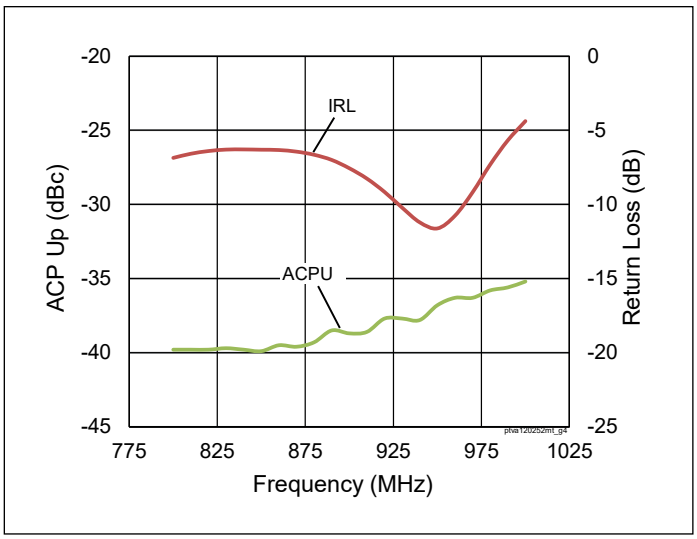


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, I_{DQ} = 95 mA, P_{OUT} = 37.4 dBm,
3GPP WCDMA signal, PAR = 10 dB

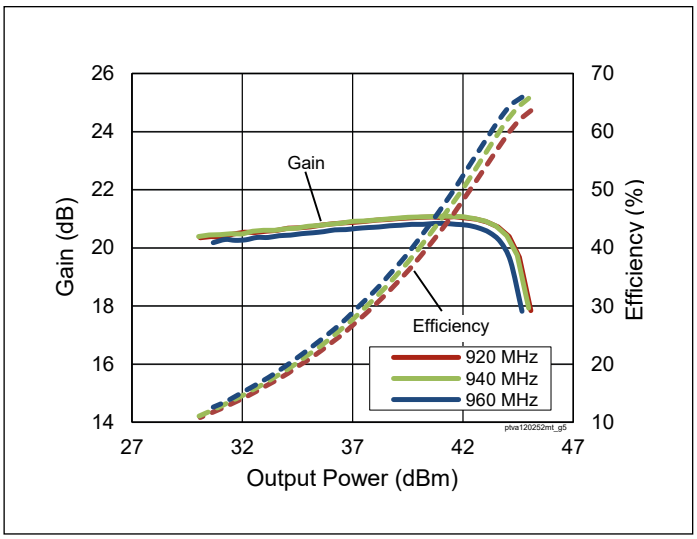


Figure 4. CW Performance

V_{DD} = 48 V, I_{DQ} = 95mA

Typical Performance (cont.)

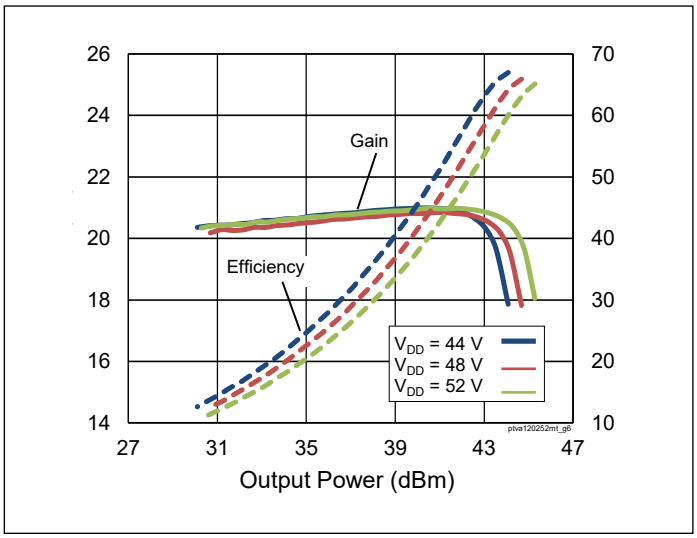


Figure 5. CW Performance at various V_{DD}

I_{DQ} = 95 mA, f = 960 MHz

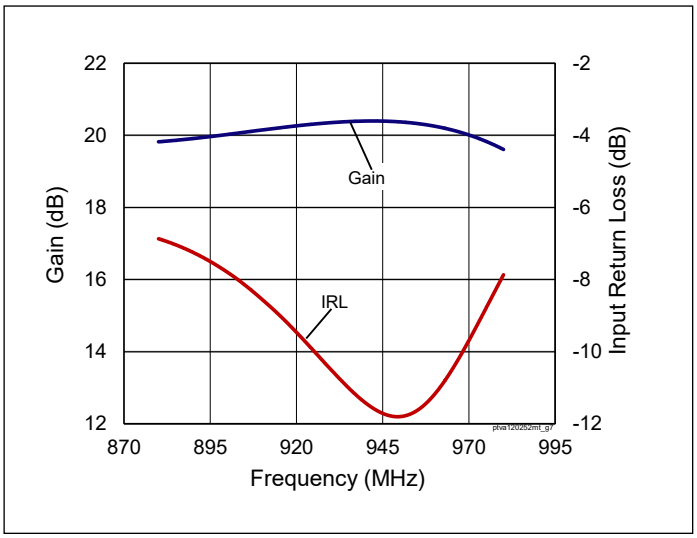


Figure 6. Small Signal CW Gain & Input Return Loss

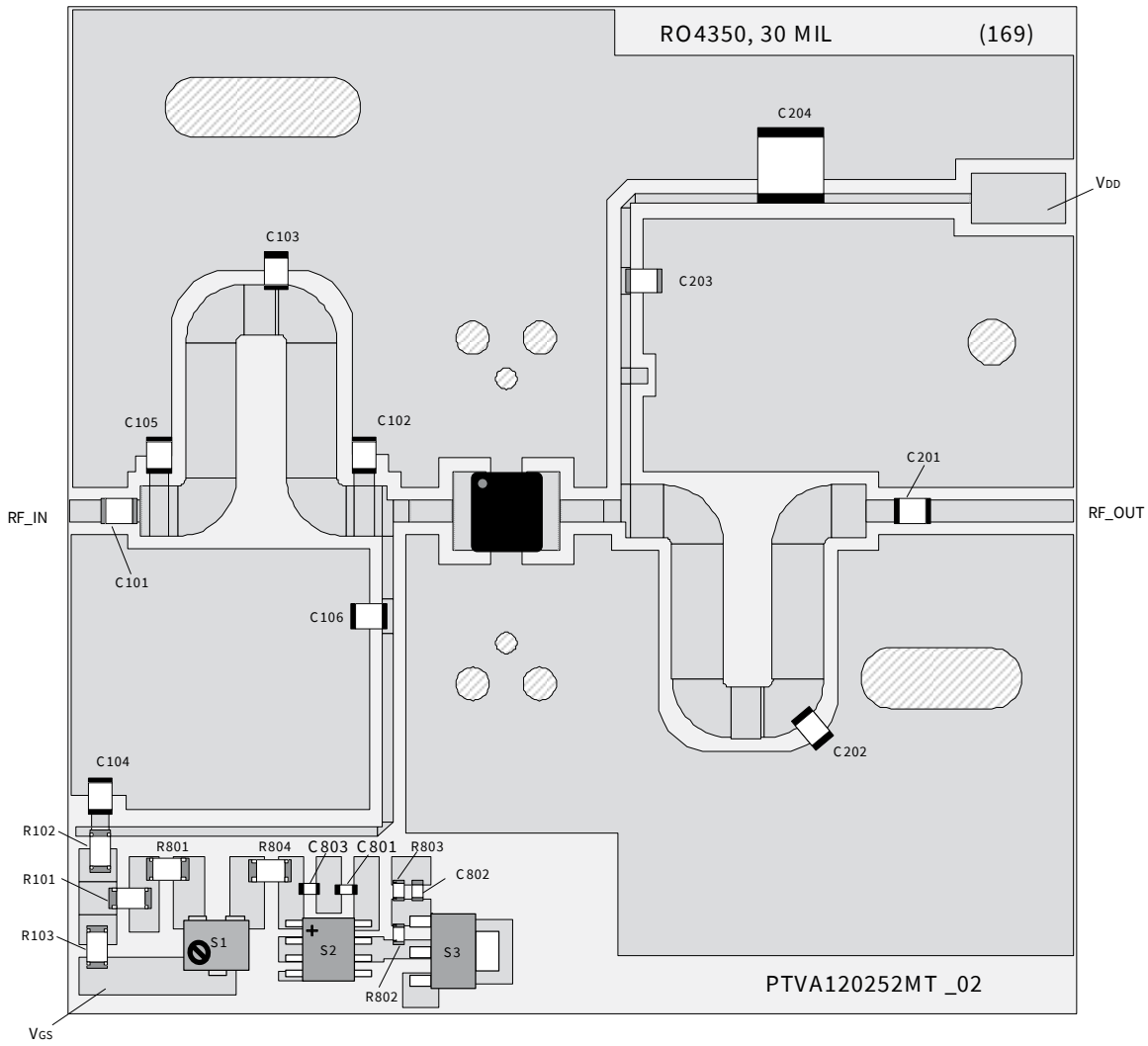
V_{DD} = 48 V, I_{DQ} = 95 mA

Load Pull Performance

Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 40 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
791	3.12+j7.44	18.94+j8.73	20.85	45.06	32.06	60.1	10.67+j26.27	23.27	41.79	15.10	70.8
821	3.2+j7	18.77+j9.38	20.54	45.03	31.84	59.7	10+j25.7	22.94	41.76	15.00	69.8
869	3.08+j6.56	20.14+j8.78	19.75	44.95	31.26	58.0	14.39+j21	21.46	43.59	22.86	68.0
894	3.02+j6.56	19.72+j9.41	19.41	44.79	30.13	57.5	9.22+j25.02	21.61	41.69	14.76	68.2
925	2.9+j6.12	20.67+j9.26	18.85	45.06	32.06	57.6	14.61+j21.69	20.44	43.55	22.65	66.0
960	2.86+j5.68	18.72+j9.45	18.2	44.80	30.20	55.6	9.75+j23.93	20.24	42.07	16.11	65.5

Evaluation Board, 925 – 960 MHz



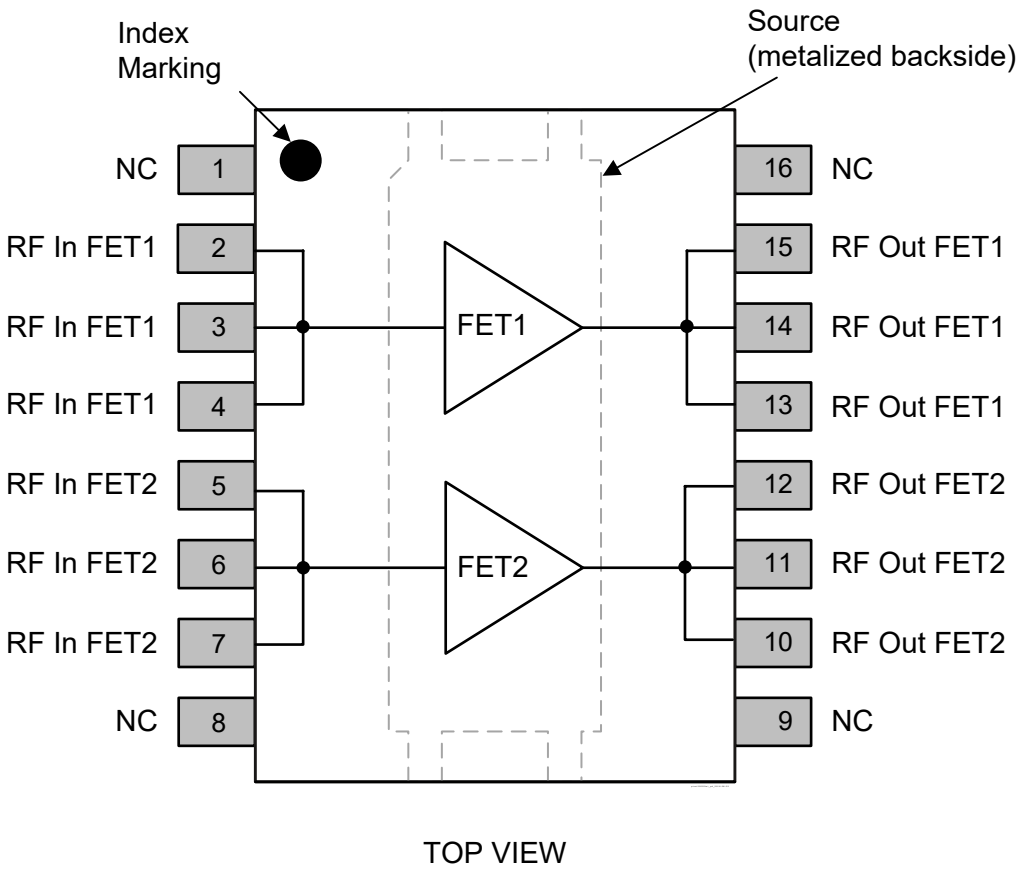
Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTNPTVA120252MT-V1
PCB Information	Rogers 4350, 0.762 mm [0.030”] thick, 2 oz. copper, ε_r = 3.66, f = 925 – 960 MHz

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C104, C106	Capacitor, 75 pF	ATC	ATC100B750JW500XB
C102	Capacitor, 14 pF	ATC	ATC100B140KW500XB
C103	Capacitor, 2.2 pF	ATC	ATC100B2R2DW500XB
C105	Capacitor, 2.5 pF	ATC	ATC100B2R5CW500XB
R101, R103	Resistor, 200 ohms	Panasonic Electronic Components	ERJ-8GEYJ201V
R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
Output			
C201, C203	Capacitor, 75 pF	ATC	ATC100B750JW500XB
C202	Capacitor, 2.0 pF	ATC	ATC100B2R0CW500XB
C204	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C801,C802, C803	Capacitor, 1000 pF	Panasonic Electronic Components	ECJ-1VB1H102K
R801	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R802	Resistor, 1.2K ohms	Panasonic Electronic Components	ERJ-3GEYJ122V
R803	Resistor, 1.3K ohms	Panasonic Electronic Components	ERJ-3GEYJ132V
R804	Resistor, 100 ohms	Panasonic Electronic Components	ERJ-8GEYJ101V
S1	Potentiometer 2K ohms	Bourns Inc.	3224W-1-202E
S2	Voltage Regulator	Texas Instruments	LM78L05ACM
S3	Transistor	Infineon Technologies	BCP56

Pinout Diagram (top view)



TOP VIEW

Description	**Pin**
Gate	2 – 7
Drain	10 – 15
Source	bottom metalization
	not connected
	1, 8, 9, 16

Package Outline Specifications – Package PG-SON-16

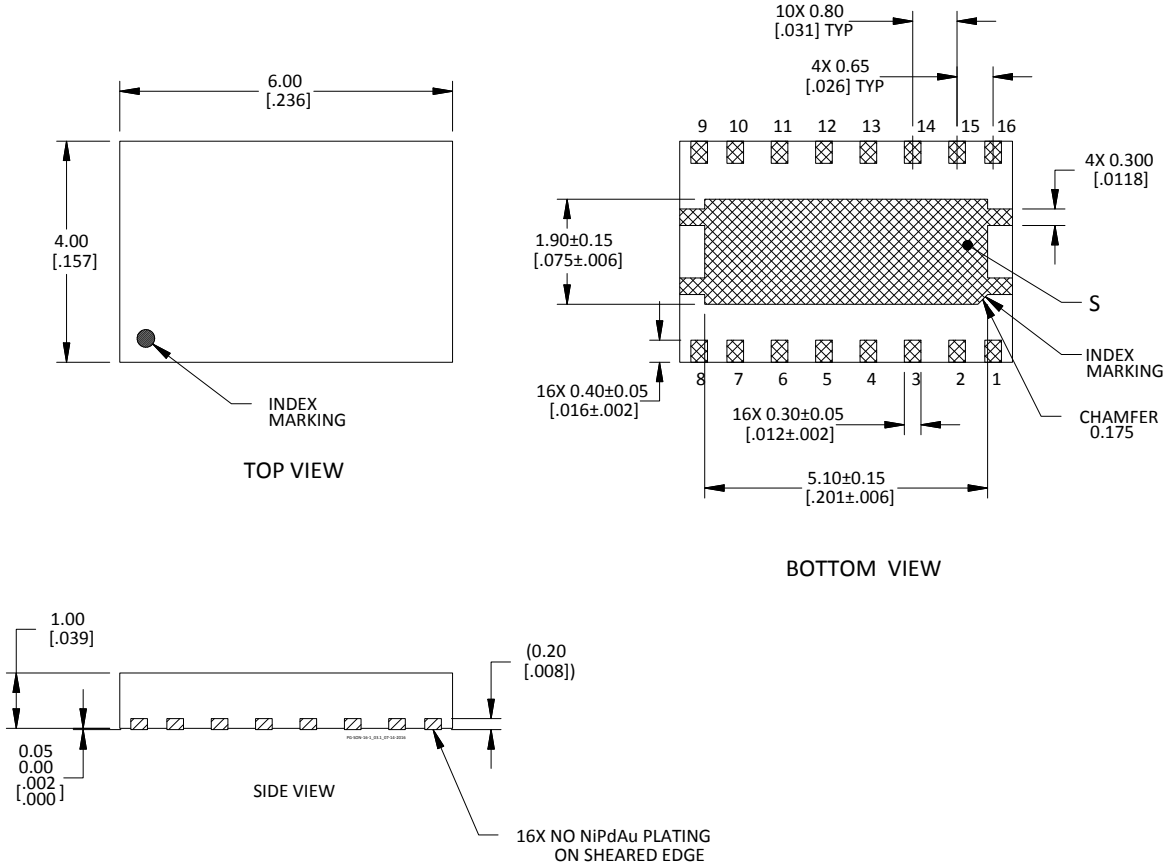


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.1 [.004].
4. Package dimensions 4.00 mm X 6.00 mm X 1.00 mm.
5. Pins: 2 – 7, gate; 10 – 15, drain; S, source (bottom metalization); 1, 8, 9, 16, not connected.
6. Gold plating thickness: 0.025 – 0.127 micron [1 – 5 microinch].

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