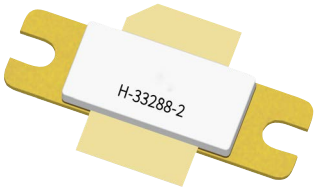
PTVA104501EH

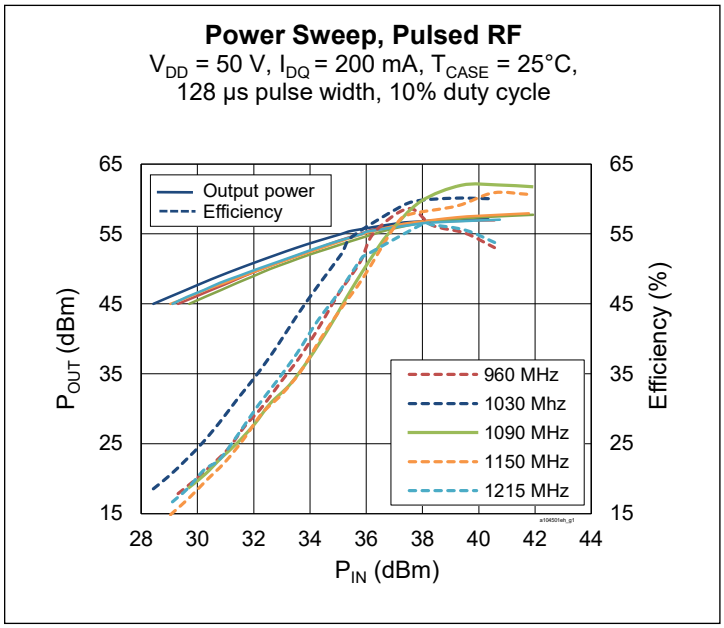
Thermally-Enhanced High Power RF LDMOS FET
450 W, 50 V, 960 – 1215 MHz

Description

The PTVA104501EH LDMOS FET is designed for use in power amplifier applications in the 960 to 1215 MHz frequency band. Features include high gain and thermally-enhanced package with bolt-down flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTVA104501EH
Package H-33288-2



Features

- Broadband internal input and output matching
- High gain and efficiency
- Integrated ESD protection
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Excellent ruggedness
- Pb-free and RoHS compliant
- Capable of withstanding a 10:1 load mismatch (all phase angles) at 450 W peak under RF pulse, 128 µS, 10% duty cycle.

RF Characteristics

Pulsed RF Performance (tested in the test fixture)

V_{DD} = 50 V, I_{DQ} = 200 mA, P_{OUT} = 450 W (peak), f_1 = 960 MHz, f_2 = 1090 MHz, f_3 = 1215 MHz, RF pulse 128 µs, 10% duty cycle

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16.5	17.5	—	dB
Drain Efficiency	η_D	53	58	—	%
Gain Flatness	ΔG	—	0.85	1.8	dB
Return Loss	IRL	—	–9.5	–6	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Rev. 04, 2023-07-10

RF Characteristics

Typical RF Performance (not subject to production test, verified by design/characterization in the test fixture)
V_{DD} = 50 V, I_{DQ} = 200 mA, Input signal (t_r = 7.0 ns, t_f = 7.0 ns), 128 µs pulse width, 10% duty cycle, class AB test

Mode of Operation	f (MHz)	IRL (dB)	P_{1dB}			P_{3dB}			Max P_{droop} (pulse) @ P_{1dB}	$t_{r\,(ns)}$ @P_{1dB}	$t_{f\,(ns)}$ @P_{1dB}
			Gain (dB)	Eff (%)	P_{OUT} (W)	Gain (dB)	Eff (%)	P_{OUT} (W)			
128 µs, 10%	960	–7.5	18.0	56	460	16.0	53	490	0.15	5	<2
	1030	–13.0	18.5	59	470	16.5	60	540	0.15	5	<2
	1090	–8.0	17.8	61	510	15.8	61	590	0.20	5	<2
	1150	–15.0	18.1	59	540	16.1	60	620	0.20	5	<2
	1215	–9.0	18.3	56	460	16.3	53	510	0.20	5	<2

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 111 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.1	—	Ω
Operating Gate Voltage	V_{DS} = 50 V, I_{DQ} = 200 mA	V_{GS}	3.0	3.5	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

Maximum Ratings

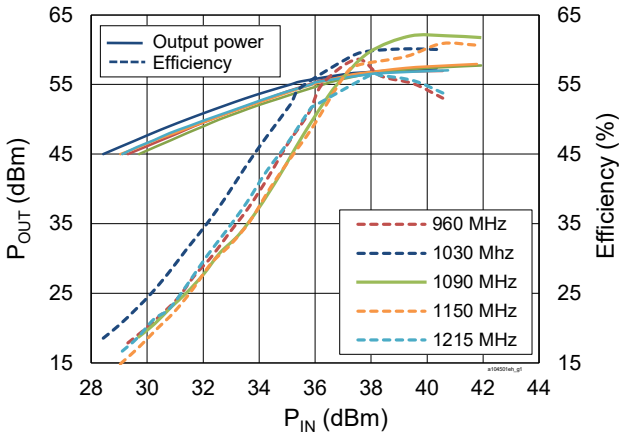
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	–6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance	$R_{\theta JC}$	0.25	°C/W
(T_{CASE} = 70°C, 430 W CW, f = 1090 MHZ, V_{DD} = 50 V, I_{DQ} = 200 mA)			

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTVA104501EH V1 R0	PTVA104501EH-V1-R0	H-33288-2	Tape & Reel, 50 pcs
PTVA104501EH V1 R250	PTVA104501EH-V1-R250	H-33288-2	Tape & Reel, 250 pcs

Typical RF Performance (data taken in production test fixture)

Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 200 mA, T_{CASE} = 25°C,
128 µs pulse width, 10% duty cycle



Power Sweep, Pulsed RF
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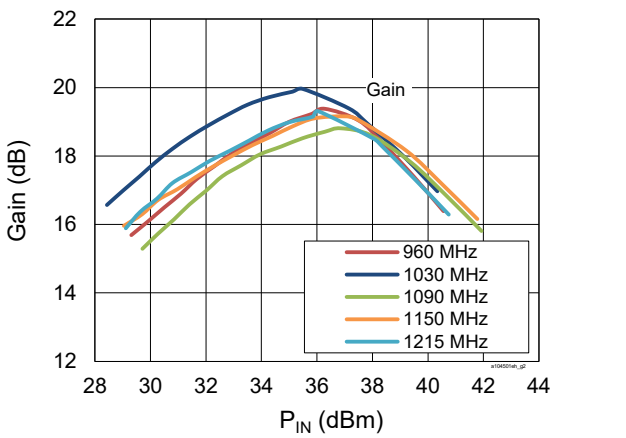
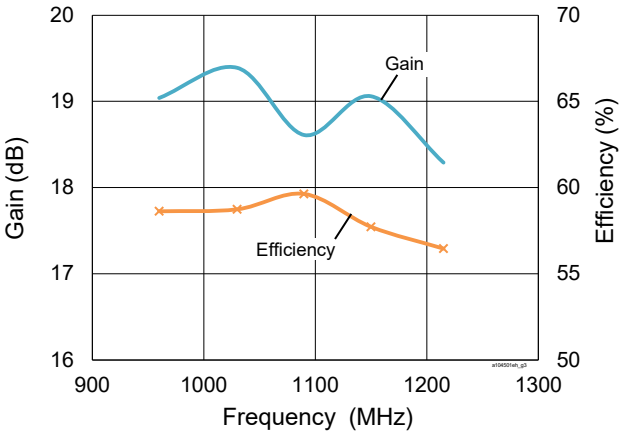


Pulsed RF Performance
V_{DD} = 50V, I_{DQ} = 200mA, P_{OUT}= 450W (peak),
128 µs pulse width, 10% duty cycle



Pulsed RF Performance
V_{DD} = 50V, I_{DQ} = 200mA, P_{OUT}= 450W (peak),
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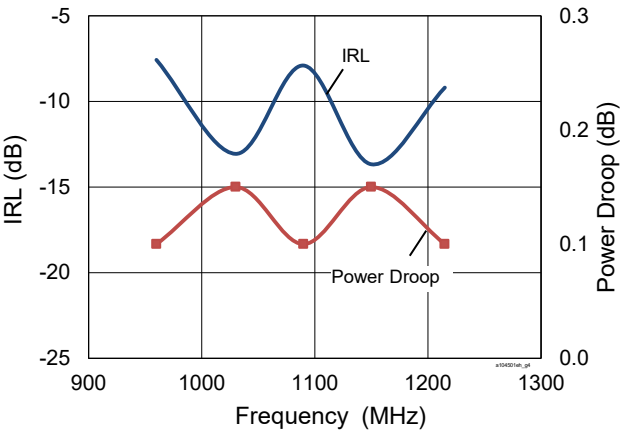
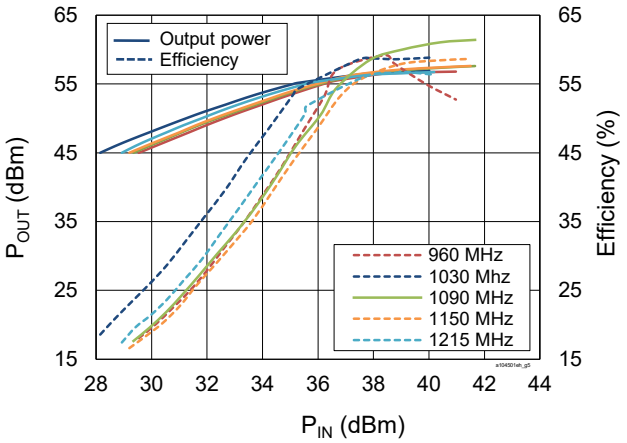
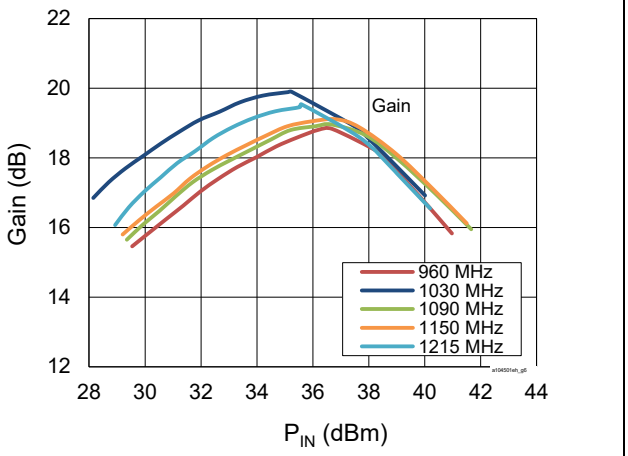


Typical RF Performance (cont.)

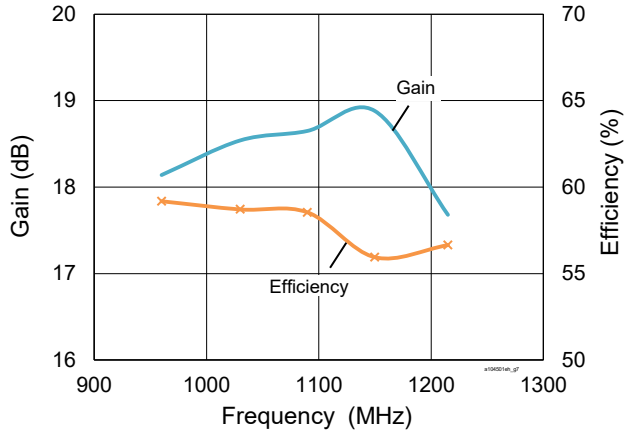
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 200 mA, T_{CASE} = 25°C,
P.W = 3.354mS, Burts = 7µS On, 6µS Off,
L.T = 22.7% duty cycle



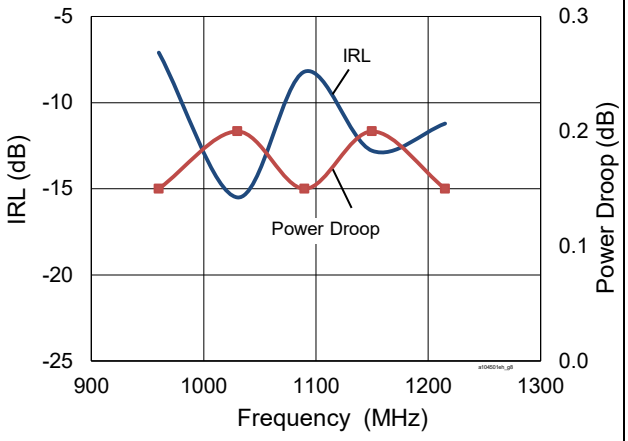
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 200 mA, T_{CASE} = 25°C
P.W = 3.354mS, Burts = 7µS On, 6µS Off,
L.T = 22.7% duty cycle



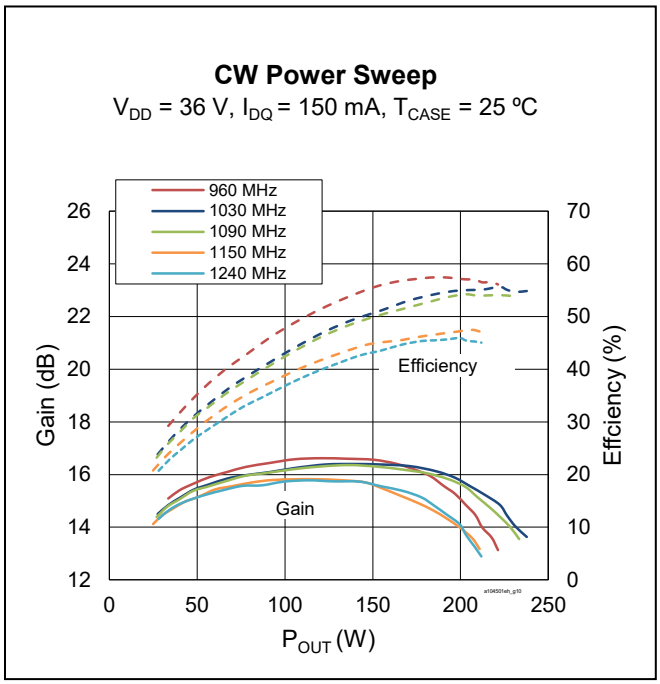
Pulsed RF Performance
V_{DD} = 50V, I_{DQ} = 200mA, P_{OUT} = 450W (peak),
P.W = 3.354mS, Burts = 7µS On, 6µS Off,
L.T = 22.7% duty cycle

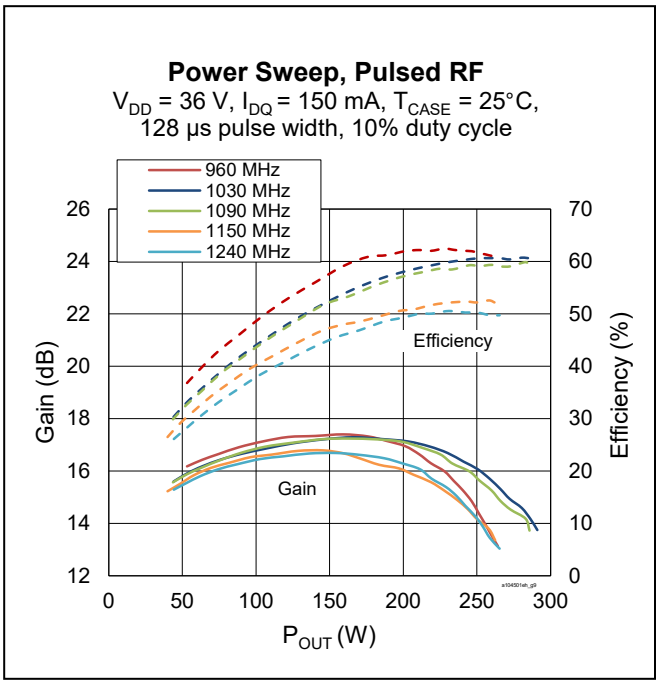


Pulsed RF Performance
V_{DD} = 50V, I_{DQ} = 200mA, P_{OUT} = 450W (peak),
P.W = 3.354mS, Burts = 7µS On, 6µS Off,
L.T = 22.7% duty cycle



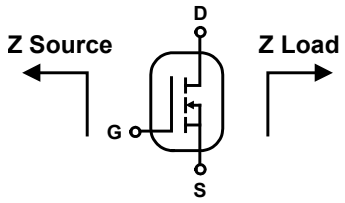
Typical RF Performance (cont.)





Broadband Circuit Impedance

Freq [MHz]	Z Source Ω		Z Load Ω	
	R	jX	R	jX
960	2.04	–0.30	0.79	–0.02
1030	1.71	–0.18	0.73	0.64
1090	1.45	0.09	0.95	1.09
1150	1.23	0.41	1.26	0.98
1215	1.07	0.77	0.71	0.93



Load Pull Performance

Load Pull at Max P_{OUT} Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 200 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
960	1.35 – j0.70	43.30	57.83	606.74	14.53	54.90	1.29 – j1.37
1030	0.99 – j0.78	42.14	57.62	578.10	15.48	50.96	1.02 – j1.43
1090	1.24 – j0.84	41.37	57.40	549.54	16.03	50.52	1.06 – j1.51
1215	1.56 – j0.99	39.24	56.92	492.04	17.68	48.12	1.13 – j1.66

Load Pull at Max G_T Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 200 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
960	1.35 – j0.70	40.10	55.70	371.54	15.60	58.76	2.15 – j2.60
1030	0.99 – j0.78	38.16	55.33	341.19	17.17	59.44	2.73 – j2.02
1090	1.24 – j0.84	36.05	54.14	259.42	18.09	56.31	3.55 – j0.42
1215	1.56 – j0.99	33.38	53.42	219.79	20.04	49.44	1.34 – j0.08

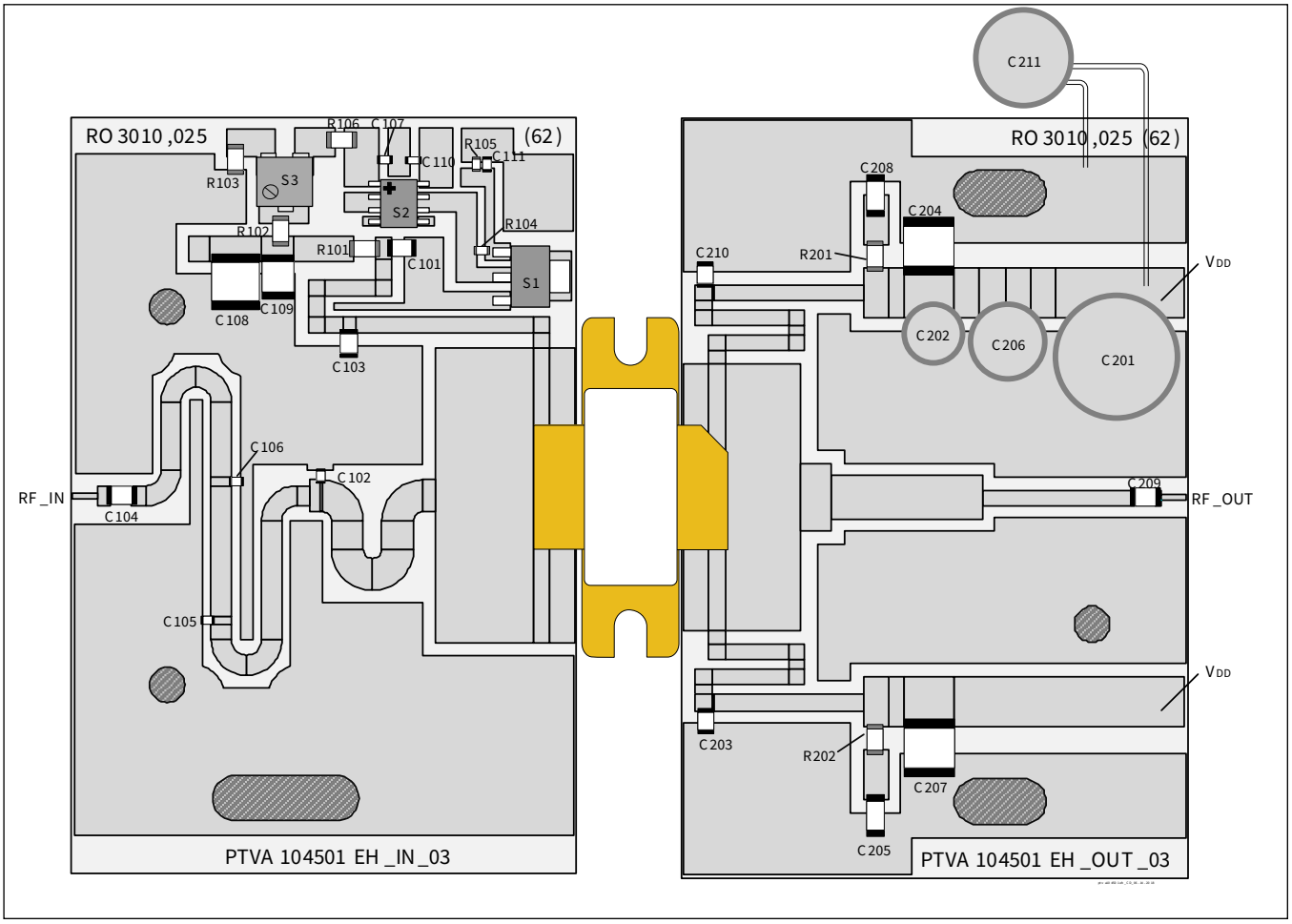
Load Pull at Max Efficiency Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 200 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
960	1.35 – j0.70	42.00	57.27	533.33	15.27	62.15	1.60 – j1.79
1030	0.99 – j0.78	39.44	56.34	430.53	16.90	61.78	2.27 – j1.50
1090	1.24 – j0.84	37.54	55.36	343.56	17.82	59.60	2.72 – j1.29
1215	1.56 – j0.99	36.19	55.58	361.41	19.39	56.63	1.65 – j0.92

Z Optimum – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 200 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
960	1.35 – j0.70	42.62	57.62	578.10	15.00	60.03	1.50 – j1.61
1030	0.99 – j0.78	39.82	56.62	459.20	16.80	61.39	2.03 – j1.45
1090	1.24 – j0.84	38.71	56.21	417.83	17.50	58.60	2.02 – j1.38
1215	1.56 – j0.99	37.79	56.47	443.61	18.68	53.43	1.29 – j1.37

Reference Circuit



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

Reference Circuit Assembly

DUT	PTVA104501EH
Test Fixture Part No.	LTN/PTVA104501EH V1
PCB	Rogers 3010, 0.635 mm [0.025"] thick, 2 oz. copper, $\varepsilon_r = 10.2$

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C103	Capacitor, 39 pF	ATC	100B 390
C102	Capacitor, 3.3 pF	ATC	800A 3R3
C104	Capacitor, 56 pF	ATC	100B 560
C105	Capacitor, 3.9 pF	ATC	800A 3R9
C106	Capacitor, 2.4 pF	ATC	800A 2R4
C107, C110, C111	Capacitor, 1000 pF	Panasonic Electronic Components	ECJ-1VB1H102K
C108	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C109	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
R101	Resistor, 20 Ω	Panasonic Electronic Components	ERJ-8GEYJ200V
R102	Resistor, 1k Ω	Panasonic Electronic Components	ERJ-8GEYJ102V
R103	Resistor, 2k Ω	Panasonic Electronic Components	ERJ-8GEYJ202V
R104	Resistor, 1.2k Ω	Panasonic Electronic Components	ERJ-3GEYJ122V
R105	Resistor, 1.3k Ω	Panasonic Electronic Components	ERJ-3GEYJ132V
R106	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
S1	Transistor	Infineon Technologies	BCP56
S2	Voltage Regulator	Texas Instruments	LM78L05ACM
S3	Potentiometer, 2k Ω	Bourns Inc.	3224W-1-202E
Output			
C201	Capacitor, 100 µF	Cornell Dubilier Electronics (CDE)	SK101M100ST
C202	Capacitor, 10 µF	Cornell Dubilier Electronics (CDE)	SEK100M100ST
C203, C210	Capacitor, 39 pF	ATC	100B 390
C204, C207	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C205, C208	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C206	Capacitor, 22 µF	Cornell Dubilier Electronics (CDE)	SEK220M100ST
C209	Capacitor, 56 pF	ATC	100B 560
C211	Capacitor, 6800 µF	Panasonic Electronic Components	ECO-S2AP682EA
R201, R202	Resistor, 5.6 Ω	Panasonic Electronic Components	ERJ-8RQJ5R6V

Package Outline Specifications

Package H-33288-2

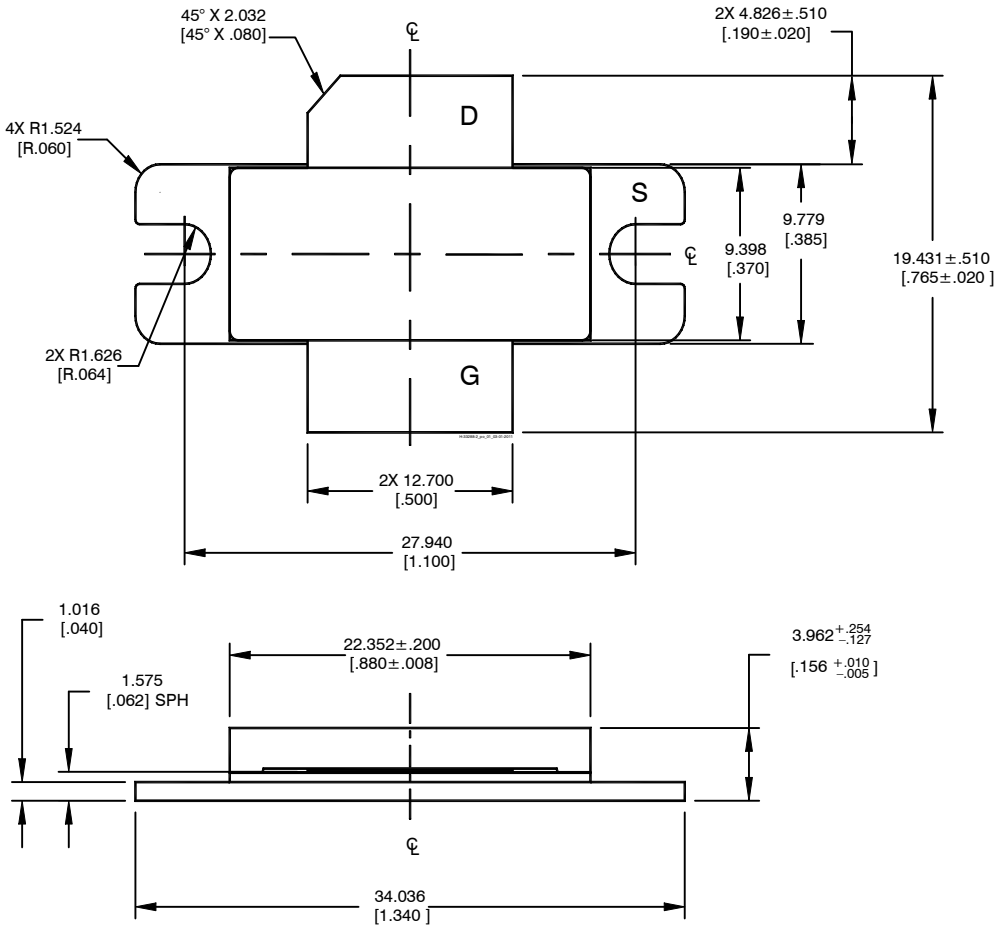


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D – drain; G – gate; S – source.
5. Lead thickness: 0.10 + 0.051/-0.025 mm [.004 +0.002/-0.001 inch].
6. Gold plating thickness: 0.25 micron [10 microinch] max.

Notes & Disclaimer

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