

PTVA092407NF

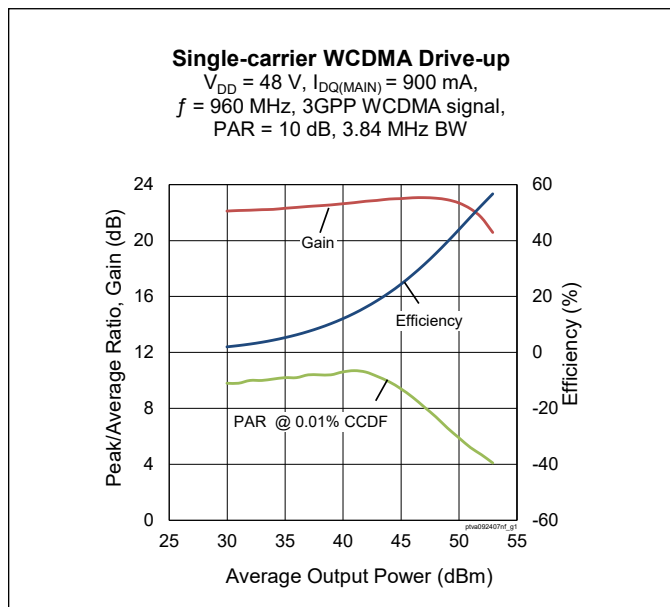
Thermally-Enhanced High Power RF LDMOS FET
240 W, 48 V, 869 – 960 MHz



Package Types: PG-HBSOF-4-2

Description

The PTVA092407NF is a 240-watt LDMOS FET manufactured with the 48-V LDMOS process. It is designed for use in multi-standard cellular power amplifier applications. It features a single ended design and input and output matching that allow for use from 869 MHz to 960 MHz. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input and output matching
- Typical CW performance, 960 MHz, 48 V, 10 μs pulse width, 10% duty cycle, single side
 - Output power at $P_{1dB} = 240\text{ W}$
 - Output power at $P_{3dB} = 287\text{ W}$
 - Gain = 20 dB
 - Efficiency = 62%
- Capable of handling 10:1 VSWR @ 48 V, 80 W CW output power
- Integrated ESD protection
- Human Body Model class 2 (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the production test fixture)

$V_{DD} = 48\text{ V}$, $I_{DQ} = 900\text{ mA}$, $P_{OUT} = 80\text{ W}$ avg, $f = 960\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|----------|------|------|-------|------|
| Linear Gain | G_{ps} | 21.3 | 22.5 | — | dB |
| Drain Efficiency | η_D | 38 | 40 | — | % |
| Adjacent Channel Power Ratio | ACPR | — | -30 | -28.5 | dBc |
| Output PAR @ 0.01% CCDF | OPAR | 5.7 | 6.2 | — | dB |

Note:

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



DC Characteristics

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------------|---------------|------|------|------|---------------|--|
| Drain-Source Breakdown Voltage | $V_{BR(DSS)}$ | 105 | — | — | V | $V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$ |
| Drain Leakage Current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$ |
| | | — | — | 10 | | $V_{DS} = 105\text{ V}, V_{GS} = 0\text{ V}$ |
| Gate Leakage Current | I_{GSS} | — | — | 1 | | $V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$ |
| On-State Resistance | $R_{DS(on)}$ | — | 0.13 | — | Ω | $V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$ |
| Operating Gate Voltage | V_{GS} | 3.3 | 3.7 | 4.1 | V | $V_{DS} = 48\text{ V}, I_{DQ} = 900\text{ mA}$ |

Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---------------------------|-----------|-------------|--------------------|
| Drain-source Voltage | V_{DSS} | 105 | V |
| Gate-source Voltage | V_{GS} | -6 to +12 | |
| Operating Voltage | V_{DD} | 0 to +55 | |
| Junction Temperature | T_J | 225 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{STG} | -65 to +150 | |

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

| Parameter | Symbol | Value | Unit | Conditions |
|---------------------------|-----------------|-------|-----------------------------|--|
| Thermal Resistance (Main) | $R_{\theta JC}$ | 0.29 | $^{\circ}\text{C}/\text{W}$ | $T_{CASE} = 70^{\circ}\text{C}, 240\text{ W CW}$ |

Moisture Sensitivity Level

| Level | Test Signal | Package Temperature | Unit |
|-------|---------------------|---------------------|--------------------|
| 3 | IPC/JEDEC J-STD-020 | 260 | $^{\circ}\text{C}$ |

Ordering Information

| Type and Version | Order Code | Package Description | Shipping |
|--------------------|--------------------|-------------------------------|----------------------|
| PTVA092407NF V2 R5 | PTVA092407NF-V2-R5 | PG-HBSOF-4-2, plastic package | Tape & Reel, 500 pcs |

Typical RF Performance (data taken in production test fixture)

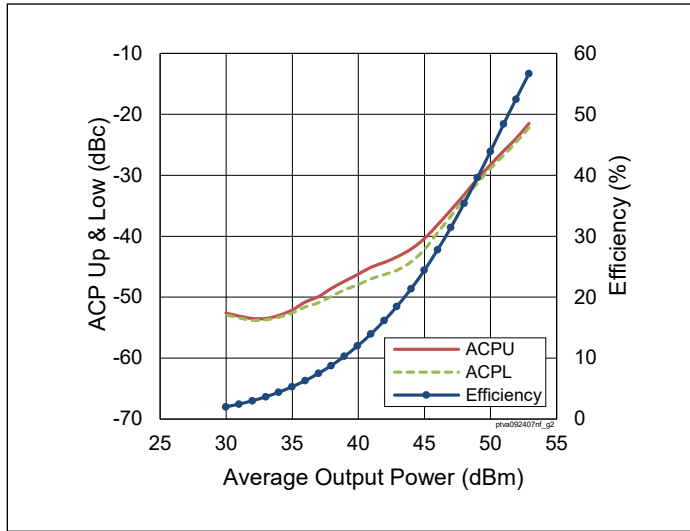


Figure 1. Single-carrier WCDMA Drive-up

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 900\text{ mA}$, $f = 960\text{ MHz}$
 3GPP WCDMA signal, PAR = 10 dB,
 BW = 3.84 MHz

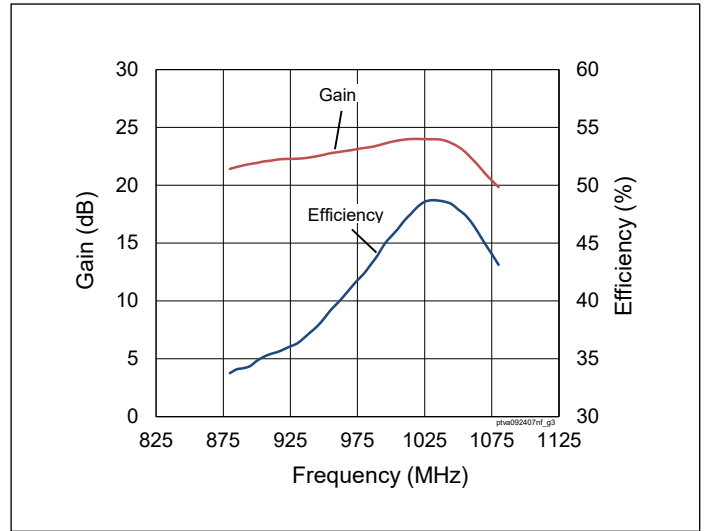


Figure 2. Single-carrier WCDMA Broadband Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 900\text{ mA}$,
 $P_{OUT} = 49\text{ dBm}$, 3GPP WCDMA signal,
 PAR = 10 dB

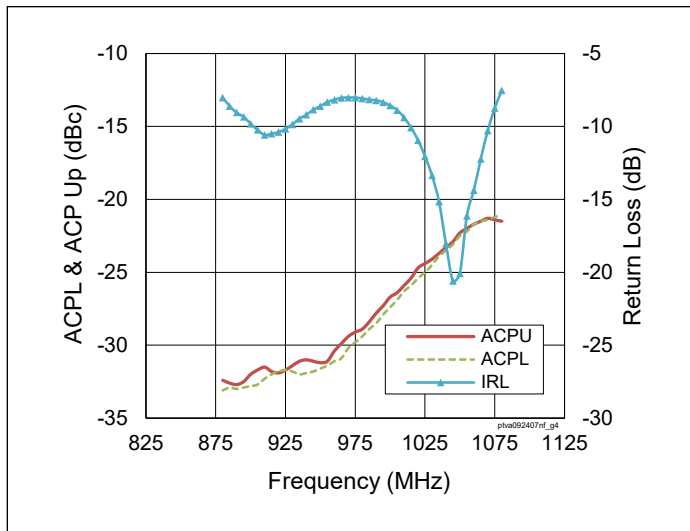


Figure 3. Single-carrier WCDMA Broadband Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 900\text{ mA}$,
 $P_{OUT} = 49\text{ dBm}$, 3GPP WCDMA signal,
 PAR = 10 dB

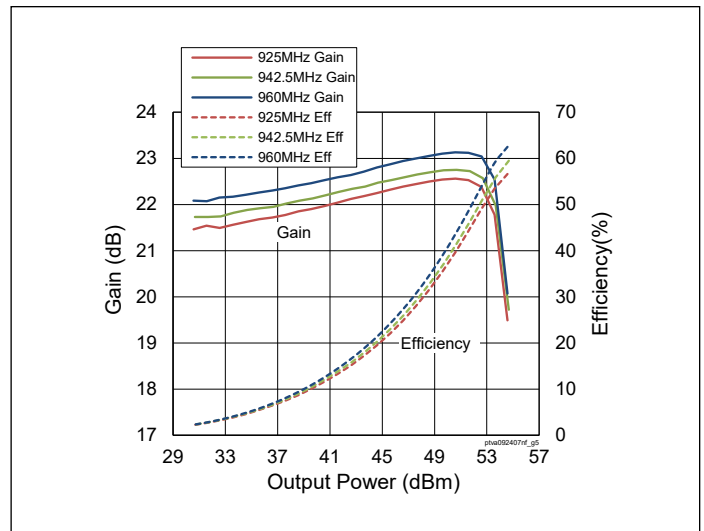


Figure 4. CW Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 900\text{ mA}$

Typical RF Performance (cont.)

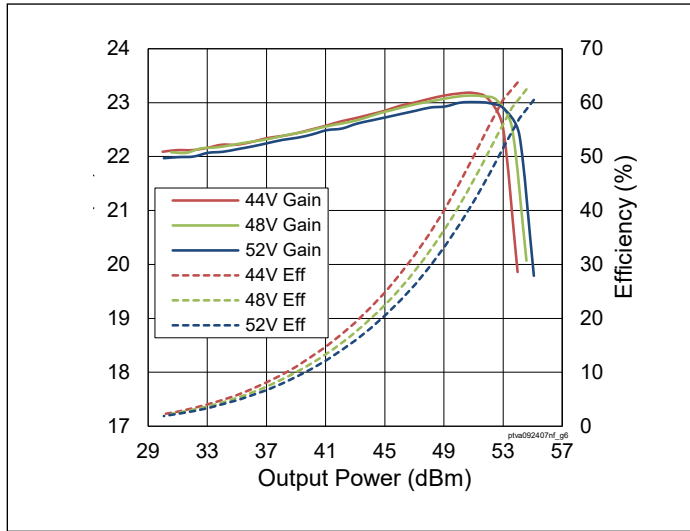


Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)} = 900 \text{ mA}$, $f = 960 \text{ MHz}$

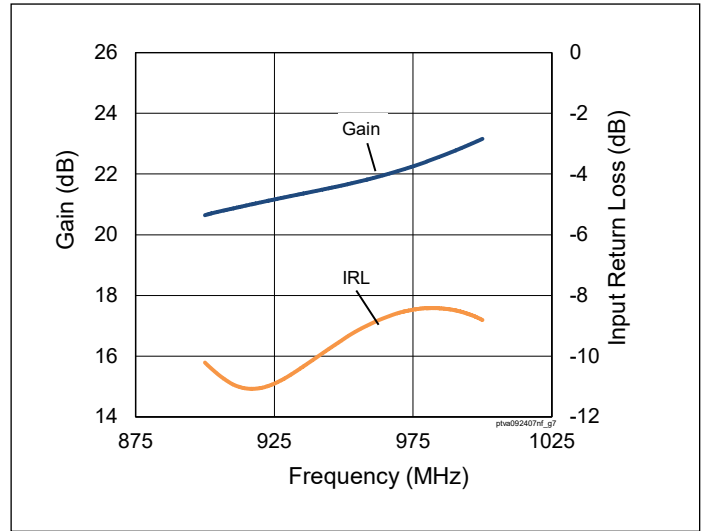


Figure 6. CW Performance Small Signal Gain & Input Return Loss

$V_{DD} = 48 \text{ V}$, $I_{DQ(MAIN)} = 900 \text{ mA}$

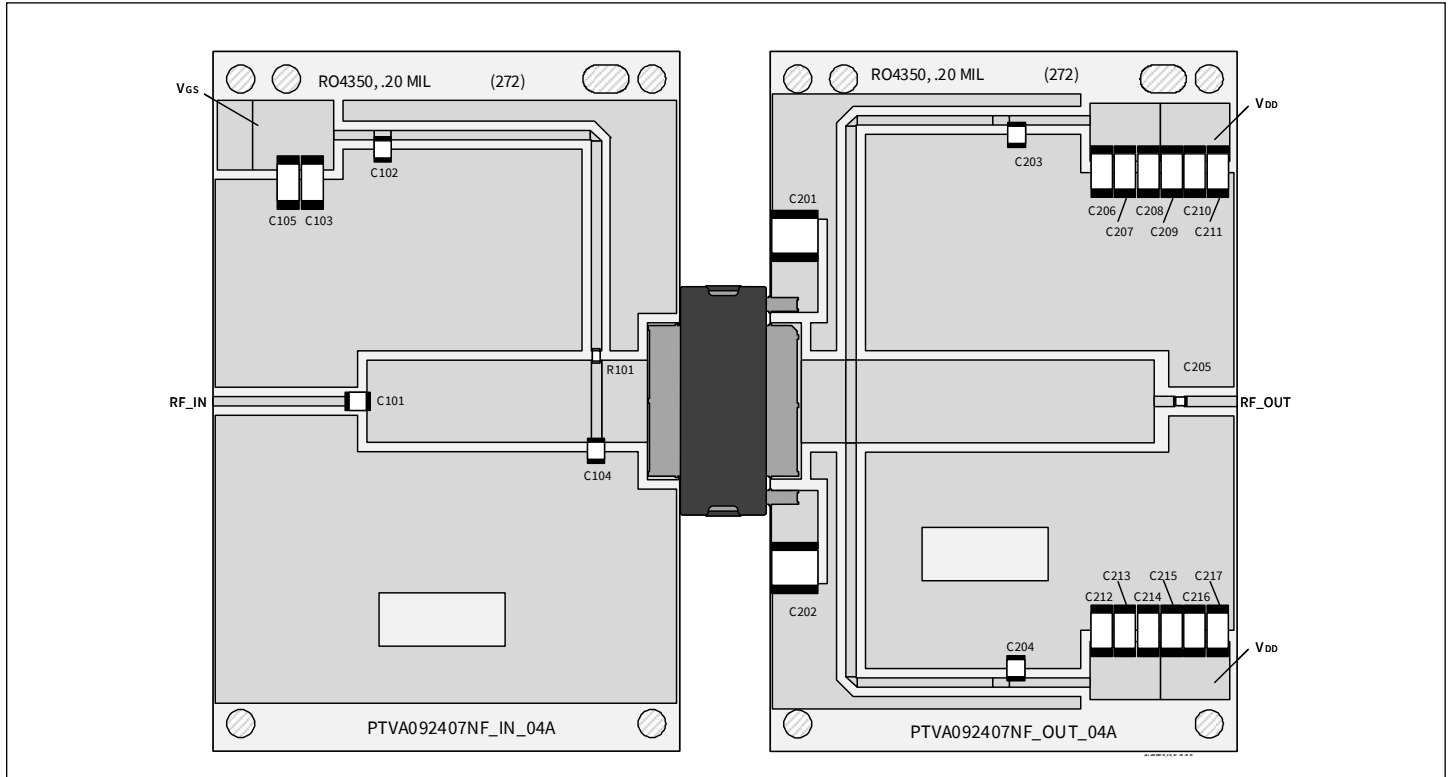
Load Pull Performance

Each Side Load Pull Performance – Pulsed CW signal: 10 μs , 10% duty cycle, 48 V, $I_{DQ} = 480 \text{ mA}$

| | | P_{1dB} | | | | | | | | | |
|------------|----------------|------------------|-----------|------------------------|----------------------|---------------|----------------------|-----------|------------------------|----------------------|---------------|
| | | Max Output Power | | | | | Max Drain Efficiency | | | | |
| Freq [MHz] | $Z_s [\Omega]$ | $Z_l [\Omega]$ | Gain [dB] | $P_{1dB} [\text{dBm}]$ | $P_{1dB} [\text{W}]$ | $\eta_D [\%]$ | $Z_l [\Omega]$ | Gain [dB] | $P_{1dB} [\text{dBm}]$ | $P_{1dB} [\text{W}]$ | $\eta_D [\%]$ |
| 869 | 0.69-j3.06 | 1.52-j0.62 | 20.83 | 55.70 | 371.54 | 57.6 | 2.72+j1.29 | 23.07 | 53.51 | 224.39 | 71.3 |
| 925 | 1.29-j3.32 | 1.46-j0.56 | 21.35 | 55.55 | 354.81 | 60.4 | 2.24+j1.18 | 23.44 | 53.27 | 212.32 | 70.5 |
| 960 | 2.45-j3.23 | 1.31-j0.55 | 21.52 | 55.51 | 355.63 | 59.9 | 2.01+j0.7 | 23.39 | 53.66 | 232.27 | 71.7 |

| | | P_{3dB} | | | | | | | | | |
|------------|----------------|------------------|-----------|------------------------|----------------------|---------------|----------------------|-----------|------------------------|----------------------|---------------|
| | | Max Output Power | | | | | Max Drain Efficiency | | | | |
| Freq [MHz] | $Z_s [\Omega]$ | $Z_l [\Omega]$ | Gain [dB] | $P_{3dB} [\text{dBm}]$ | $P_{3dB} [\text{W}]$ | $\eta_D [\%]$ | $Z_l [\Omega]$ | Gain [dB] | $P_{3dB} [\text{dBm}]$ | $P_{3dB} [\text{W}]$ | $\eta_D [\%]$ |
| 869 | 0.69-j3.06 | 1.55-j0.78 | 18.81 | 56.40 | 436.52 | 60.0 | 2.81+j1.47 | 21.17 | 53.84 | 242.1 | 71.9 |
| 925 | 1.29-j3.32 | 1.58-j0.7 | 19.43 | 56.30 | 426.58 | 63.2 | 2.27+j1.17 | 21.46 | 53.90 | 245.47 | 72.6 |
| 960 | 2.45-j3.23 | 1.41-j0.54 | 19.72 | 56.17 | 414 | 64.7 | 1.76+j0.92 | 21.5 | 53.87 | 243.78 | 72.7 |

Evaluation Board, 869 – 960 MHz

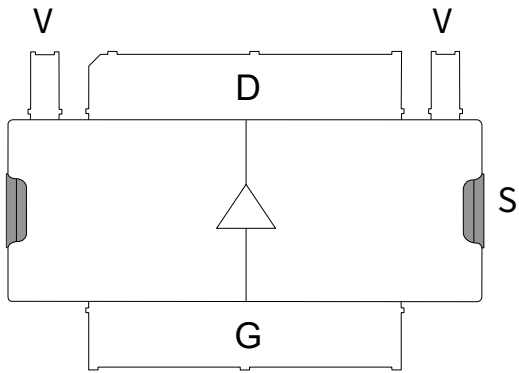


Reference circuit assembly diagram (not to scale)

| | |
|------------------------------|---|
| Evaluation Board Part Number | LTN/PTVA092407NF-V2 |
| PCB Information | Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$, $f = 869 - 960$ MHz |

Components Information

| Component | Description | Manufacturer | P/N |
|--|------------------------------|---------------------------------|---------------------|
| Input | | | |
| C101 | Capacitor, 47 pF | ATC | ATC100B470KW500XT |
| C102 | Capacitor, 75 pF | ATC | ATC100B750KW500XT |
| C103, C105 | Capacitor, 10 μ F, 100 V | TDK Corporation | C5750X7S2A106M230KB |
| C104 | Capacitor, 3.6 pF | ATC | ATC100B3R6CW500XT |
| R101 | Resistor, 10 ohms | Panasonic Electronic Components | ERJ-8GEYJ100V |
| Output | | | |
| C201, C202, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217 | Capacitor, 10 μ F, 100 V | TDK Corporation | C5750X7S2A106M230KB |
| C203, C204 | Capacitor, 75 pF | ATC | ATC100B750KW500XT |
| C205 | Capacitor, 10 pF | ATC | ATC100A101JW150XT |

Pinout Diagram (top view)


| Pin | Description |
|-----|---|
| D | Drain |
| G | Gate |
| S | Source (flange) |
| V | Drain video decoupling (use only for decoupling), not for DC bias |

Package Outline Specifications – Package PG-HBSOF-4-2

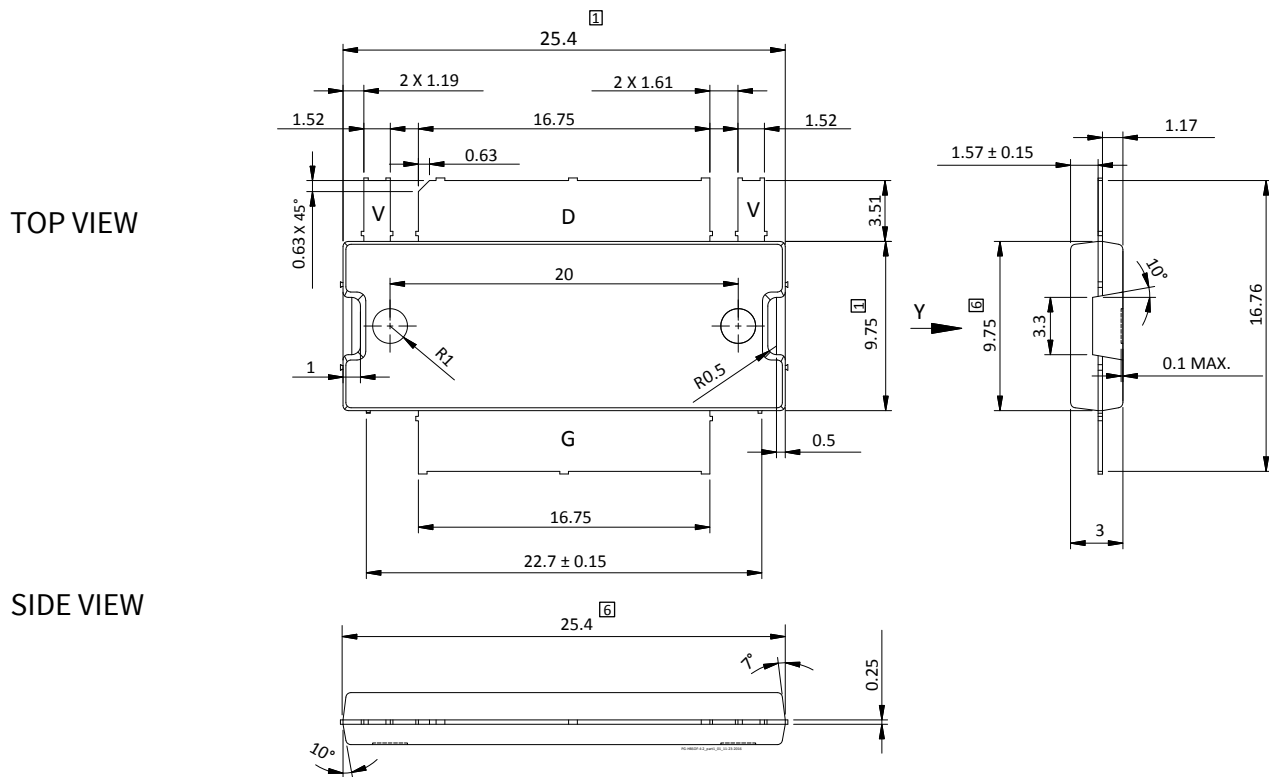


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Does not include mold/dam bar/metal protrusion.
7. Exposed metal surface tin-plated, may not be covered by mold compound.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces are tin-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D – drain; G – gate; S – source; V – drain video decoupling (use only for decoupling), not for DC bias

Package Outline Specifications (cont.) – Package PG-HBSOF-4-2

BOTTOM VIEW

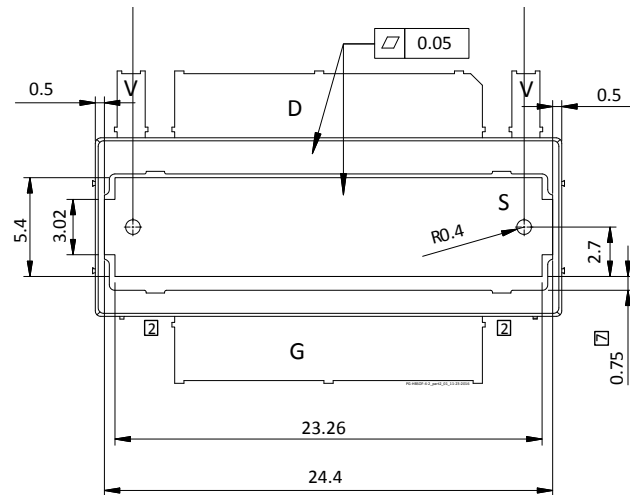


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