

# PTRA095908NB

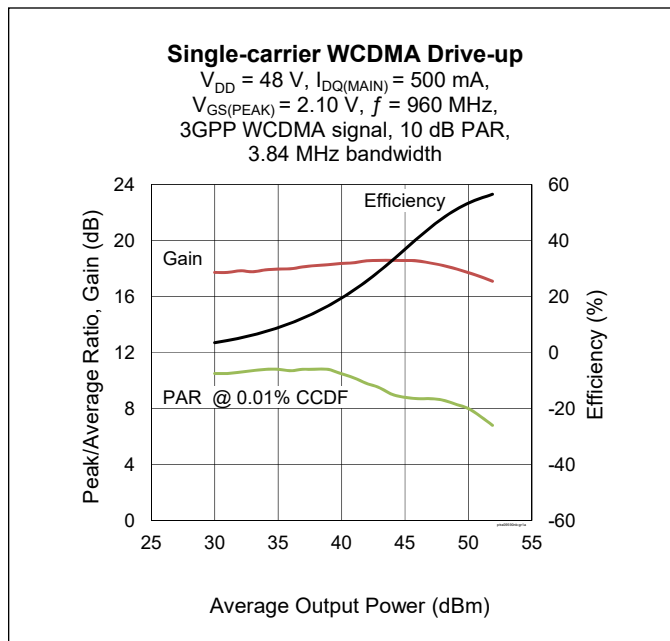
Thermally-Enhanced High Power RF LDMOS FET  
520 W, 48 V, 925 – 960 MHz



Package Types: PG-HB2SOF-6-1

## Description

The PTRA095908NB is a 520-watt ( $P_{3dB}$ ) LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 925 to 960 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced plastic overmold package with earless flange.



## Features

- Broadband internal input and output matching
- Asymmetric Doherty design
  - Main:  $P_{1dB} = 250\text{ W Typ}$
  - Peak:  $P_{1dB} = 400\text{ W Typ}$
- Typical pulsed CW performance, 942 MHz, 48 V, Doherty configuration, 10  $\mu\text{s}$ , 10% duty cycle
  - Output power at  $P_{1dB} = 160\text{ W}$
  - Output power at  $P_{3dB} = 520\text{ W}$
  - Efficiency = 58% ( $P_{OUT} = 109\text{ W}$ )
  - Gain = 19 dB ( $P_{OUT} = 109\text{ W}$ )
- Capable of handling 10:1 VSWR @ 48 V, 109 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

## RF Characteristics

### Single-carrier WCDMA Specifications (tested in the Doherty test fixture)

$V_{DD} = 48\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$ ,  $P_{OUT} = 109\text{ W avg}$ ,  $V_{GS(PEAK)} = (V_{GS} @ I_{DQ} = 600\text{ mA}) - 1.4\text{ V}$ ,  $f = 960\text{ MHz}$ , 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	$G_{ps}$	16.8	17.5	—	dB
Drain Efficiency	$\eta_D$	49.5	52	—	%
Adjacent Channel Power Ratio	ACPR	—	-31	-27.5	dBc
Output PAR @ 0.01% probability on CCDF	OPAR	6.6	7.2	—	dB

Note:

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



## DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	105	—	—	V	$V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$
Drain Leakage Current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$
		—	—	10		$V_{DS} = 105\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	$I_{GSS}$	—	—	1		$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$
On-State Resistance (main)	$R_{DS(on)}$	—	0.09	—	$\Omega$	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$
On-State Resistance (peak)		—	0.05	—		
Operating Gate Voltage (main)	$V_{GS}$	3.3	3.6	3.9	V	$V_{DS} = 48\text{ V}, I_{DQ} = 500\text{ mA}$
Operating Gate Voltage (peak)		1.85	2.2	2.45		$V_{DS} = 48\text{ V}, I_{DQ} = 0\text{ mA}$

## Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	$V_{DSS}$	105	V
Gate-source Voltage	$V_{GS}$	-6 to +12	
Operating Voltage	$V_{DD}$	0 to +55	
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range ( $V_{DD}$ ) specified above.

2. Parameters values can be affected by end application and product usage. Values may change over time.

## Thermal Characteristics

Characteristic	Symbol	Value	Unit	Conditions
Thermal Resistance (Main)	$R_{\theta JC}$	0.58	$^{\circ}\text{C/W}$	$T_{CASE} = 70^{\circ}\text{C}, 48\text{ V}, 942\text{ MHz}; 85\text{ W CW}, I_{DQ} = 500\text{ mA}$
Thermal Resistance (Peak)		0.21		$T_{CASE} = 70^{\circ}\text{C}, 48\text{ V}, 942\text{ MHz}; 125\text{ W CW}, V_{GS(PEAK)} = 2.1\text{ V}$

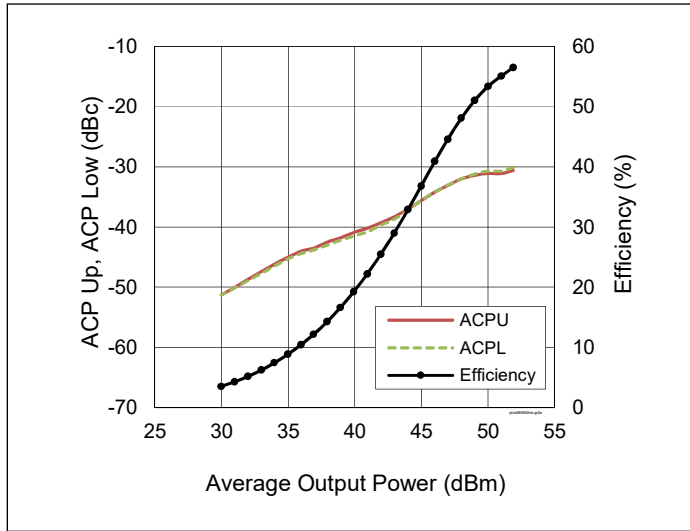
## Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	$^{\circ}\text{C}$

## Ordering Information

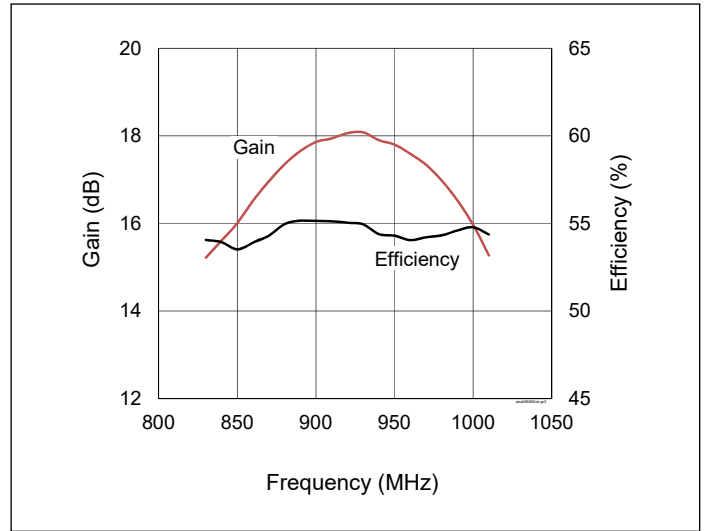
Type and Version	Order Code	Package and Description	Shipping
PTRA095908NB V1 R2	PTRA095908NB-V1-R2	PG-HB2SOF-6-1	Tape & Reel, 250 pcs

**Typical Performance** (data taken in the test fixture)



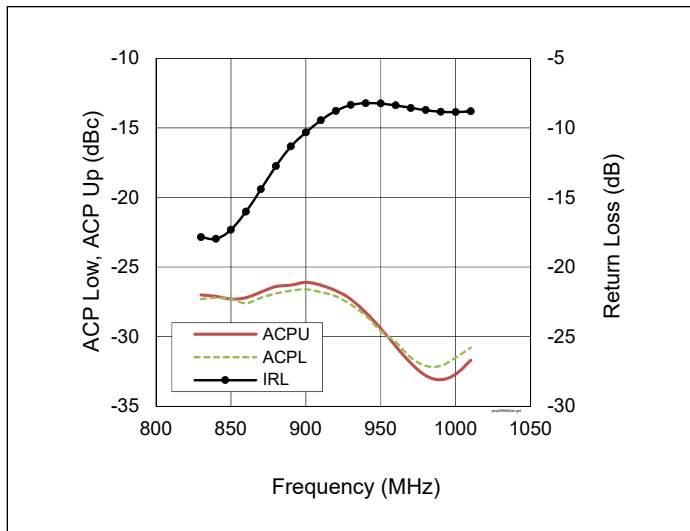
**Figure 1.** Single-carrier WCDMA Drive-up

$V_{DD} = 48\text{ V}$ ,  $I_{DQ(MAIN)} = 500\text{ mA}$ ,  
 $V_{GS(PEAK)} = 2.10\text{ V}$ ,  $f = 960\text{ MHz}$ ,  
 3GPP WCDMA signal, 10 dB PAR,  
 3.84 MHz bandwidth



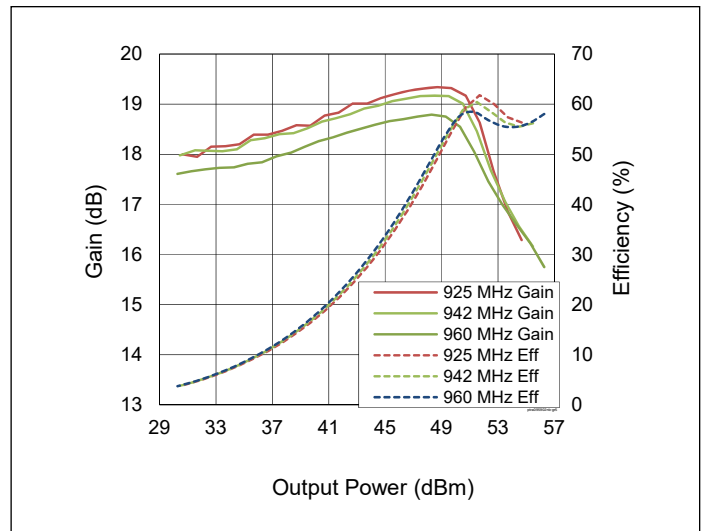
**Figure 2.** Single-carrier WCDMA Broadband

$V_{DD} = 48\text{ V}$ ,  $I_{DQ(MAIN)} = 500\text{ mA}$ ,  
 $V_{GS(PEAK)} = 2.10\text{ V}$ ,  $P_{OUT} = 50.4\text{ dBm}$ ,  
 3GPP WCDMA signal, 10 dB PAR,  
 3.84 MHz bandwidth



**Figure 3.** Single-carrier WCDMA Broadband

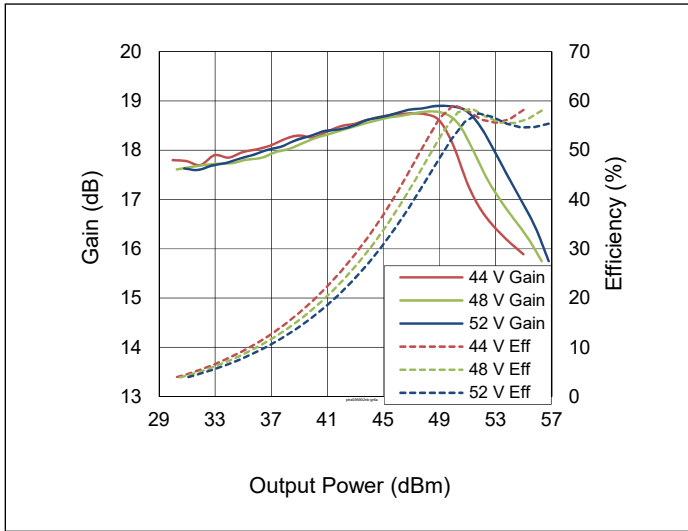
$V_{DD} = 48\text{ V}$ ,  $I_{DQ(MAIN)} = 500\text{ mA}$ ,  
 $V_{GS(PEAK)} = 2.10\text{ V}$ ,  $P_{OUT} = 50.4\text{ dBm}$ ,  
 3GPP WCDMA signal, 10 dB PAR,  
 3.84 MHz bandwidth



**Figure 4.** CW Performance

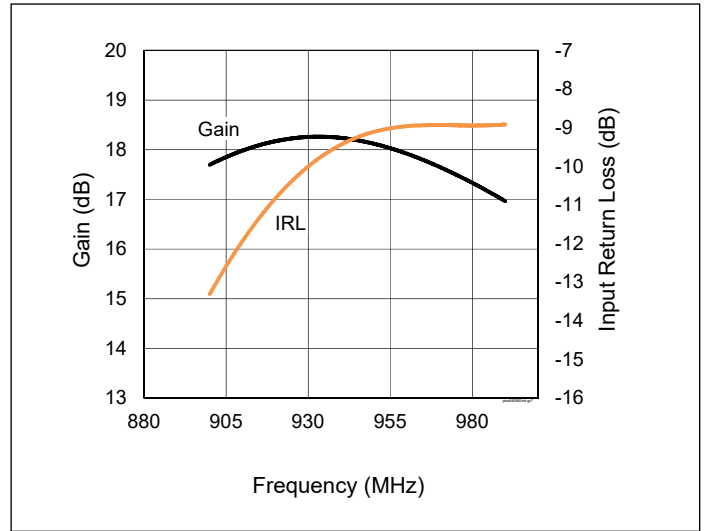
$V_{DD} = 48\text{ V}$ ,  $I_{DQ(MAIN)} = 500\text{ mA}$ ,  
 $V_{GS(PEAK)} = 2.10\text{ V}$

**Typical Performance** (cont.)



**Figure 5.** CW Performance at various  $V_{DD}$

$I_{DQ(MAIN)} = 500 \text{ mA}$ ,  $V_{GS(PEAK)} = 2.10 \text{ V}$ ,  
 $f = 960 \text{ MHz}$



**Figure 6.** CW Performance Small Signal

$V_{DD} = 48 \text{ V}$ ,  $I_{DQ(MAIN)} = 500 \text{ mA}$ ,  
 $V_{GS(PEAK)} = 2.10 \text{ V}$

See next page for Load Pull Performance

## Load Pull Performance

**Main Side Load Pull Performance** – Pulsed CW signal: 100  $\mu$ sec, 10% duty cycle,  $V_{DD} = 48$  V,  $I_{DQ} = 500$  mA, class AB

		$P_{1dB}$									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	$Z_s$ [ $\Omega$ ]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{1dB}$ [dBm]	$P_{1dB}$ [W]	$\eta_D$ [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{1dB}$ [dBm]	$P_{1dB}$ [W]	$\eta_D$ [%]
925	1.5 – j5.8	1.54 – j0.53	20.75	53.92	246	58.9	3.17 + j0.99	23.15	51.87	153	69.7
960	1.9 – j6.9	1.67 – j0.80	20.90	54.04	253	61.7	3.05 + j0.42	22.36	52.50	177	70.8

		$P_{3dB}$									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	$Z_s$ [ $\Omega$ ]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{3dB}$ [dBm]	$P_{3dB}$ [W]	$\eta_D$ [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{3dB}$ [dBm]	$P_{3dB}$ [W]	$\eta_D$ [%]
925	1.5 – j5.8	1.80 – j0.94	19.0	54.85	305	64.2	2.36 - j0.14	19.9	54.12	258	71.5
960	1.9 – j6.9	1.65 – j1.33	18.6	54.81	302	59.8	3.05 + j0.42	20.3	53.16	207	72.5

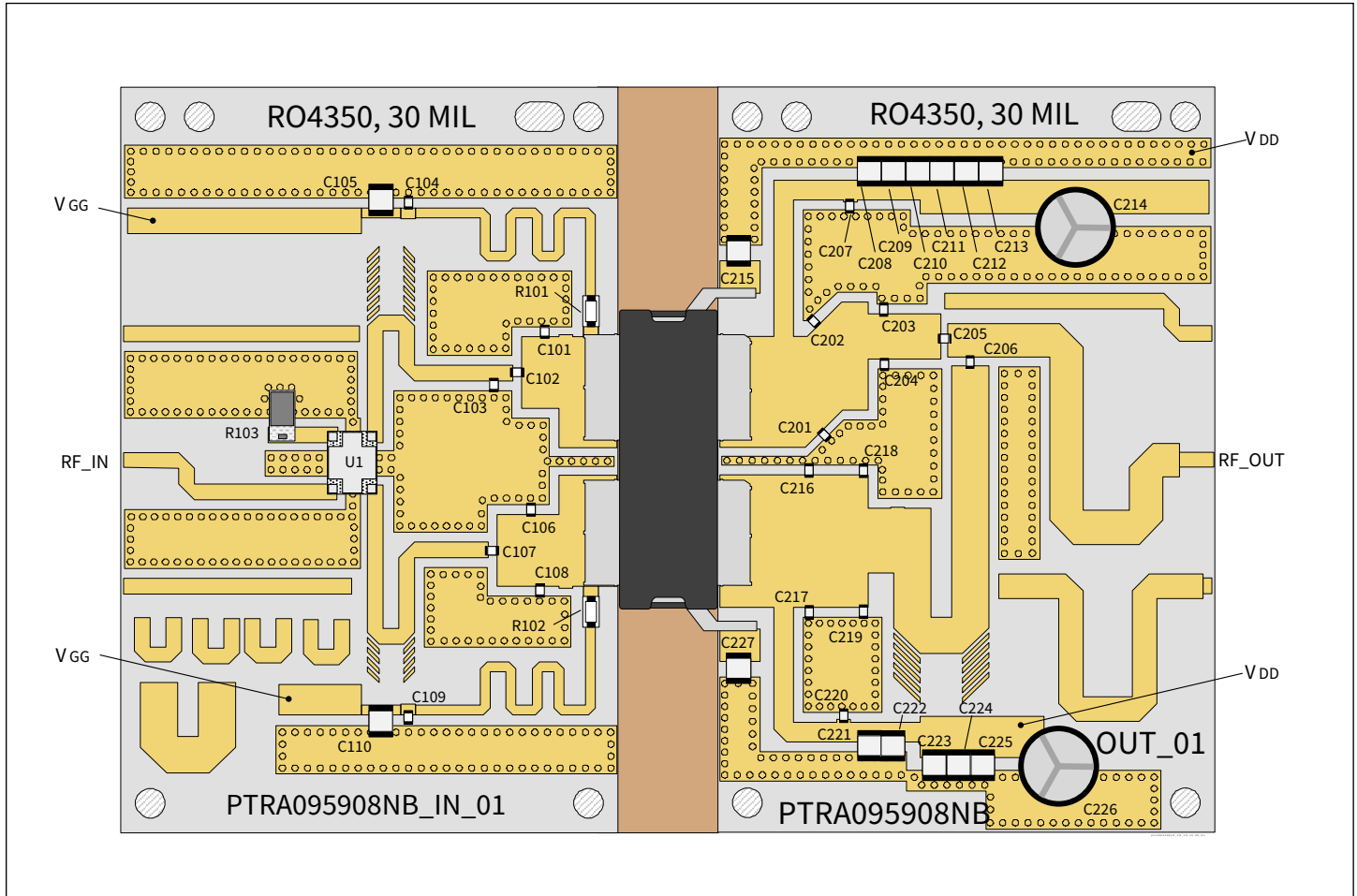
**Peak Side Load Pull Performance** – Pulsed CW signal: 100  $\mu$ sec, 10% duty cycle,  $V_{DD} = 48$  V,  $V_{GS(PEAK)} = 3$  V, class B

		$P_{1dB}$									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	$Z_s$ [ $\Omega$ ]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{1dB}$ [dBm]	$P_{1dB}$ [W]	$\eta_D$ [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{1dB}$ [dBm]	$P_{1dB}$ [W]	$\eta_D$ [%]
925	2.6 – j7.0	0.75 – j0.40	19.8	56.48	444	60.0	1.29 + j0.52	20.85	54.10	257	69.0
960	6.2 – j9.4	0.76 – j0.64	18.6	56.41	437	56.9	1.28 + j0.25	19.60	54.25	266	67.8

		$P_{3dB}$									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	$Z_s$ [ $\Omega$ ]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{3dB}$ [dBm]	$P_{3dB}$ [W]	$\eta_D$ [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{3dB}$ [dBm]	$P_{3dB}$ [W]	$\eta_D$ [%]
925	2.6 – j7.0	0.73 – j0.39	17.83	57.22	527	62.2	1.28 + j0.52	18.85	54.73	297.2	69.5
960	6.2 – j9.4	0.75 – j0.65	16.60	57.08	510	57.9	1.28 + j0.12	17.45	55.79	379.3	67.5

**Evaluation Board, 925 – 960 MHz**

Evaluation Board Part Number	LTA/PTRA095908NB-V1
PCB Information	Rogers 4350, 0.762mm [0.030"] thick, 2 oz. copper, $\epsilon_r = 3.66$

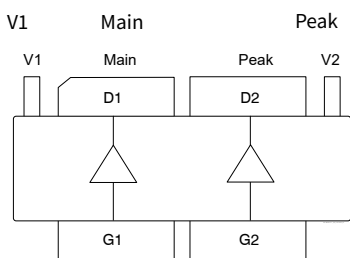


Reference circuit assembly diagram (not to scale)

## Components Information

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101	Capacitor, 8.2 pF	ATC	ATC600F8R2BT250XT
C102	Capacitor, 22 pF	ATC	ATC600F220JT250XT
C103	Capacitor, 2.0 pF	ATC	ATC600F2R0BT250XT
C104, C107, C109	Capacitor, 68 pF	ATC	ATC600F680JT250XT
C105, C110	Capacitor, 10 $\mu$ F, 100 V	Murata Electronics	GRM32EC72A106KE05L
C106	Capacitor, 4.7 pF	ATC	ATC600F4R7BT250XT
C108	Capacitor, 3.3 pF	ATC	ATC600F3R3BT250XT
R101, R102	Resistor, 6.2 ohms	Panasonic Electronic Components	ERJ-8GEYJ6R2V
R103	Resistor, 50 ohms	Anaren	C16A50Z4
U1	Hybrid Coupler	Anaren	X3C09P1-03S
<b>Output</b>			
C201	Capacitor, 2.7 pF	ATC	ATC600F2R7BT250XT
C202	Capacitor, 5.6 pF	ATC	ATC600F5R6BT250XT
C203	Capacitor, 3.3 pF	ATC	ATC600F3R3BT250XT
C204	Capacitor, 2.2 pF	ATC	ATC600F2R2BT250XT
C205	Capacitor, 12 pF	ATC	ATC600F120JT250XT
C206, C207, C220	Capacitor, 68 pF	ATC	ATC600F680JT250XT
C208, C209, C210, C211, C212, C213, C215, C221, C222, C223, C224, C225, C227	Capacitor, 10 $\mu$ F, 100 V	Murata Electronics	GRM32EC72A106KE05L
C214, C226	Capacitor, 100 $\mu$ F, 63 V	Panasonic Electronic Components	EEE-FK1J101P
C216, C218	Capacitor, 7.5 pF	ATC	ATC600F7R5BT250XT
C217	Capacitor, 6.8 pF	ATC	ATC600F6R8BT250XT
C219	Capacitor, 0.5 pF	ATC	ATC600F0R5BT250XT

## Pinout Diagram (top view)

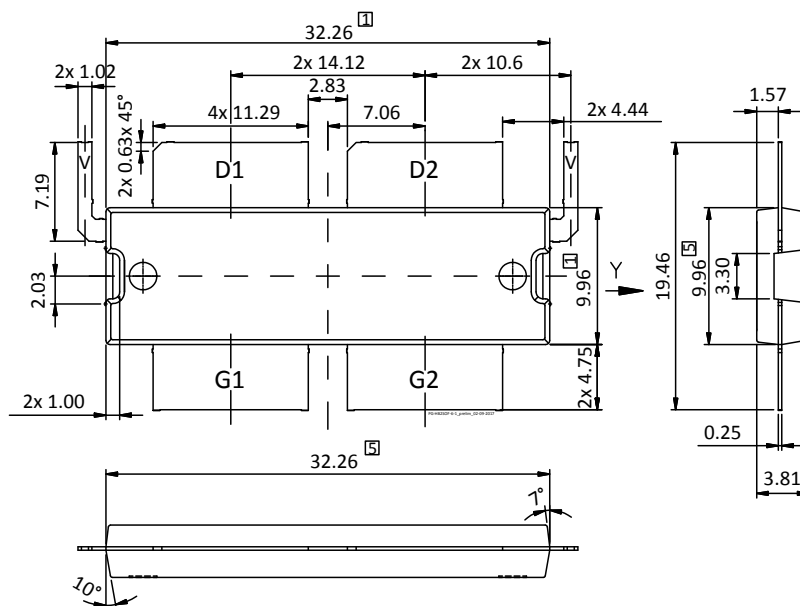


Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1, V2	Drain video decoupling, no DC Bias

Lead connections for PTRA095908NB

## Package Outline Specifications – Package PG-HB2SOF-6-1

Top and Side View



Bottom View

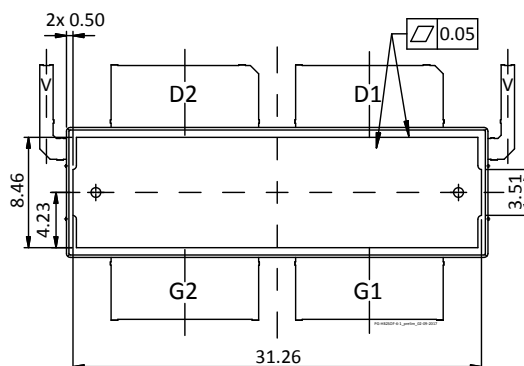


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max.
3. Interpret dimensions and tolerances per ISO 8015.
4. Dimensions are mm.
5. Does not include mold/dam bar and metal protrusion.
6. All tolerances  $\pm 0.1$  mm unless specified otherwise.
7. All metal surfaces tin pre-plated, except area of cut.
8. Lead thickness: 0.25 mm.
9. Pins: D1, D2 – drain; G1, G2 – gate; S – source;  
V – drain video decoupling, no DC bias



## Notes & Disclaimer

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