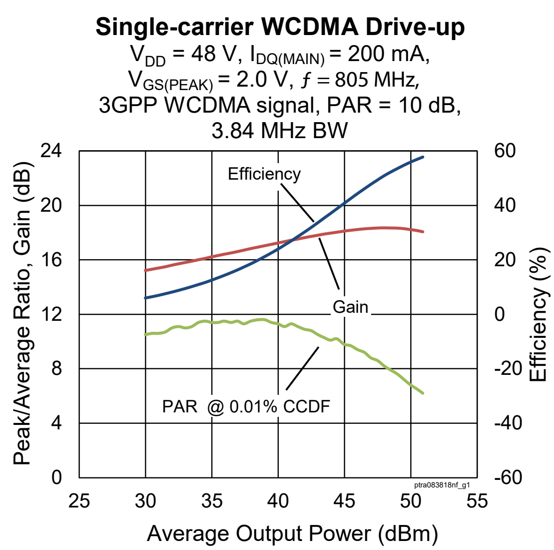
PTRA083818NF

Thermally-Enhanced High Power RF LDMOS FET
275 W, 48 V, 733 – 805 MHz

Package Types: PG-HBSOF-6-2

Description

The PTRA083818NF is a 275-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 733 to 805 MHz frequency band. Features include input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input matching
- Asymmetrical Doherty design
  - Main : P_{1dB} = 165 W Typ
  - Peak : P_{1dB} = 250 W Typ
- Typical Pulsed CW performance, 805 MHz, 48 V, combined outputs
  - Output power at P_{1dB} = 275 W
  - Efficiency = 59.6%
  - Gain = 18.6 dB
- Capable of handling 10:1 VSWR @ 48 V, 81.3 W CW output power
- Integrated ESD protection
- Human Body Model class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty production test fixture)
V_{DD} = 48 V, I_{DQ} = 200 mA, $V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 81.3 W avg, ƒ = 805 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Linear Gain	G_{ps}	17.2	18	—	dB
Drain Efficiency	η_D	53	56	—	%
Adjacent Channel Power Ratio	ACPR	—	–27.3	–24	dBc
Output PAR @ 0.01% CCDF	OPAR	5.5	6.3	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

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Rev. 06.2, 2022-1-27

DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	105	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current	I_{DSS}	—	—	1	μA	V_{DS} = 48 V, V_{GS} = 0 V
		—	—	10		V_{DS} = 105 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	1		V_{GS} = 10 V, V_{DS} = 0 V
On-State Resistance (main)	$R_{DS(on)}$	—	0.12	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
On-State Resistance (peak)		—	0.08	—		
Operating Gate Voltage (main)	V_{GS}	3	3.5	4	V	V_{DS} = 48 V, I_{DQ} = 0.20 mA
Operating Gate Voltage (peak)		—	2	—		V_{DS} = 48 V, I_{DQ} = 0 mA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	–6 to +12	
Operating Voltage	V_{DD}	0 to +55	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	0.53	°C/W	T_{CASE} = 70°C, 81.3 W CW

Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTRA083818NF V1 R5	PTRA083818NF-V1-R5	PG-HBSOF-6-2	Tape & Reel, 500 pcs

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Typical RF Performance (data taken in production test fixture)

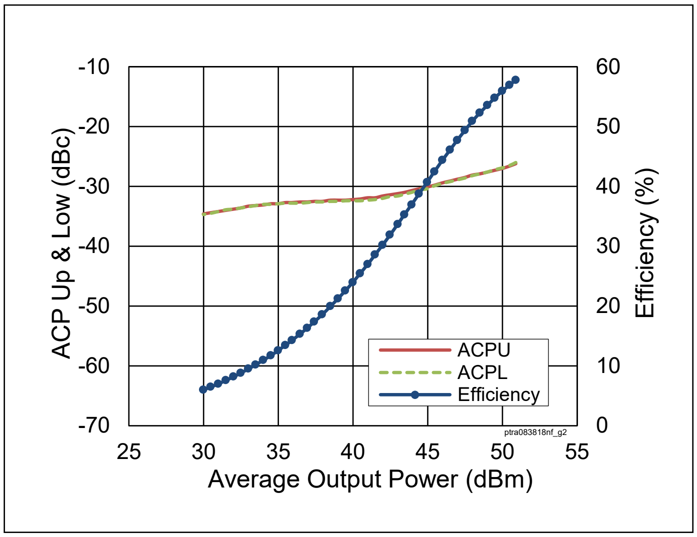

Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, f = 805 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz

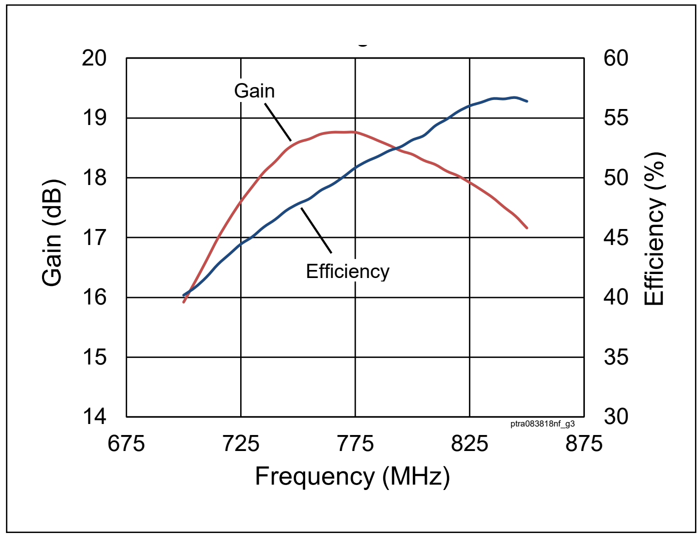

Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 49.1 dBm,
3GPP WCDMA signal, PAR = 10 dB

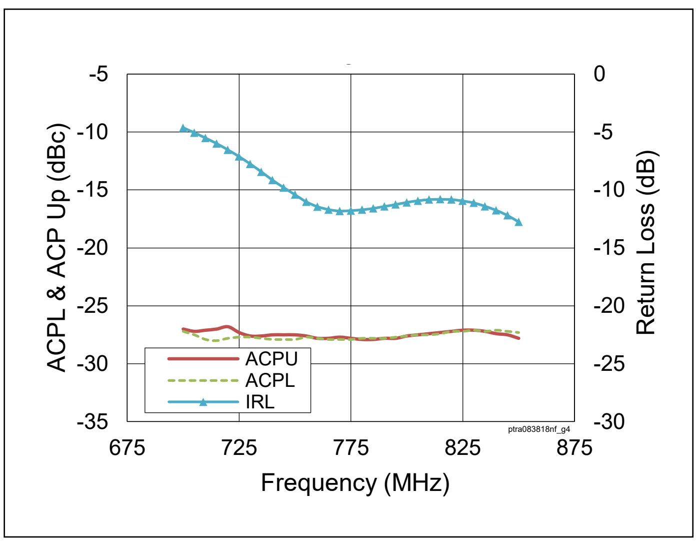

Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 49.1 dBm,
3GPP WCDMA signal, PAR = 10 dB

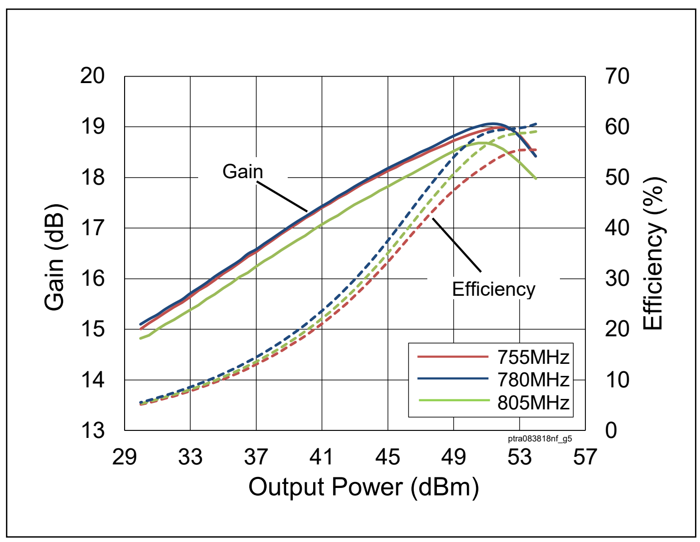

Figure 4. CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V

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Typical Performance (cont.)

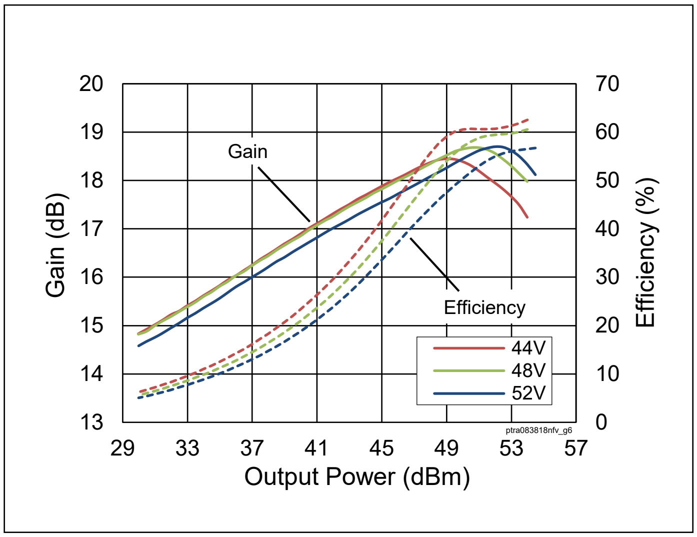

Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 200 mA, $V_{GS(PEAK)}$ = 2.0 V,
f = 805 MHz

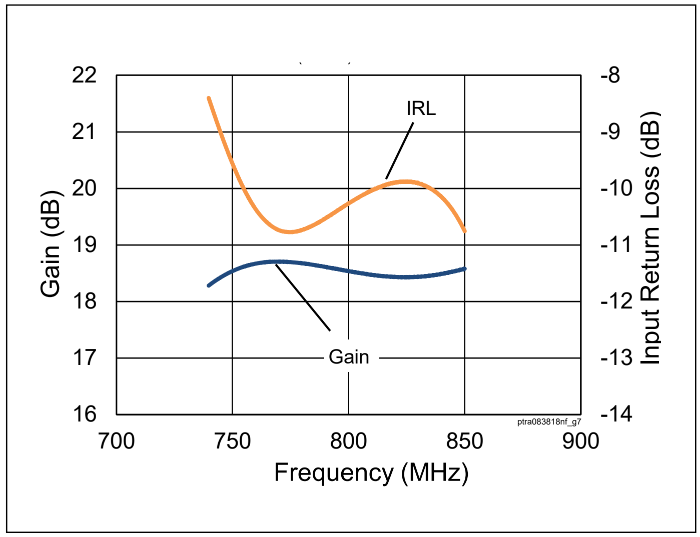

Figure 6. CW Performance Small Signal Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V

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Load Pull Performance

Main Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 350 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
760	1.8-j4.86	2.45-j0.78	20.9	53.30	212	62.0	5.91+j0.63	22.8	51.50	143	73.9
780	1.93-j4.84	2.54-j1.0	21.1	53.10	203	61.0	5.37+j1.07	22.9	51.50	140	73.6
805	2.25-j5.8	2.63-j0.92	21.2	53.10	203	62.7	4.60+j0.86	22.6	51.80	150	73.1

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
760	1.8-j4.86	2.53-j1.19	19.1	54.00	253	65.0	4.48-j0.68	20.4	53.20	208	74.8
780	1.93-j4.84	2.64-j1.16	19.3	53.90	243	65.0	5.69+j0.29	21	52.10	162	73.8
805	2.25-j5.8	2.56-j1.21	19.4	53.90	243	66.0	4.88+j0.44	21	52.30	171	74.9

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, $V_{GS(PEAK)}$ = 2.2 V, class C

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
760	2.4-j4.56	1.09-j1.11	16.5	54.90	309	60.4	1.21+j0.17	18.1	52.80	192	74.3
780	2.35-j4.58	1.03-j1.17	16.9	55.00	316	62.7	0.99+j0.3	17.8	51.90	155	75.2
805	3.25-j5.53	1.05-j1.34	16.8	54.90	309	59.8	0.95+j0.07	17.9	52.00	157	74.5

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
760	2.4-j4.56	1.13-j1.17	14.5	55.60	366	62.0	1.45+j0.08	16	53.80	237	75.1
780	2.35-j4.58	1.15-j1.17	14.8	55.80	377	64.0	1.19+j0.03	15.9	53.30	214	75.8
805	3.25-j5.53	1.32-j1.52	14.7	55.70	373	63.0	1.35-j0.06	15.9	53.50	222	74.5

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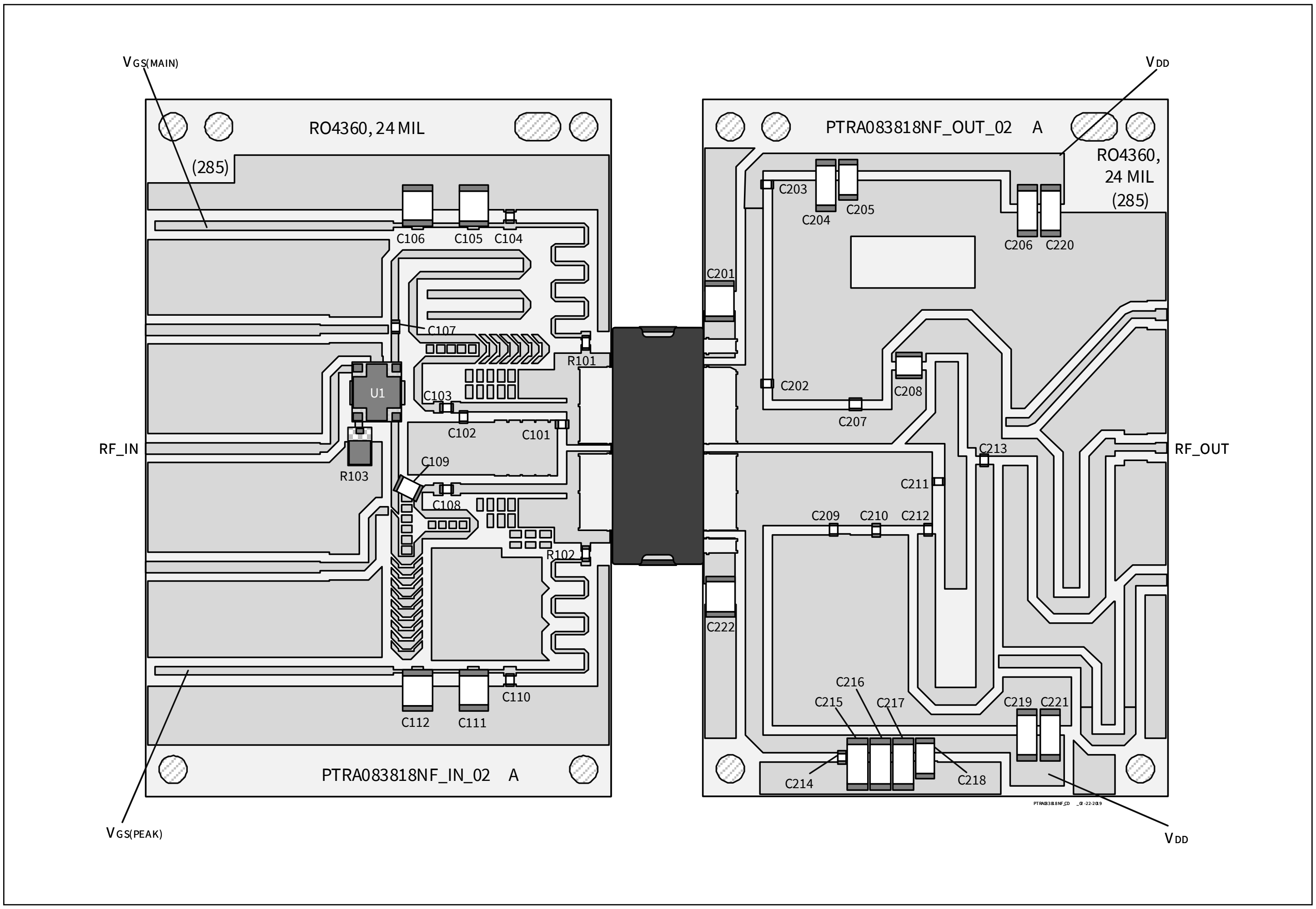
Evaluation Board, 733 – 805 MHz



Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTA/PTRA083818NF-V1
PCB Information	Rogers 4360, 0.609 mm [0.024”] thick, 2 oz. copper, ε_r = 6.4, f = 733 – 805 MHz

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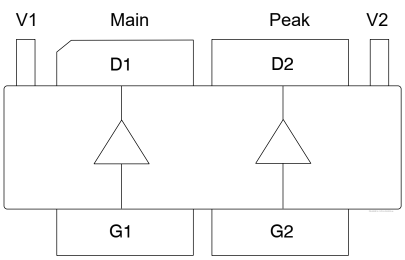
Components Information

Component	Description	Manufacturer	P/N
Input			
C101	Capacitor, 10 pF	ATC	ATC800A100JT250T
C102	Capacitor, 5.6 pF	ATC	ATC800A5R6CT250T
C103, C104, C108, C110	Capacitor, 82 pF	ATC	ATC800A820JT250T
C105, C106, C111, C112	Capacitor, 2.2 µF	TDK Corporation	C4532X7R1H225M160KA
C107	Capacitor, 20 pF	ATC	ATC800A200JT250T
C109	Capacitor, 9.1 pF	ATC	ATC100B9R1CW500XB
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-3GEYJ100V
R103	Resistor, 50 ohms	Richardson	C8A50Z4A
U1	Hybrid Coupler	Anaren	X3C07P1-05S
Output			
C201, C222	Capacitor, 2.2 µF	TDK Corporation	C4532X7R1H225M160KA
C202	Capacitor, 2.7 pF	ATC	ATC800A2R7CT250T
C203, C214	Capacitor, 82 pF	ATC	ATC800A820JT250T
C204, C206, C215, C216, C217, C219, C220, C221	Capacitor, 10 µF	TDK Corporation	C5750X7S2A106M230KB
C205, C218	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C207, C210	Capacitor, 3.9 pF	ATC	ATC800A3R9CT250T
C208	Capacitor, 12 pF	ATC	ATC100B120JW500XB
C209	Capacitor, 5.6 pF	ATC	ATC800A5R6CT250T
C211	Capacitor, 1.2 pF	ATC	ATC800A1R2CT250T
C212	Capacitor, 6.8 pF	ATC	ATC800A6R8CT250T
C213	Capacitor, 100 pF	ATC	ATC800A101JT250T

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1	Drain video decoupling, no DC bias
V2	NC or connected to GRD

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Package Outline Specifications – Package PG-HBSOF-6-2 (top view)

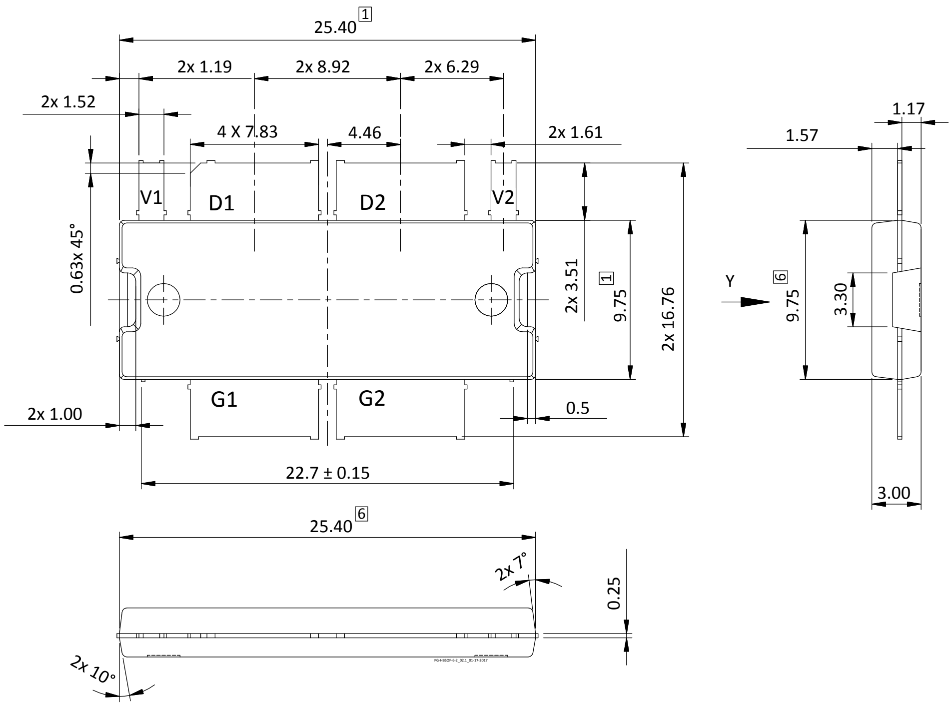

Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Does not include mold/dam bar and metal protrusion.
7. Exposed metal surface is tin-plated, may not be covered by mold compound.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces are tin-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; S = source; V1 = drain video decoupling, no DC Bias, V2 = NC or connected to GRD

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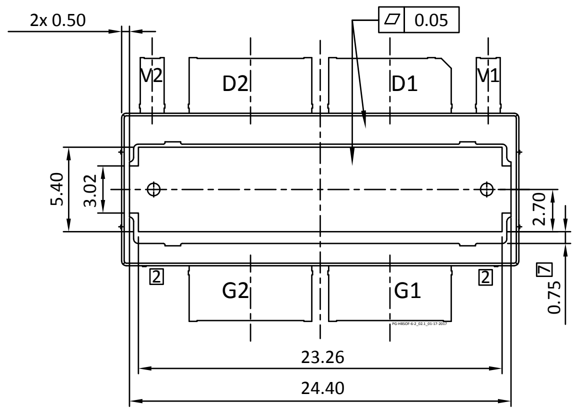
Package Outline Specifications (cont.) **– Package PG-HBSOF-6-2** (bottom view)



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