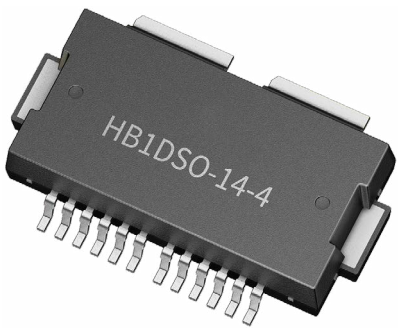
PTMC210404MD

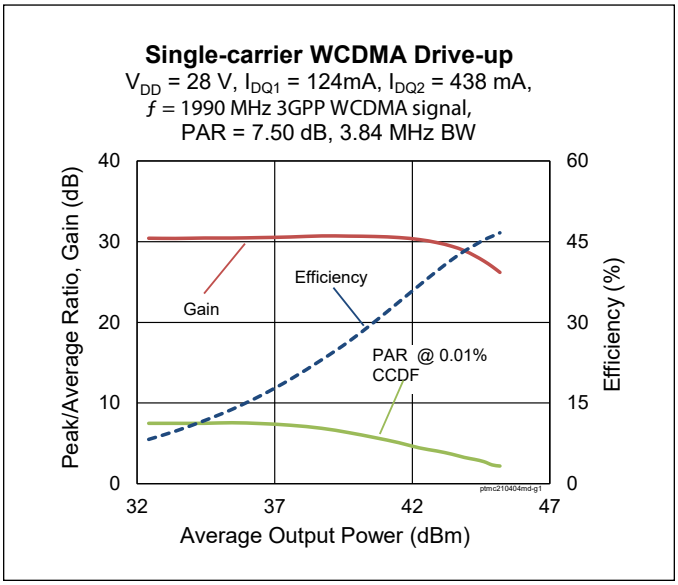
Wideband LDMOS Two-stage Integrated Power Amplifier
2 x 20 W, 28 V, 1805 – 2200 MHz



Package Types: PG-HB1DSO-14-4 (formed leads)

Description

The PTMC210204MD is a wideband, two-stage LDMOS integrated amplifier intended for wideband driver applications. It has internal matching for operation from 1805 to 2200 MHz. It features on-chip matching high efficiency, and dual independent outputs with 20 W of output power each. It is available in a 14-lead plastic overmold package with gull wing leads.



Features

- On-chip matching for broadband operation
- Typical pulsed CW performance, 1990 MHz, 28 V, combined outputs
  - Output power at P1dB = 37 W
  - Linear Gain = 31.5 dB
  - Efficiency = 53.1%
- Capable of handling 10:1 VSWR @28 V, 37 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1B (per ANSI/ESDA/JEDEC JS-001)
- Integrated temperature compensation
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the test fixture)

V_{DD} = 28 V, $I_{DQ1(A+B)}$ = 63 mA, $I_{DQ2(A+B)}$ = 219 mA, P_{OUT} = 5 W avg, ƒ = 1990 MHz, 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 7.5 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Linear Gain	G_{ps}	29	30	—	dB
Power Added Efficiency	PAE	17.5	18.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–49.5	-47.5	dBc
Output PAR @ 0.01% CCDF	OPAR	7.0	7.2	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics

Stage 1	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain Leakage Current	I_{DSS}	—	—	0.1	µA	V_{DS} = 28 V, V_{GS} = 0 V
		—	—	1.0		V_{DS} = 60 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	0.1		V_{GS} = 1 V, V_{DS} = 0 V
On-State Resistance	$R_{DS(on)}$	—	5	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
Operating Gate Voltage	V_{GS1}	—	2.7	—	V	V_{DS} = 28 V, I_{DQ1} = 63 mA
Fixture Operating Gate Voltage		—	4.9	—		

Stage 2	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage	$V_{BR(DSS)}$	64	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current	I_{DSS}	—	—	0.1	µA	V_{DS} = 28 V, V_{GS} = 0 V
		—	—	1.0		V_{DS} = 60 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	0.1		V_{GS} = 1 V, V_{DS} = 0 V
On-State Resistance	$R_{DS(on)}$	—	1.5	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
Operating Gate Voltage	V_{GS2}	—	2.7	—	V	V_{DS} = 28 V, I_{DQ2} = 219 mA
Fixture Operating Gate Voltage		—	4.9	—		

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	
Operating Voltage	V_{DD}	0 to 32	V

Thermal Characteristics

Characteristic	Symbol	Value	Unit	Conditions
Thermal Resistance Stage 1	$R_{\theta JC}$	6.7	°C/W	T_{CASE} = 70°C, 37 W CW
Thermal Resistance Stage 2		1.4		T_{CASE} = 70°C, 37 W CW

Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTMC210404MD V2 R5	PTMC210404MD-V2-R5	PG-HB1DSO-14-4, 14-lead, overmold	Tape & Reel, 500 pcs

Evaluation Boards

Order Code	Frequency	Description
LTN/PTMC210404MD-V2	1805 – 2200 MHz	Class AB with combined outputs, R04350, 0.508 mm thick

Typical Performance (data taken in a production test fixture)

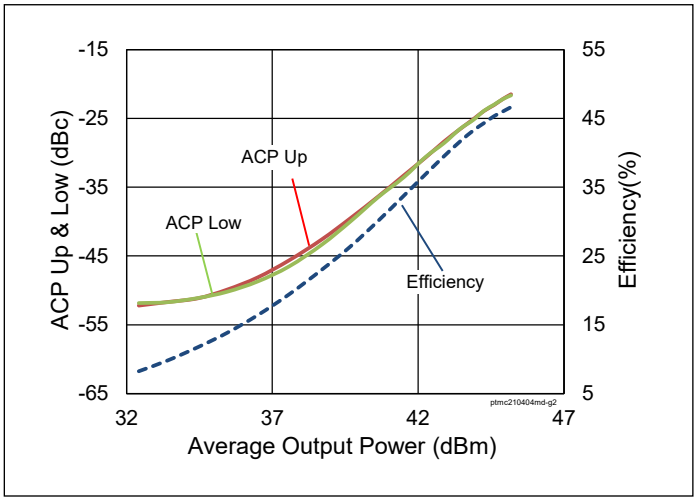


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 28 V, I_{DQ1} = 124mA, I_{DQ2} = 438 mA,
f = 1990 MHz, 3GPP WCDMA signal,
PAR = 7.50 dB, BW = 3.84 MHz

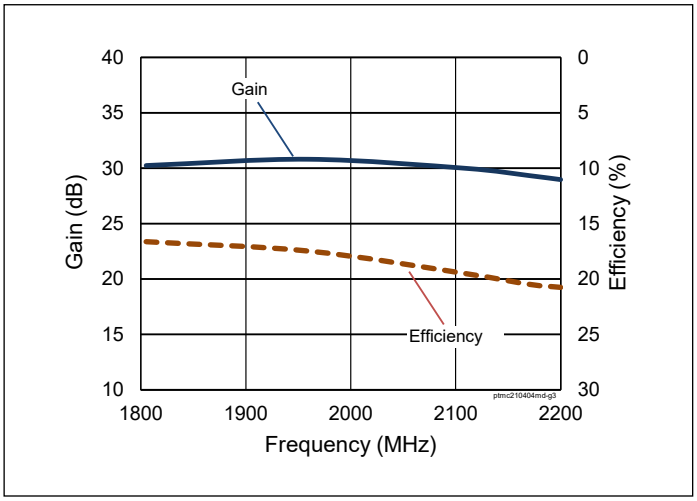


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 28 V, I_{DQ1} = 124mA, I_{DQ2} = 438 mA,
P_{OUT} = 37dBm, 3GPP WCDMA signal,
PAR = 7.50 dB

Typical Performance (cont.)

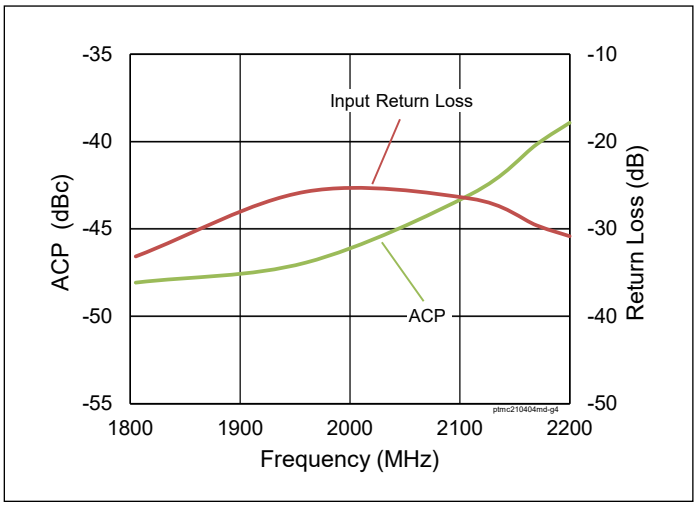


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 28 V, I_{DQ1} = 124mA, I_{DQ2} = 438 mA,
P_{OUT} = 37dBm, 3GPP WCDMA signal,
PAR = 7.50 dB

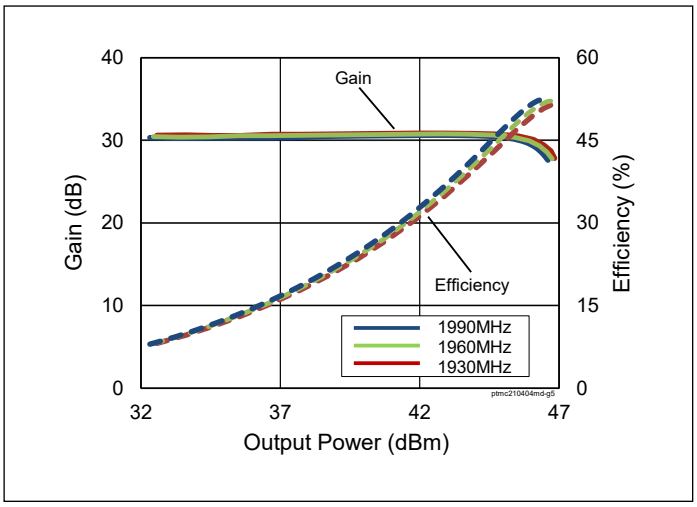


Figure 4. CW Performance

V_{DD} = 28 V, I_{DQ1} = 124mA, I_{DQ2} = 438 mA

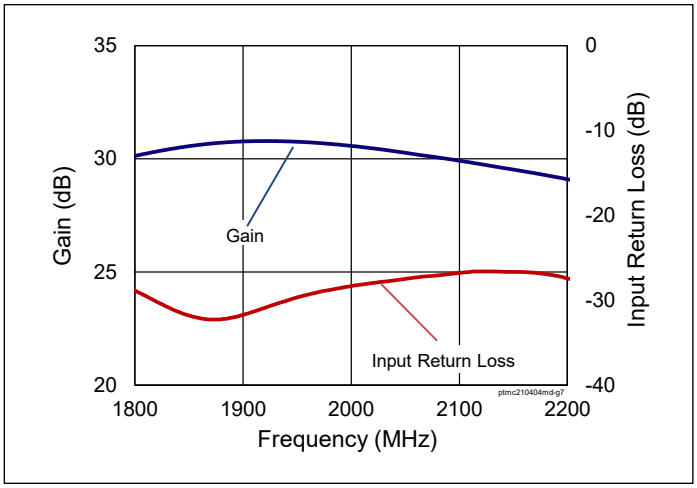


Figure 5. Small Signal CW Gain & Input Return Loss

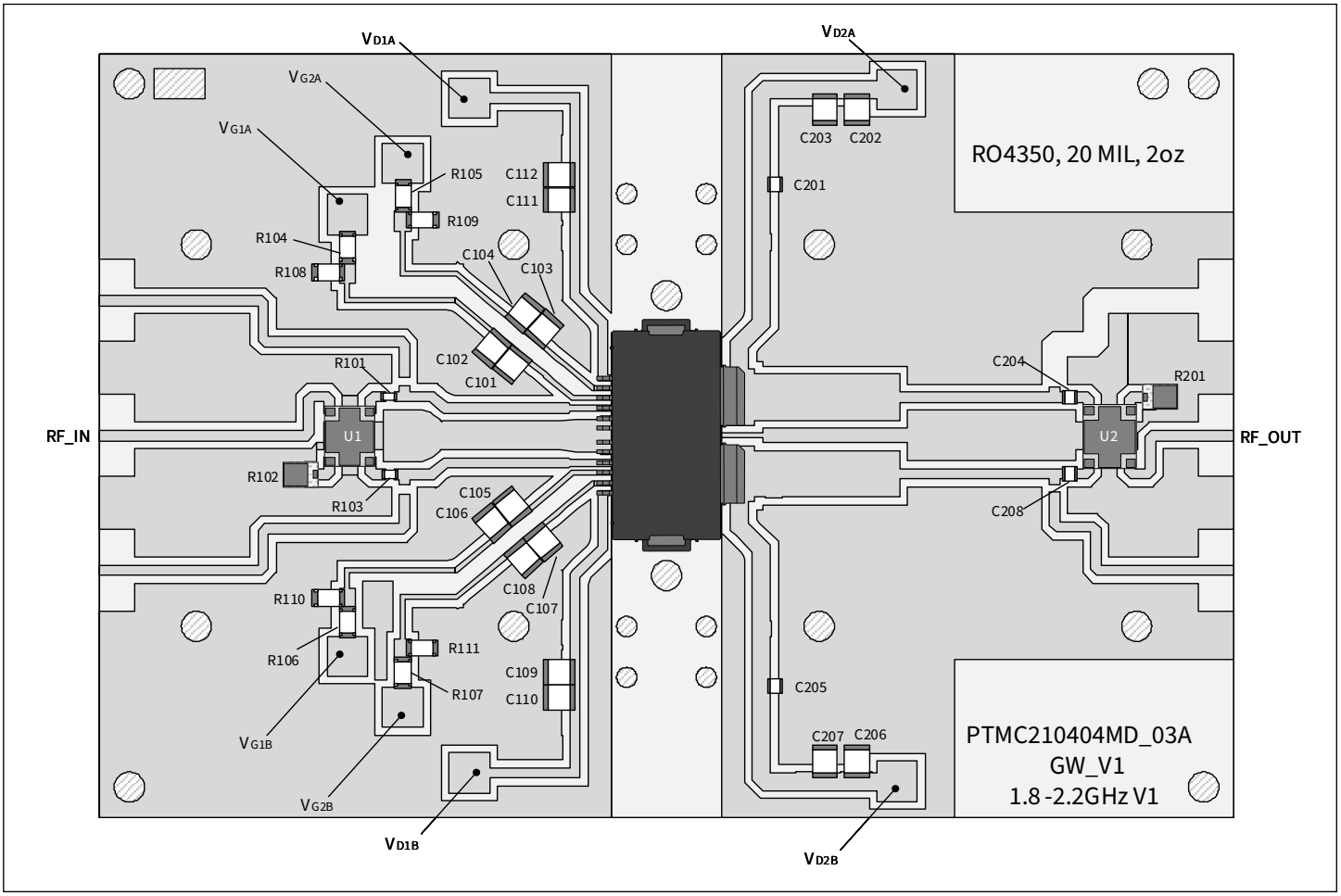
V_{DD} = 28 V, I_{DQ1} = 124mA, I_{DQ2} = 438 mA

Load Pull Performance

Load Pull Performance – Pulsed CW signal: V_{DD} = 28 V, I_{DQ1} = 63 mA, I_{DQ2} = 219 mA, class AB, each side

Class AB		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1805	49.8+j2.3	8.8-j6.30	29.8	43.8	23.8	51.2	13.4-j3.7	31.0	42.9	19.4	55.9
1960	49.9-j0.1	8.5-j8.20	29.5	43.8	23.9	50.5	10.9-j2.4	31.0	42.7	18.5	57.0
2170	51.9+j0.2	7.4-j7.60	27.9	43.9	24.3	51.8	7.10-j3.8	29.0	42.9	19.6	56.6
2200	49.3+j1.0	7.7-j7.70	27.6	43.8	23.8	51.5	6.90-j3.7	28.8	42.8	19.0	56.6

Evaluation Board, 1805 – 2200 MHz



Reference circuit assembly diagram (not to scale)

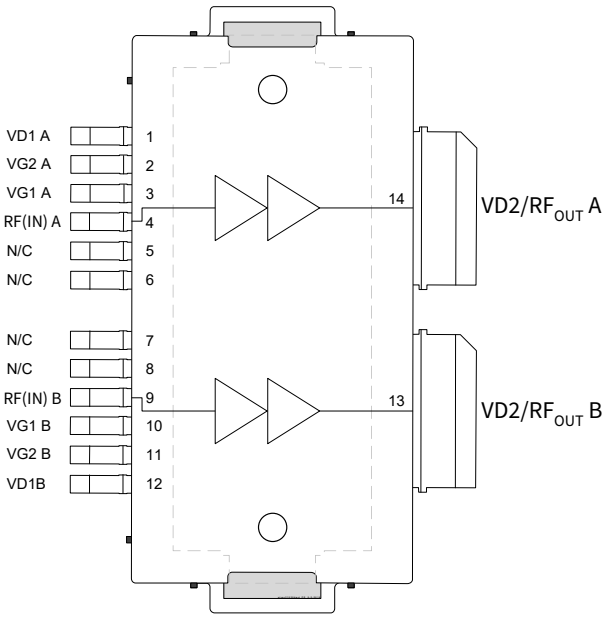
Evaluation Board, 1805 – 2200 MHz (cont.)

Evaluation Board Part No.	LTN/PTMC210404MD-V2
PCB Information	Rogers 4350B, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, ƒ = 1805 – 2200 MHz

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C103, C105, C107, C109, C111, C203, C207	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C102, C104, C106, C108, C110, C112, C202, C206	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C201, C204, C205, C208	Capacitor, 10 pF	ATC	ATC800A100JT250T
R101, R103	Resistor, 0.0 ohms	Panasonic Electronic Components	ERJ-3GEY0R00V
R102, R201	Resistor, 50 ohms	Anaren	C8A50Z4A
R104, R105, R106, R107	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
R108, R109, R110, R111	Resistor, 4.3K ohms	Panasonic Electronic Components	ERJ-8GEYJ432V
U1, U2	Hybrid Coupler	Anaren	X3C21P1-03S

Pinout Diagram



Source: plated copper heat slug on backside of package

Package Outline Specifications – Package PG-HB1DSO-14-4

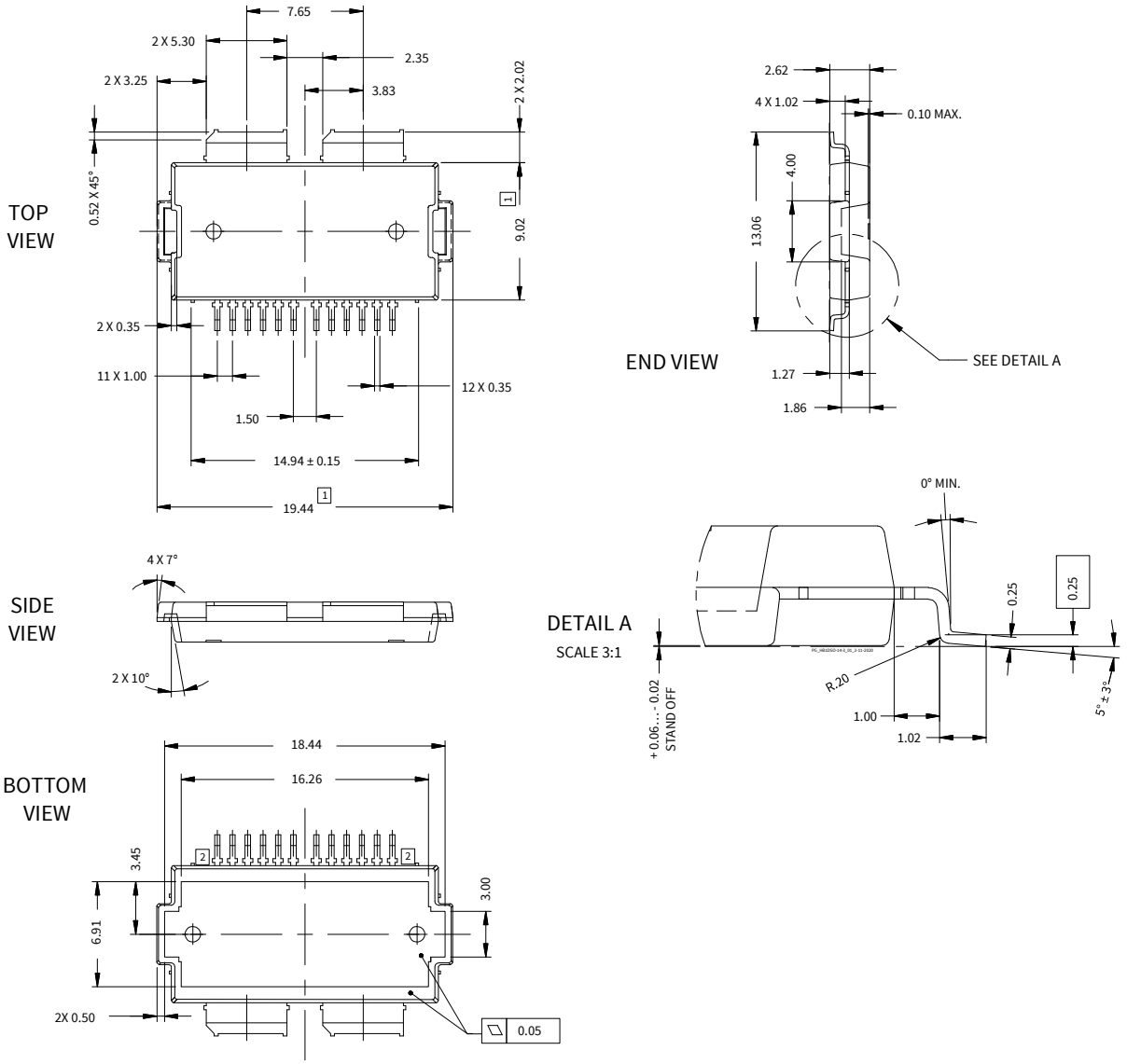


Diagram Notes–unless otherwise specified:

1. Mold/Dam Bar/Metal protrusion of 0.30 mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. All tolerances ± 0.1 mm unless specified otherwise.
7. All metal surfaces are tin-plated, except area of cut.
8. Lead thickness: 0.25 mm.

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