

Features

Guaranteed Performance @ 30 MHz, 50 V:

- Output Power: 150 W
- Gain: 18 dB (22 dB Typ.)
- Efficiency: 40%

Typical Performance @ 175 MHz, 50 V:

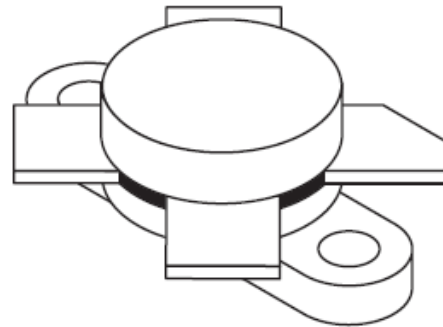
- Output Power: 150 W
- Gain: 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Binned by Gfs and Vth for pairing

Applications

- Aerospace & Defense
- ISM

Description

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.



CASE 211-11, STYLE 1

Electrical Specifications: $T_C = +25^\circ\text{C}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Off Characteristics					
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 100\text{ mA}$	Vdc	125	—	—
Zero Gate Voltage	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$	mAdC	—	—	5
Gate-Body Leakage Current	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	mAdc	—	—	1
On Characteristics					
Gate Threshold Voltage	$V_{DS} = 10\text{ V}, I_D = 100\text{ mA}$	Vdc	2.525	3.0	3.65
Drain-Source On-Voltage	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Vdc	1	3	5
Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$	mhos	6.3	7	7.9
Dynamic Characteristics					
Input Capacitance	$V_{DC} = 50\text{ V}, V_{GS} = 0\text{ V}, \text{Freq.} = 1\text{ MHz}$	pF	—	350	—
Output Capacitance	$V_{DC} = 50\text{ V}, V_{GS} = 0\text{ V}, \text{Freq.} = 1\text{ MHz}$	pF	—	220	—
Reverse Transfer Capacitance	$V_{DC} = 50\text{ V}, V_{GS} = 0\text{ V}, \text{Freq.} = 1\text{ MHz}$	pF	—	15	—
Functional Tests					
Common Source Amplifier Power Gain	$V_{DD} = 50\text{ V}, P_{OUT} = 150\text{ W (PEP)}, I_{DQ} = 250\text{ mA},$ Freq = 30; 30.001 MHz Freq = 175 MHz	dB dB	18 —	22 13	— —
Drain Efficiency	$V_{DD} = 50\text{ V}, P_{OUT} = 150\text{ W (PEP)}$ Freq = 30 MHz; 30.001 MHz, $I_D = 3.75\text{ A}$	%	40	45	—
Intermodulation Distortion	$V_{DD} = 50\text{ V}, P_{OUT} = 150\text{ W (PEP)}, I_{DQ} = 250\text{ mA},$ Freq.1 = 30.000 MHz, Freq.2 = 30.001 MHz	dB	—	-32 -60	-30 —
Load Mismatch	$V_{DD} = 50\text{ V}, P_{OUT} = 150\text{ W (PEP)}, I_{DQ} = 250\text{ mA},$ Freq = 30 MHz; 30.001 MHz, @ all phase angles	No Degradation in Output Power			
Class A Performance					
Intermodulation Distortion ¹ & Power Gain	$V_{DD} = 50\text{ V}, P_{OUT} = 50\text{ W (PEP)}, I_{DQ} = 250\text{ mA},$ Freq = 30 MHz; 30.001 MHz, $I_D = 3\text{ A}$	dB	—	23 -50 -75	—

1. MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

Absolute Maximum Ratings^{2,3}

Parameter	Absolute Maximum
Drain-Source Voltage	125 V
Gate-Source Voltage	125 V
Gate-Source Voltage	±40 V
Drain Current - Continuous	16 A _{DC}
Total Device Dissipation @ T _C = +25°C, Derate above +25°C	300 W, 1.71 W/°C
Junction Temperature	+200°C
Storage Temperature	-65°C to +150°C
Thermal Characteristics	
Thermal Resistance, Junction-to-Case	0.6°C/W

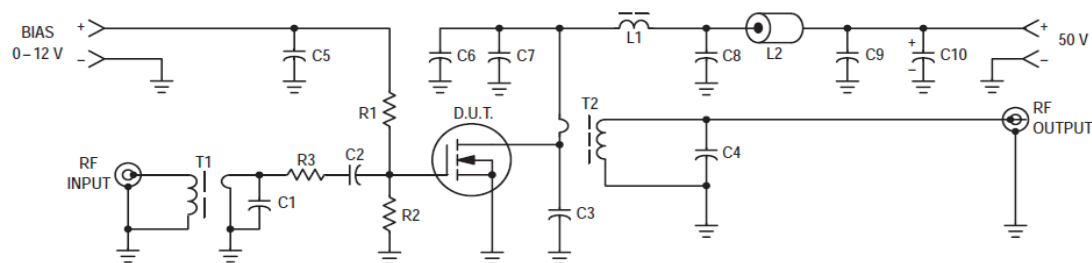
- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.



- | | |
|---|--|
| C1 — 470 pF Dipped Mica | L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH |
| C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolithic with Short Leads | L2 — Ferrite Bead(s), 2.0 μH |
| C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads | R1, R2 — 51 Ω/1.0 W Carbon |
| C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads | R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel) |
| C10 — 10 μF/100 V Electrolytic | T1 — 9:1 Broadband Transformer |
| | T2 — 1:9 Broadband Transformer |
| | Board Material — 0.062" Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε _r = 5 |

Figure 1. 30 MHz Test Circuit

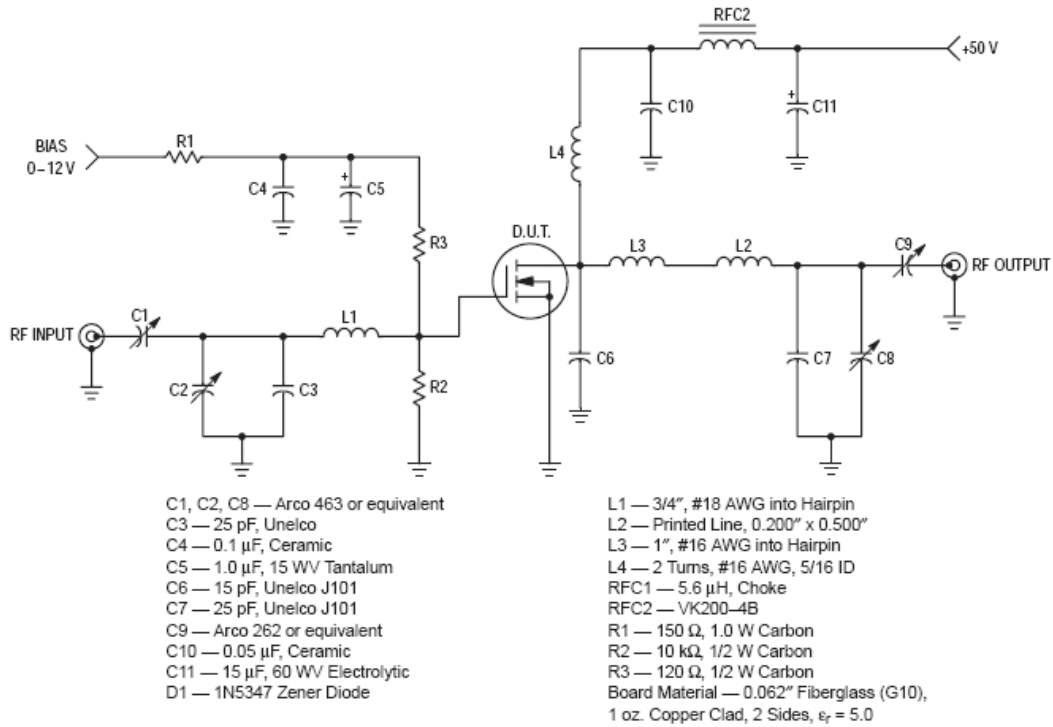


Figure 2. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

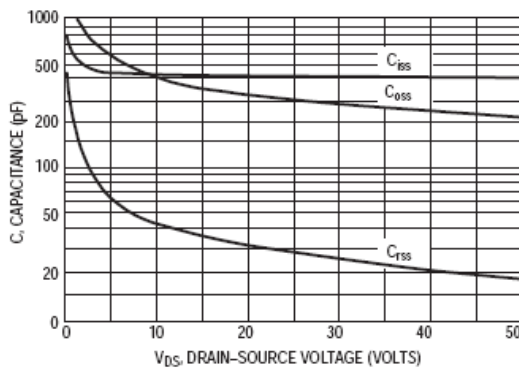


Figure 3. Capacitance versus Drain-Source Voltage

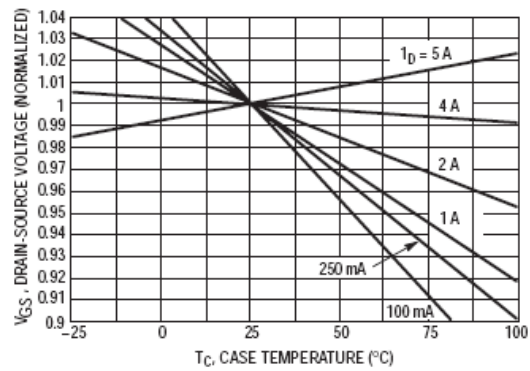


Figure 4. Gate-Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS

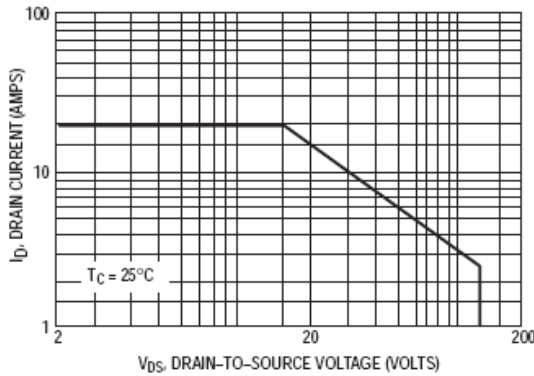


Figure 5. DC Safe Operating Area

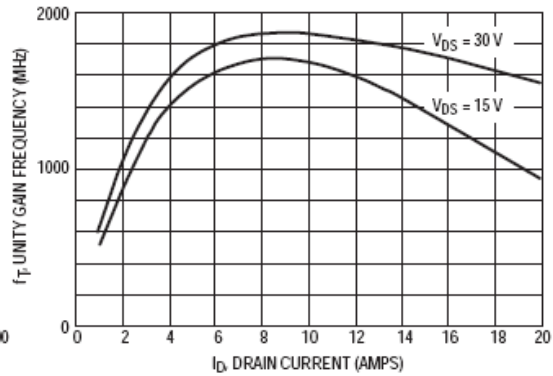


Figure 6. Common Source Unity Gain Frequency versus Drain Current

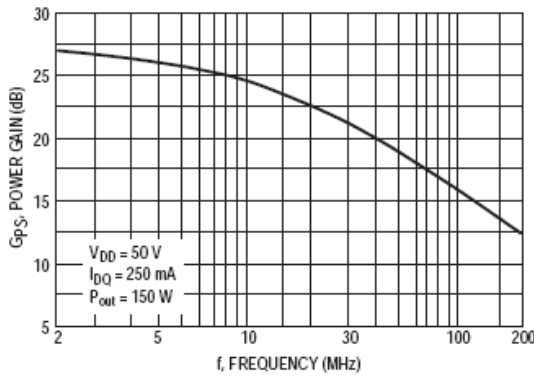


Figure 7. Power Gain versus Frequency

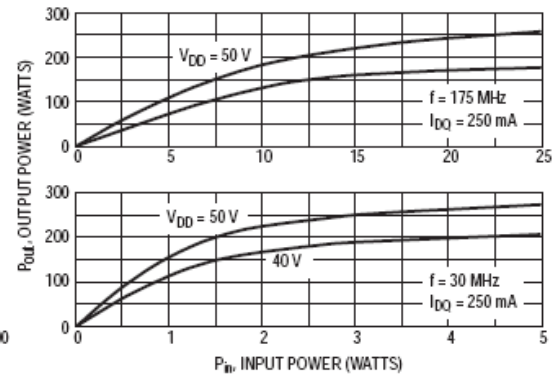


Figure 8. Output Power versus Input Power

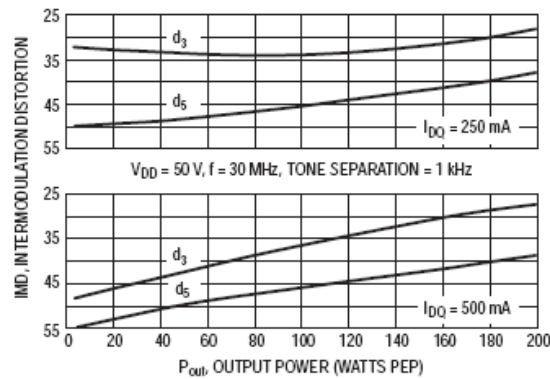


Figure 9. IMD versus P_{out}

Table 1. Common Source S-Parameters ($V_{DS} = 50\text{ V}$, $I_D = 2\text{ A}$) continued

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
250	0.972	177	0.51	12	0.039	80	0.935	179
260	0.973	177	0.47	11	0.041	79	0.954	178
270	0.972	176	0.45	9	0.044	80	0.953	176
280	0.974	176	0.41	9	0.046	80	0.965	175
290	0.974	176	0.40	6	0.046	79	0.944	175
300	0.975	176	0.39	10	0.048	82	0.929	176
310	0.976	175	0.36	9	0.049	82	0.943	176
320	0.974	175	0.33	7	0.053	78	0.954	173
330	0.975	174	0.31	4	0.056	78	0.935	172
340	0.976	174	0.30	10	0.056	77	0.948	172
350	0.975	174	0.29	7	0.058	80	0.950	174
360	0.977	174	0.28	8	0.059	79	0.978	172
370	0.976	173	0.26	8	0.061	76	0.981	170
380	0.976	173	0.26	7	0.065	75	0.944	171
390	0.977	173	0.24	10	0.066	76	0.960	171
400	0.976	172	0.23	7	0.068	80	0.955	173
410	0.976	172	0.22	9	0.071	77	0.999	170
420	0.977	172	0.21	9	0.071	76	0.962	168
430	0.976	171	0.19	10	0.073	76	0.950	168
440	0.976	171	0.20	12	0.075	75	0.953	168
450	0.978	171	0.19	10	0.080	77	0.982	168
460	0.978	170	0.18	13	0.082	74	0.990	165
470	0.978	170	0.18	10	0.081	77	0.953	168
480	0.974	170	0.18	13	0.085	78	0.944	167
490	0.973	169	0.17	13	0.086	75	0.966	165
500	0.972	169	0.17	14	0.089	73	0.980	165

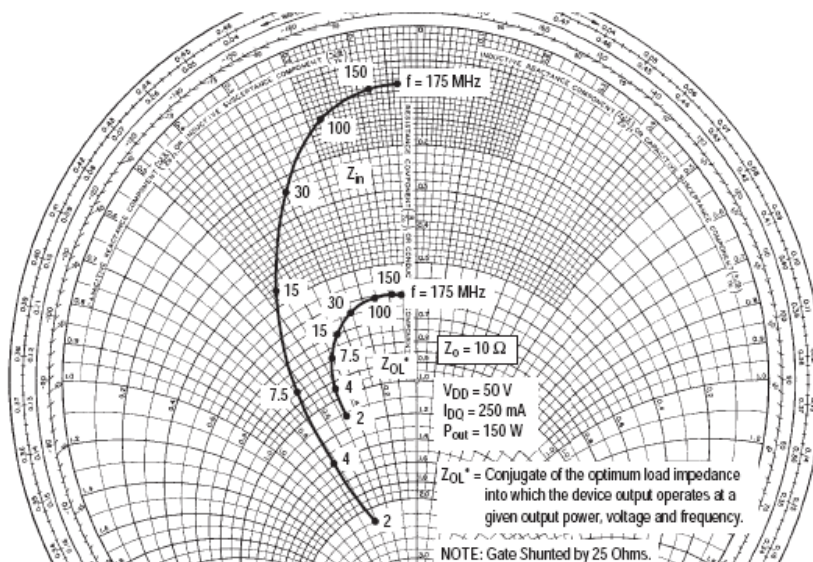


Figure 10. Series Equivalent Impedance

Table 1. Common Source S-Parameters ($V_{DS} = 50\text{ V}$, $I_D = 2\text{ A}$)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
30	0.877	-174	10.10	77	0.008	19	0.707	-169
40	0.886	-175	7.47	69	0.009	24	0.715	-172
50	0.895	-175	5.76	63	0.008	33	0.756	-171
60	0.902	-176	4.73	58	0.009	39	0.764	-171
70	0.912	-176	3.86	52	0.009	46	0.784	-172
80	0.918	-177	3.19	48	0.010	54	0.802	-171
90	0.925	-177	2.69	45	0.011	62	0.808	-171
100	0.932	-177	2.34	40	0.013	67	0.850	-173
110	0.936	-178	2.06	37	0.014	72	0.865	-175
120	0.942	-178	1.77	35	0.015	76	0.875	-173
130	0.946	-179	1.55	32	0.017	77	0.874	-172
140	0.950	-179	1.39	30	0.019	77	0.884	-174
150	0.954	-180	1.23	27	0.021	78	0.909	-175
160	0.957	-180	1.13	24	0.023	79	0.911	-176
170	0.960	180	1.01	22	0.024	82	0.904	-177
180	0.962	179	0.90	20	0.026	82	0.931	-176
190	0.964	179	0.84	19	0.028	80	0.929	-178
200	0.967	179	0.75	18	0.030	79	0.922	-179
210	0.967	178	0.71	16	0.032	80	0.937	-180
220	0.969	178	0.67	14	0.035	82	0.949	180
230	0.971	178	0.60	12	0.038	81	0.950	179
240	0.970	177	0.57	12	0.037	80	0.950	179

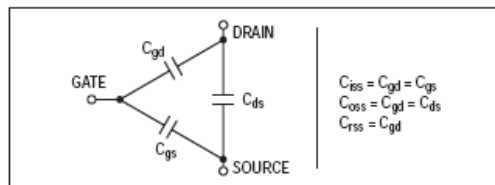
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 6 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open-circuited or float-

ing should be avoided. These conditions can result in turn-on of the device due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF151 is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

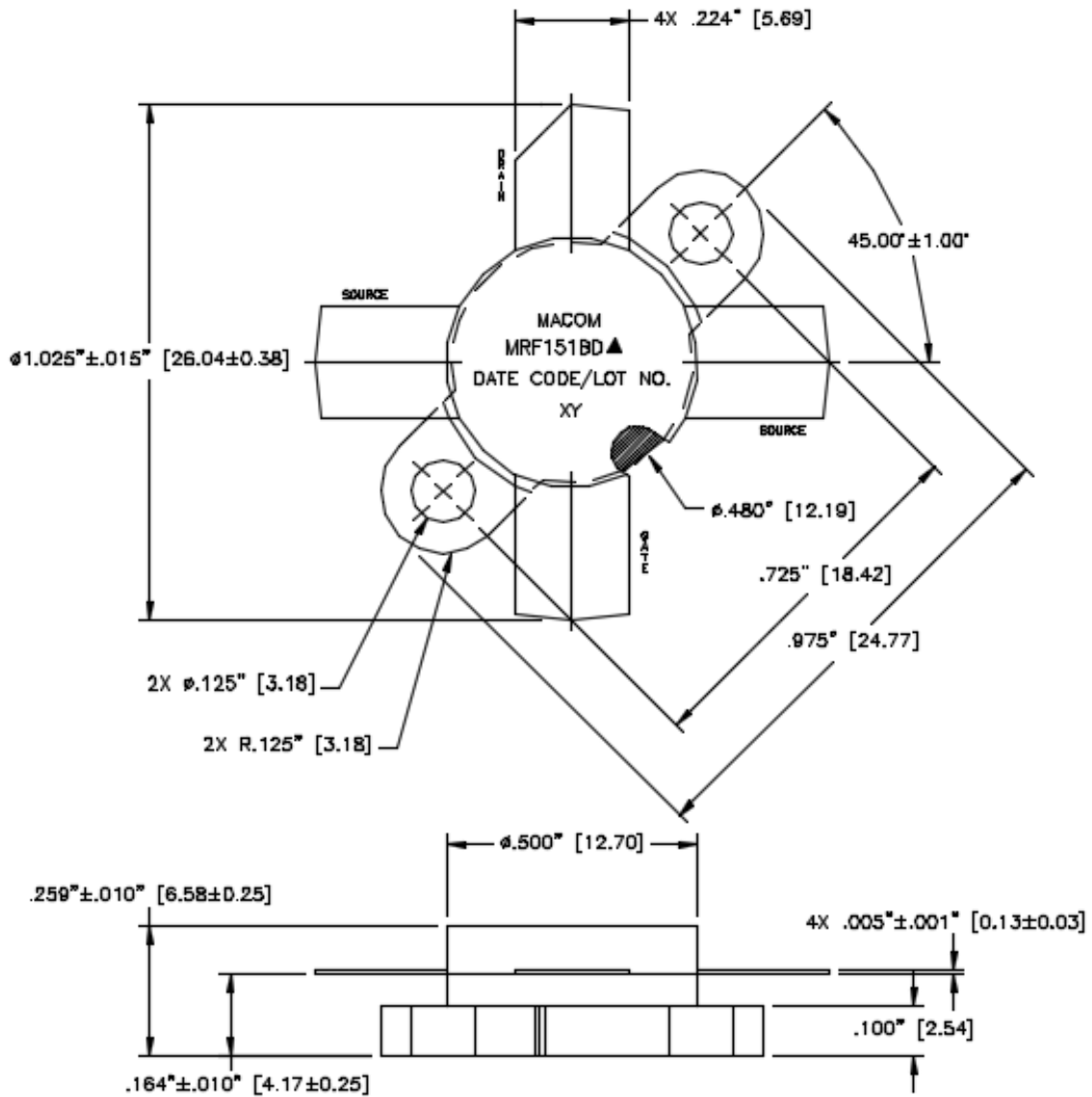
DC BIAS

The MRF151 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF151 was characterized at $I_{DQ} = 250$ mA, each side, which is the suggested minimum value of I_{DQ} . For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

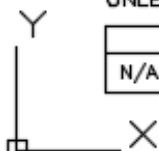
The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF151 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.



UNLESS OTHERWISE NOTED, TOLERANCES ARE INCHES $\pm .005''$ [MILLIMETERS $\pm 0.13\text{mm}$]



LEAD TRIMMING INSTRUCTIONS
N/A

MARKING INSTRUCTIONS
LETTER CODE "X" INDICATES ALPHA G _{fs} CODE
LETTER CODE "Y" INDICATES ALPHA V _{th} CODE.

MRF151BDMP can be matched based on Gfs and Vth values as detailed in the table below:

Gfs ALPHA	MIN	MAX
E	6.300	7.000
F	7.001	7.900

Vth ALPHA	MIN	MAX
A	2.525	2.600
B	2.601	2.675
C	2.676	2.750
D	2.751	2.825
E	2.826	2.900
F	2.901	2.975
G	2.976	3.050
H	3.051	3.125
J	3.126	3.200
K	3.201	3.275
M	3.276	3.350
N	3.351	3.425
P	3.426	3.500
R	3.501	3.575
S	3.576	3.650

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