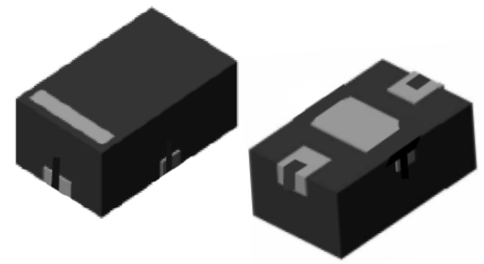
MLP7120-2012

Surface Mount Limiter PIN Diode

Rev. V2

Features

- Low Junction Capacitance for Low Insertion Loss and High Isolation: C_T6 <0.3 pF
- Low Series Resistance for High Isolation: R_S <1 Ω
- Nominal I Layer Width: W = 10 µm
- Compact Surface Mount Plastic Package
- RoHS* Compliant



2012

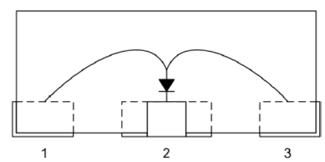
Description

The MLP7120-2012 limiter PIN diode is a low series resistance The MLP7120-2012 limiter PIN diode is a low series resistance, low capacitance limiter PIN diode packaged in a surface mount, low-parasitic plastic package. It is manufactured using a proprietary diode process for excellent performance and high reliability.

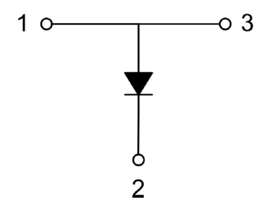
The 10 µm nominal I layer width of this diode produces a threshold level of 20 dBm nominal, for demanding receiver protection applications. The low series resistance (<1 Ω), and low total capacitance (<0.3 pF) of MLP7120-2012 produce excellent isolation and insertion loss in shunt, receiver protection applications.

The MLP7120-2012 limiter PIN diode is designed to be used in receiver protection applications.

Pin out / Schematic



Side View



Ordering Information

Part Number	Package
MLP7120-2012-R	3000 piece reel
MLP7120-2012-B	100 per bag bulk
MLP7120-2012-W	400 piece waffle pack

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 0 devices.

Moisture Sensitivity

These electronic devices are rated MSL 1.

Environmental Capabilities

Capable of meeting the environmental requirements of MIL-STD-750 and MIL-STD-883.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: T_A = +25°C (measured on evaluation board)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage (V_B)	I_R = 10 µA	V	120	—	180
Forward Voltage (V_F)	I_F = 100 mA	V	—	0.95	1.2
Total Capacitance[1] (C_T)	V_R = 6 V, 1 MHz	pF	—	—	0.3
Series Resistance[2] (R_S)	I_F = 1 mA, 1 GHz I_F = 10 mA, 1 GHz	Ω	—	3.5 1.0	—
Recovery Time (T_R)	End of the RF input to 1 dB excess insertion loss	ns	—	50	—
Minority Carrier Lifetime (T_L)	50% control to 90% output voltage, I_F = 10 mA, I_R = 6 mA, 1 KHz	ns	—	50	—
Thermal Resistance (θ_{JC})	—	°C/W	—	—	45
I layer Thickness (W)	—	µm	—	10	—

1. Total capacitance (C_T) is the sum of the diode junction capacitance (C_J) and the package capacitance (C_{PKG}).
2. Series resistance (R_S) is measured on the HP 4291 Impedance Analyzer.

Absolute Maximum Ratings

Parameter	Test Conditions	Absolute Maximum
Forward DC Current	—	150 mA
Reverse DC Voltage	—	180 V
Forward DC Voltage	I_F = 150 mA	1.3 V
Peak RF Input Power	Pulse Width = 1 µs, Duty Cycle = 1%	60 dBm
CW Input Power	—	37 dBm
Junction Temperature	—	+175°C
Operating Temperature	—	-55°C to +150°C
Storage Temperature	—	-65°C to +100°C
Assembly Temperature	t = 10 s	+260°C

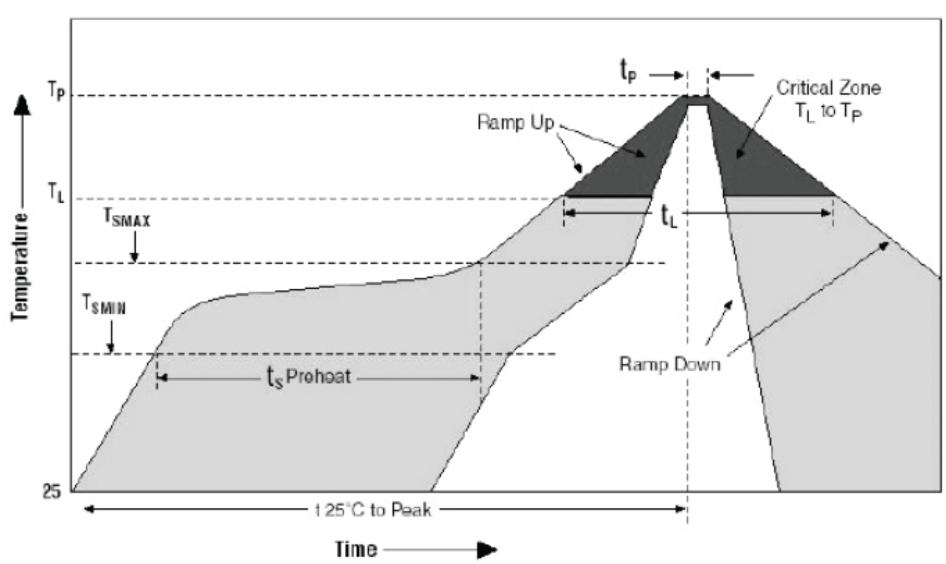
Assembly Instructions

Diodes may be placed onto circuit boards with pick and place manufacturing equipment from tape-reel. The devices are attached to the circuit using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60 / Pb 40 type solders.

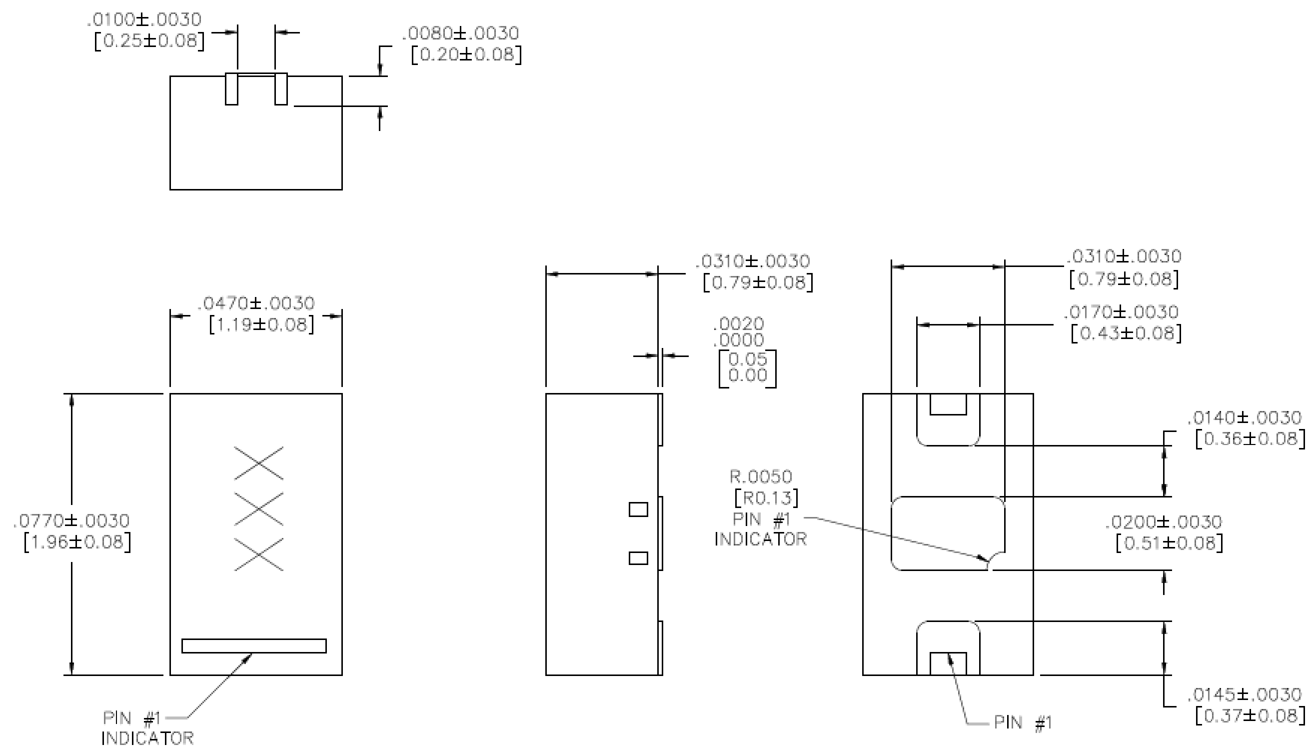
Table 1. Time-Temperature Profile for Sn60/Pb40 or RoHS Type Solders

Profile Feature	SnPb Solder Assembly	Pb-Free Solder Assembly
Average Ramp-Up Rate (T_L to T_P)	3°C /second maximum	3°C /second maximum
Preheat: -Temperature Min (T_{SMIN}) -Temperature Max (T_{SMAX}) -Time (min to max)(t_S)	100°C 150°C 60 - 120 s	150°C 200°C 60 - 180 s
T_{SMAX} to T_L - Ramp-Up Rate		3°C /s maximum
Time Maintained Above: -Temperature (T_L) - Time (t_L)	183°C 60 - 150 s	217°C 60 - 150 s
Peak temperature (T_P)	225 +0/-5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 – 30 s	20 – 40 s
Ramp-Down Rate	6°C /s maximum	6°C /s maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Figure 1. Solder Re-Flow Time-Temperature Profile

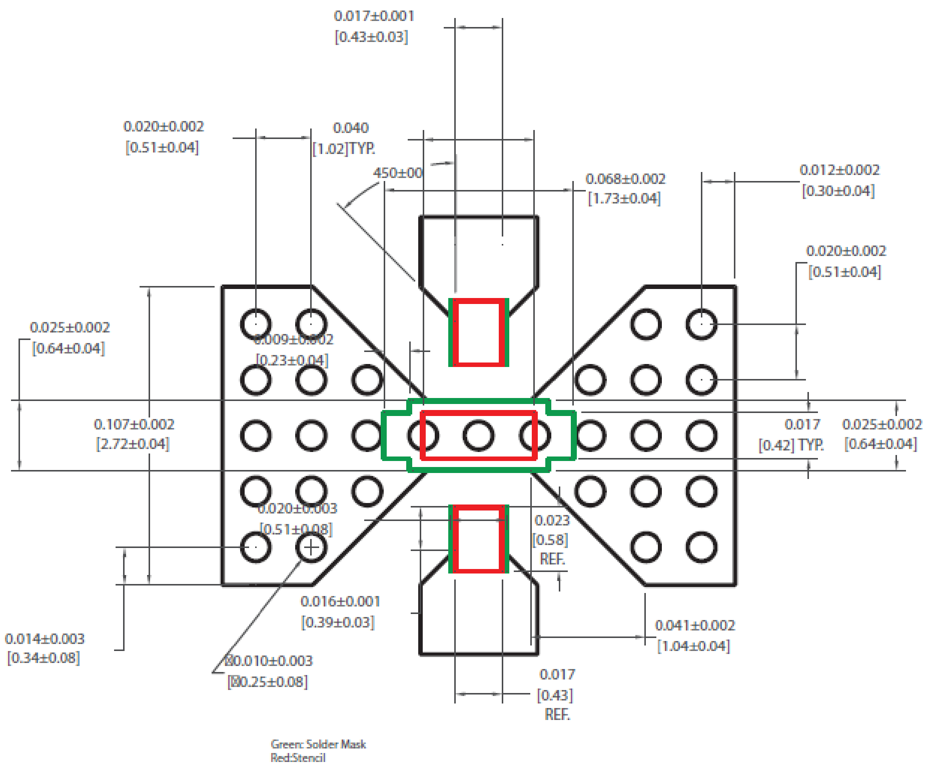


Package Outline



All dimensions shown as in [mm].
Bottom Terminal Plating: NiPdAu
Lead Frame Material: 8 mil Copper

Printed Circuit Board Layout (Soldering Footprint)[3,4,5,6,7]



3. Unless otherwise specified: Tolerance ±0.10 mm.
4. If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.
5. Solder mask should provide a 60 µm clearance between copper pad and soldermask. Rounded package pads should have matching rounded solder mask openings.
6. Use circles or squares for thermal land stencil such that there is only 50% to 80% solder paste coverage.
7. 20 mils Rogers RO4350B with 1 oz. copper clad and 10 mil diameter plated thru vias on 20 mil centers underneath package.