Features

- Higher Power SMT Switch
- Operating Frequency: 30 MHz - 5 GHz
- CW Power Handling:
  53 dBm @ +25 °C, 3.5 GHz
- Peak Power Handling:
  62 dBm @ +25 °C, 3.5 GHz
- Insertion Loss: 0.5 dB
- Return Loss: 13 dB
- Isolation: 40 dB
- T_{ON} Switching Speed: 6 μs
- Input IP3: 70 dBm
- RoHS* Compliant
- Higher Reliability Compared to Electromechanical Switches

Applications

- Aerospace and Defense
- Space

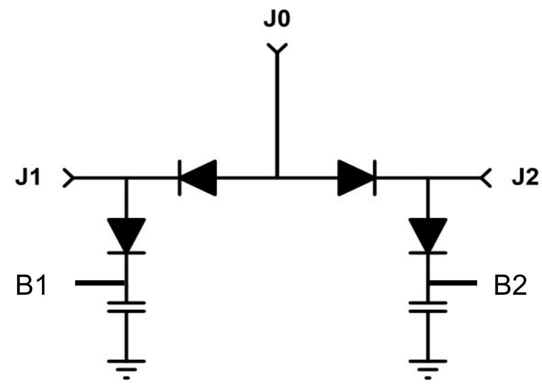
Description

The MASW-011209 is a 30 MHz - 5 GHz reflective surface mount SP2T switch that uses 5 V DC and 200 V DC positive voltage only for successful high RF power operation. This product provides an exceptional isolation to insertion loss ratio of 40 dB to 0.7 dB at 5 GHz, with 6 μs switching speed in a 20 x 10 x 3 mm BeO ceramic housing. It is ideally suited for applications requiring higher RF power surface mount switching applications.

Ordering Information

Part Number	Package
MASW-011209	Parts in Gel-Pak
MASW-011209-000SMB	Sample Test Board

Functional Schematic



Port Configuration [1]

Port Description	Function
J0	RF Input
J1	RF Output 1
J2	RF Output 2
B1	DC Bias for J1 Shunt Diode
B2	DC Bias for J2 Shunt Diode
GND	RF & DC Voltage Ground Return

1. The backside of the SP2T substrate must be directly connected to thermal, DC, and RF Ground for proper and successful operation.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: T_A = 25 °C, P_{IN} = 0 dBm, Z_0 = 50 Ω, DC Power = 5 V @ 200 mA (Insertion Loss), 200 V @ 25 mA (Isolation)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss, J0-J1 and J0-J2	1.0 GHz 2.5 GHz 4.0 GHz 5.0 GHz	dB	—	0.2 0.5 0.4 0.3	0.6 0.9 0.9 0.8
Return Loss, J0-J1 and J0-J2	1.0 GHz 2.5 GHz 4.0 GHz 5.0 GHz	dB	—	22 15 18 18	—
Isolation, J0-J1 and J0-J2	1.0 GHz 2.5 GHz 4.0 GHz 5.0 GHz	dB	52 33 35 29	65 45 44 38	—
Switching Speed (T_{ON})[3]	3.5 GHz, 10 kHz TTL repetition rate (50% Control Voltage - 90% RF Voltage)	µs	—	6	—
Switching Speed (T_{OFF})[3]	3.5 GHz, 10 kHz TTL repetition rate (50% Control Voltage - 10% RF Voltage)	µs	—	3	—
CW Incident Power[2]	3.5 GHz	dBm	—	53	—
Peak Incident Power [2]	3.5 GHz, RF pulse width = 100 µs, 5% duty cycle		—	62	—
Input IP3	F1 = 2.000 GHz, F2 = 2.010 GHz 39 dBm per tone power	dbm	—	71	—

2. Maximum source and load VSWR = 1.2:1 each.
3. Switching speed measured in commutating mode.

Nominal Operating Conditions[4,5]

Parameter	Nominal Value
CW Incident Power[2]	53 dBm @ +25 °C 52 dBm @ +55 °C 51 dBm @ +85 °C
Peak Incident Power[2] Pulse Width = 100 µs Duty Cycle = 5%	62.0 dBm @ +25 °C 61.5 dBm @ +85 °C
DC Operating Voltage & Current Bias $+V_{CC}$ $+V_{DD}$	5 ± 3% V @ 200 mA 200 ± 3% V @ 25 mA
Operating Temperature	-40 °C to +85 °C
Storage Temperature	-40 °C to +85 °C

4. Operating at nominal conditions with $T_J \le +175$ °C will ensure MTBF > 1 x 10^6 hours.
5. Maximum Source VSWR = 1.2 :1 and Load VSWR = 1.2:1

Maximum Survivability Ratings[6,7]

Parameter	Absolute Maximum
CW Incident Power[2]	53.5 dBm @ +25 °C 52.5 dBm @ +55 °C 51.5 dBm @ +85 °C
Peak Incident Power[2] Pulse Width = 100 µs Duty Cycle = 5%	62.5 dBm @ +25 °C 62.0 dBm @ +85 °C
DC Operating Voltage & Current Bias $+V_{CC}$ $+V_{DD}$	5 ± 5% V @ 250 mA 200 ± 5% V @ 40 mA
Operating Temperature	-40 °C to +85 °C
Storage Temperature	-40 °C to +85 °C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near ANY of these maximum survivability limits.

DC Bias to RF Truth Table[8]

Insertion Loss Typical Bias State = 5 V @ 200 mA, Isolation Bias Typical State = 200 V @ 25 mA

RF State	J0 Bias (V3)	J1 Bias (V1)	B1 Bias	J2 Bias (V2)	B2 Bias
J0-J1 Insertion Loss & J0-J2 Isolation	5 V @ 200 mA	0 V @ 200 mA	200 V @ 0 mA	200 V @ 25 mA	0 V @ 25 mA
J0-J2 Insertion Loss & J0-J1 Isolation	5 V @ 200 mA	200 V @ 25 mA	0 V @ 25 mA	0 V @ 200 mA	200 V @ 0 mA
J0-J1 & J0-J2 Isolation	0 V @ 0 mA	200 V @ 25 mA	0 V @ 25 mA	200 V @ 25 mA	0 V @ 25 mA

8. Current limiting resistors are required for proper DC bias operation. Suggested values for operation with the bias voltages and currents shown above and operation at 1 to 5 GHz are listed in the Evaluation Board Components table.

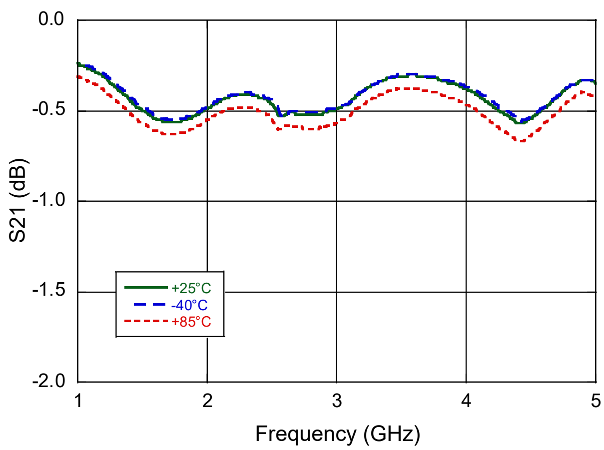
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

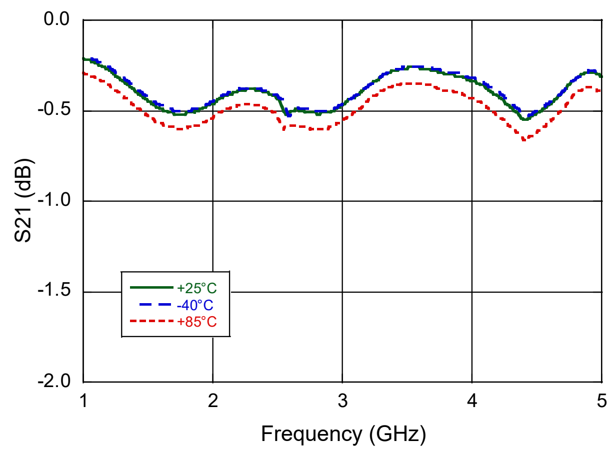
Typical Performance Curves:

S-Parameter measurements are made on switches soldered to RF evaluation boards with high power bias components in the band shown.

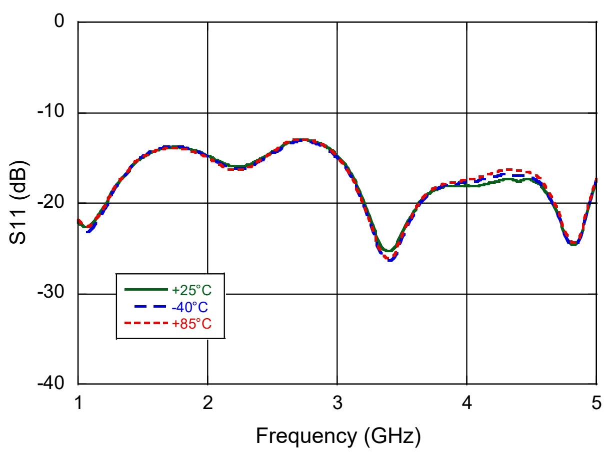
J0-J1 Insertion Loss



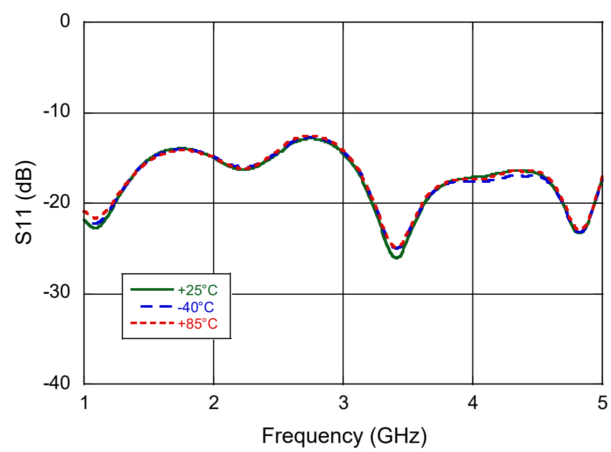
J0-J2 Insertion Loss



J0-J1 Input Return Loss

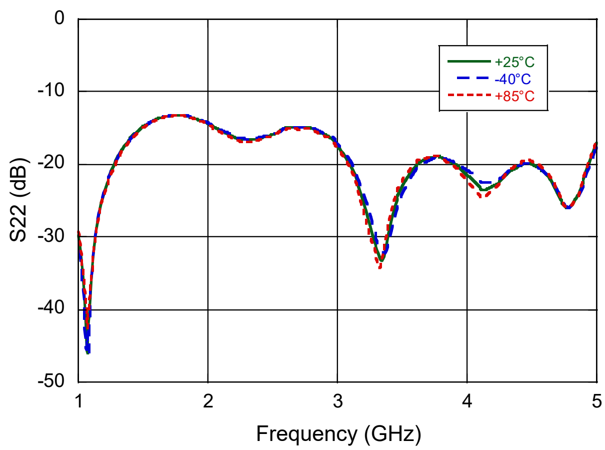


J0-J2 Input Return Loss

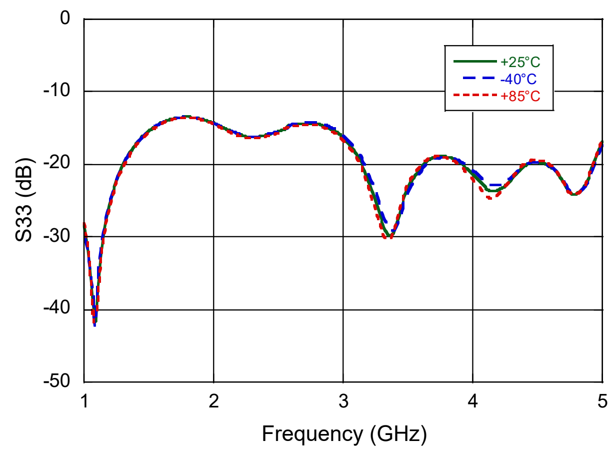


Typical Performance Curves:

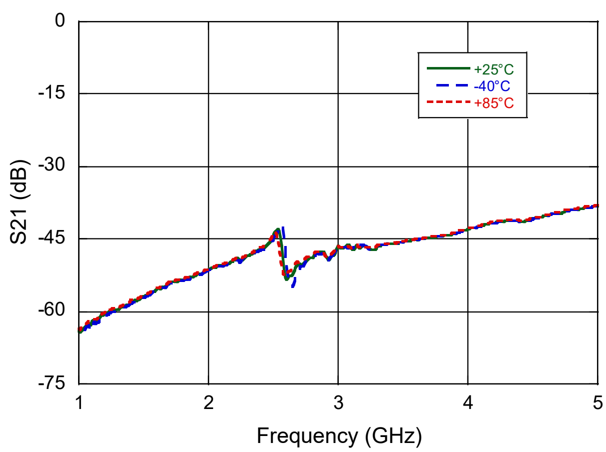
J1-J0 Output Return Loss



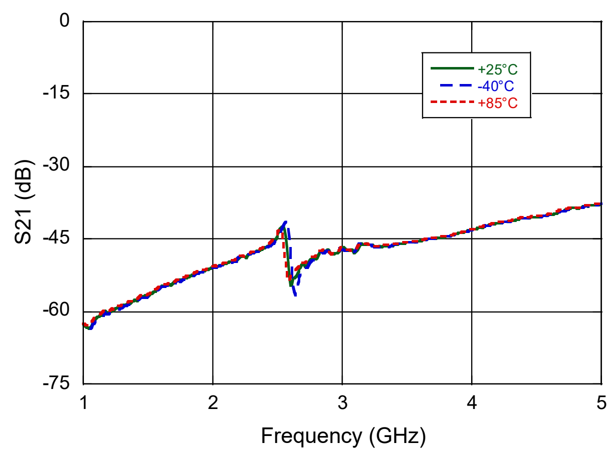
J2-J0 Output Return Loss



J0-J1 Isolation (J0-J2 in Insertion Loss)

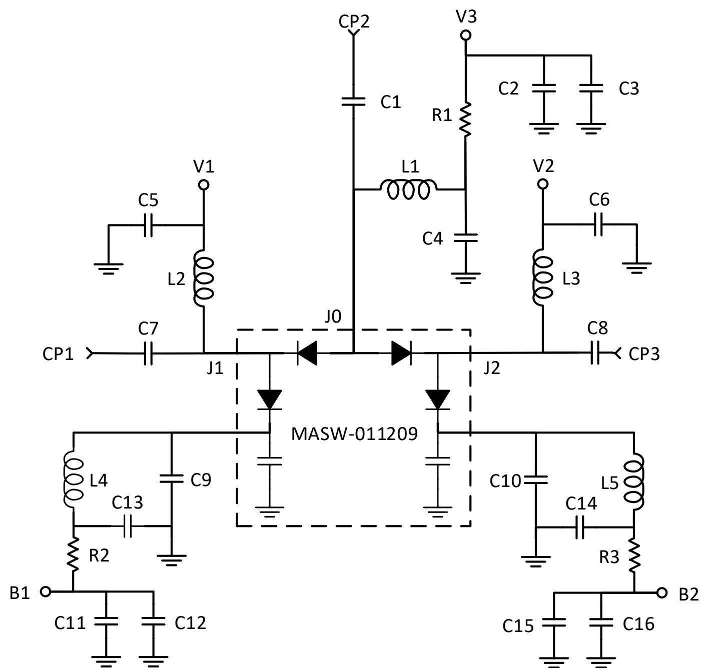


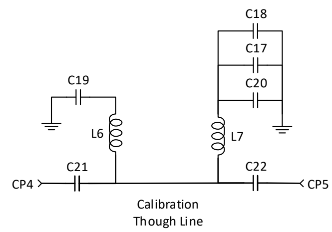
J0-J2 Isolation (J0-J1 in Insertion Loss)

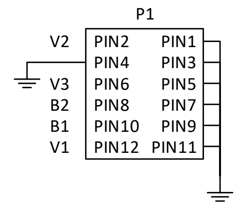


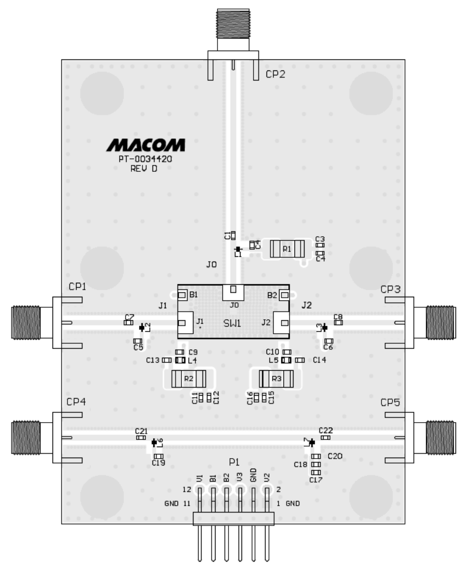
Evaluation Board

Evaluation Board Circuit Diagram and Layout









Evaluation Board Components[9]

Component	Manufacturer	Manufacturer's Part Number	Value
C1, C7, C8, C21, C22	American Technical Ceramics	600S6R8BW250XT	6.8 pF, 250 V
C2, C3, C11, C12, C15, C16, C17, C18 - C3	Wurth Elektronik	885342206006	10 nF, 250 V
C4, C5, C6, C9, C10, C13, C14, C19, C20	American Technical Ceramics	600S330FT250XT	33 pF, 250 V
L1, L2, L3	Microwave Components, Inc.	6-2538-CPAS-27-15-48	18.7 nH, air core[10]
L4, L5	Johanson Technology	LRC0603CS1N8GV001T	1.8 nH, 300 mA, 150 mΩ
R1	TE Connectivity	CRGP2512F12R	12 Ω, 2 W
R2, R3	TE Connectivity	3504G3A7K5FTDF	7.5 kΩ, 6 W

9. Suggested component values for operation 1 GHz to 5 GHz, bias conditions shown in the DC Bias to RF Truth table
10. This air core inductor is required for broadband operation. Do not substitute.

Evaluation Board Operation

The evaluation board for the MASW-011209 surface mount silicon PIN diode SP2T switch allows the exercise of this switch for small signal performance analysis, as well as for large signal operation with maximum input signal power of 40 dBm. The evaluation board includes the MASW-011209 switch, DC blocking capacitors at each RF port, current-limiting bias resistors and bias decoupling networks at each RF port which allow DC or low frequency control signals to be applied to control the state of the switch.

For the purposes of this description, State 1 is defined to be the condition in which the evaluation board is biased to produce the low insertion loss condition between ports J0 and J1 while producing isolation between ports J0 and J2. State 2 is the converse of State 1.

Four complementary control signals and one DC bias voltage are required for proper operation. All voltages are positive with respect to ground. Bias voltages are applied to the B1 (pin 10 of multi-pin connector P1) and B2 (pin 8 of P1) bias ports, as well as to the V1 (pin 12 of P1) and V2 (pin 2 of P1) RF ports to control the state of the switch. A fixed bias voltage is applied to the V3 port (connect 5 V to pin 6 of P1) for State 1 and State 2 operation.

Caution: the evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 40 dBm. The evaluation board must be connected to an adequate heat sink for large signal operation. Contact the factory for a recommended heat sink.

State 1

In State 1, the series PIN diode between the J0 and J1 ports is forward biased by applying 0 V to the V1 bias input port (pin 1 of P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the V3 bias port (pin 6 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 200 mA. At the same time, the PIN diode connected between J2 and B2 ports is also forward biased by applying a high bias voltage, nominally 200 V, to the V2 bias port (pin 2 of P1) and 0 V to the B2 bias port (pin 8 of P1).

Under this condition, the PIN diode connected between the J0 and J2 ports is reverse biased and the PIN diode connected between the J2 and B2 ports is forward biased. The magnitude of the bias current through this diode is primarily determined by the voltage applied to the V2 bias port, the magnitude of the forward voltage across the PIN diode and the resistance of R3. This current is nominally 25 mA.

The series PIN diode which is connected between the J0 and J2 ports must be reverse biased during State 1. The reverse bias voltage must be sufficiently large to maintain the diode in its non-conducting, high impedance state when large RF signal voltage may be present in the J0-to-J1 path. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the V2 bias port and the DC forward voltage of the forward biased J0-to-J1 series PIN diode.

The minimum voltage required to maintain the series diode between J0 and J2 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the series diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. Minimum control voltages for several signal frequencies are shown in the table "Minimum Reverse Bias Voltage", assuming the input power to the J0 or J1 port to be 200 W CW and the VSWR on the J0-J1 path to be 1.5:1.

Evaluation Board Operation (cont'd)

State 2

In State 2, the series PIN diode between the J0 and J2 ports is forward biased by applying 0 V to the V2 bias input port (pin 2 of P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the V3 bias port (pin 6 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 200 mA. At the same time, the PIN diode connected between J2 and B2 ports is reverse biased by applying a high bias voltage, nominally 200 V, to the B2 bias port (pin 8 of P1). A high voltage, nominally 200 V, is also applied to the V1 bias port (pin 12 of P1). Under this condition, the PIN diode connected between the J0 and J1 ports is reverse biased thus isolating the J1 RF port from the RF signal path between J0 and J2. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the V1 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode. The minimum voltage required to maintain the series diode on the J0-to-J1 side of the switch out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. The values of the reactive components which comprise the bias decoupling networks as well as the signal path DC blocking are shown in the Evaluation Board Components table.

The inductors L1, L2 and L3 were carefully selected to allow broadband operation of the switch. These components should not be replaced with inductors whose characteristics are inferior to the inductor listed in the Evaluation Board Components table.

Minimum Recommended Reverse Bias Voltage

T_A = 25°C, P_{IN} = 200 W, Z_0 = 50 Ω, VSWR = 1.5:1, Duty Cycle = 1

Signal Frequency	30 MHz	50 MHz	100 MHz	500 MHz	1 GHz	3 GHz	5 GHz
Minimum Reverse Bias Voltage	175 V	170 V	165 V	75 V	50 V	50 V	50 V

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1+\left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1+\sqrt{1+\left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

Where:

$|V_{DC}|$ = magnitude of the minimum DC reverse bias voltage
$|V_{RF}|$ = magnitude of the peak RF voltage (including the effects of the VSWR)
f_{MHz} = lowest RF signal frequency expressed in MHz
D = duty cycle of the RF signal
W_{MILS} = thickness of the diode I layer, expressed in mils (thousands of an inch)

R. Caverly and G. Hiller, —Establishing the Minimum Reverse Bias for a PIN Diode in a High Power Switch, IEEE Transactions on Microwave Theory and Techniques, Vol.38, No.12, December 1990

Outline Drawing