

MASW-007071

Rev. V7

Features

- · Operates DC 4 GHz on Single or Dual Supply
- ASIC TTL / CMOS Driver
- Low DC Power Consumption
- 50 Ω Nominal Impedance
- Test Boards are Available
- Tape & Reel are Available
- Lead-Free 4 x 6 mm PQFN Package
- RoHS* Compliant Version of SW90-0002

Applications

Wireless Infrastructure

Description

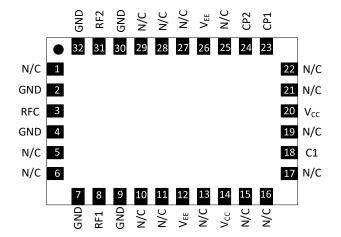
The MASW-007071 is a single pull double throw (SPDT) absorptive pHEMT switch with integral TTL driver. This device is in a PQFN plastic surface mount package. This switch offers excellent broadband performance and repeatability from DC to 4 GHz, while maintaining low DC power dissipation.

Ordering Information¹

Part Number	Package
MASW-007071-000100	Bulk Packaging
MASW-007071-0001TR	1000 piece reel
MASW-007071-0001TB	Sample Test Board

^{1.} Reference Application Note M513 for reel size information.

Block Diagram (single supply)²



Pin Configuration (single supply)²

Pin#	Function
1, 5, 6, 10, 11, 13, 15, 16, 17, 19, 21, 22, 25, 27, 28, 29	No Connection
2, 4, 7, 9, 30, 32	GND
3	RFC
8	RF1
12, 26	V_{EE}
14, 20	V _{CC}
18	C1
23	CP1
24	CP2
31	RF2

^{2.} See functional schematic for dual supply operation.

^{*} Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



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Electrical Specifications: Freq. = DC - 4 GHz, T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Insertion Loss	RFC - RF1, RF2 (Logic per truth table)	dB		_	1.8
Isolation	RF1 - RF2 (All Logic "0")	dB	30	_	_
VSWR	On (RFC,RF1, RF2), (Logic per truth table) Off (RF1, RF2), (Logic per truth table)	Ratio	_	_	2.0:1 1.8:1
1 dB Compression	50 MHz 0.5 - 4.0 GHz	dBm	_	18 29	_
Input IP ₃	Two-tone inputs up to +5 dBm 50 MHz 0.5 - 4.0 GHz	dBm		36 46	_
Switching Speed	T_{ON} (50% Control to 10% RF) T_{OFF} (50% Control to 90% RF) T_{RISE} (10% to 90% RF) T_{FALL} (90% to 10% RF)	ns		31 19 6 2	_
V _{CC}	_	V	4.5	5.0	5.5
Input Voltage	LOW-level (V _{IL}) HIGH-level (V _{IH})	V	0.0 2.0	_	0.8 5.0
L _{IN} (Input Leakage Current)	$V_{IN} = V_{CC}$ or GND	μA	-1.0	_	1.0
I _{cc} ³	V _{CC} min. to max., Logic "0" or "1"	mA	_	5	12
Turn-on Current⁴	For guaranteed start-up	mA	_	_	125
ΔI _{CC} (Additional Supply Current Per TTL Input Pin)	V _{CC} = max., Vcntrl = V _{CC} - 2.1 V	mA	_	_	1.0
Switching Noise	Generated from DC-DC Converter with recommended capacitors, 3.5 MHz	dBm	_	-93	_
Thermal Resistance θ _{JC}		°C/W		15	

^{3.} During turn-on, the device requires an initial start up current (I_{CC}) specified as "Turn-on Current". Once operational, I_{CC} will drop to the

specified levels.

4. The DC-DC converter is guaranteed to start in 100 µs as long as the power supplies have the maximum turn-on current available for



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Absolute Maximum Ratings^{5,6}

Parameter	Absolute Maximum
Input Power 0.05 GHz 0.5 - 4.0 GHz ⁷	27 dBm 34 dBm
V _{CC}	-0.5 V ≤ V _{CC} ≤ +6.0 V
V _{IN} ⁸	$-0.5 \text{ V} \le \text{V}_{\text{IN}} \le \text{V}_{\text{CC}} + 0.5 \text{ V}$
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- 7. When the ŔF input is applied to the terminated port, the absolute maximum power is +30 dBm.
- 8. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Truth Table (Switch)

Control Innut	Condition of the Switch		
Control Input	RF Common to each RF Port		
C1	RF1	RF2	
"0" = TTL Low	Off	On	
"1" = TTL High	On	Off	

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

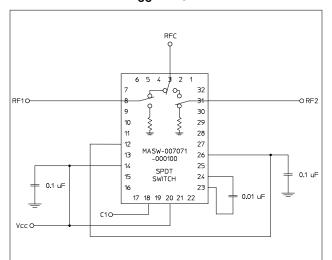


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Functional Schematics:

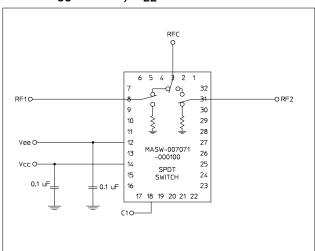
Single Supply Operation $V_{CC} = +5 \text{ V}$



Pin#	Function
1, 5, 6, 10, 11, 13, 15, 16, 17, 19, 21, 22, 25, 27, 28, 29	No Connection
2, 4, 7, 9, 30, 32	GND
3	RFC
8	RF1
12, 26	V_{EE}
14, 20	V _{cc}
18	C1
23	CP1
24	CP2
31	RF2

- V_{EE} is internally generated and must remain isolated from external power supplies. Generated noise is typical of switching DC-DC Converters.
- 10. Connections and external components shown in functional schematic are required. Capacitors (0.1 μ F) need to be located near pins 20 & 26.
- The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages).

Dual Supply Operation^{11,12} $V_{CC} = +5 \text{ V}, V_{EE} = -3.3 \text{ V to } -8 \text{ V}$



Pin#	Function
1, 5, 6, 10, 11, 13, 15, 16, 17, 19 - 29	No Connection
2, 4, 7, 9, 30, 32	GND
3	RFC
8	RF1
12	V _{EE}
14	V _{CC}
18	C1
31	RF2

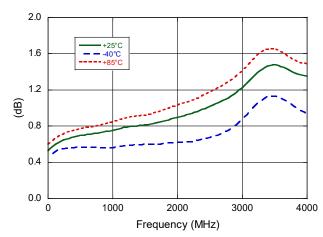
12. Dual Supply Operation will eliminate the start-up current mentioned in note 3. It will also eliminate spurious signals caused by the DC-DC converter that are present in single supply operation.



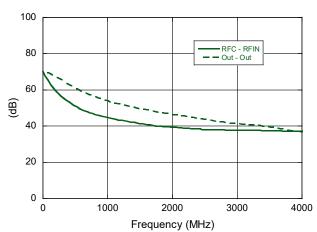
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Typical Performance Curves

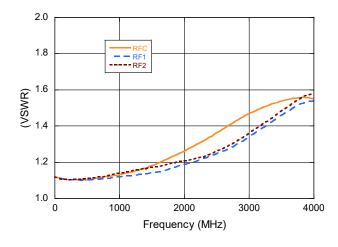
Insertion Loss



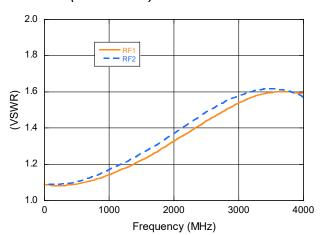
Isolation



On VSWR



Off VSWR (Terminations)

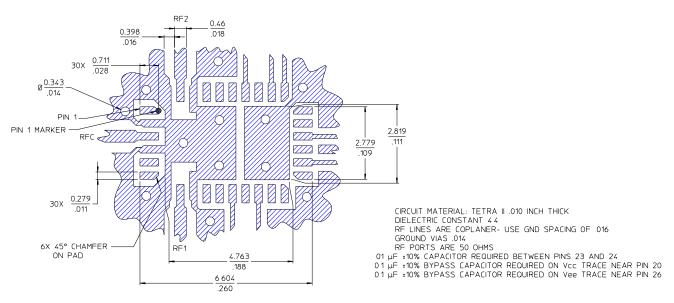




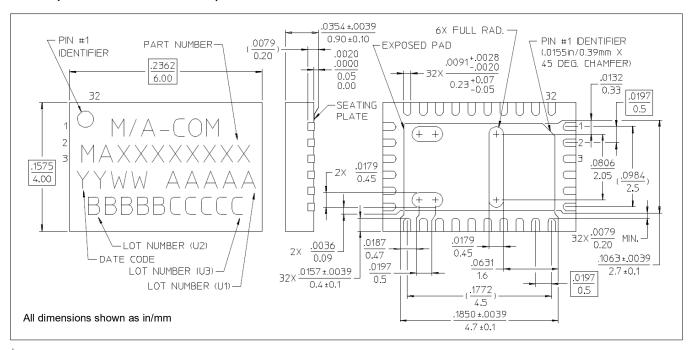
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Recommended PCB Configuration



CSP-1, Lead-Free 4 x 6 mm, 32-lead PQFN[†]



Reference Application Note M538 for lead-free solder reflow recommendations. Reference Application Note S2083 for PCB footprint information.



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