

Features

- Saturated Power: 300 W
- Drain Efficiency: 75%
- Small Signal Gain: 23 dB
- Lead-Free Air Cavity Ceramic Package
- RoHS* Compliant

Applications

- Avionics - TACAN, DME, IFF
- Military Radio
- L-Band Radar
- Electronic Warfare
- ISM
- General Amplification

Description

The MAPC-A3001 is a 300 W packaged, unmatched transistor utilizing a high performance, GaN on SiC production process. This transistor supports both defense and commercial related applications.

Offered in a thermally-enhanced flange package, the MAPC-A3001 provides superior performance under CW operation allowing customers to improve SWaP-C benchmarks in their next generation systems.

Typical RF Performance:

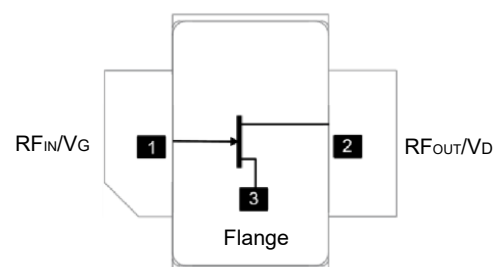
- Pulse width of 100 μ sec and 10% duty, $P_{IN} = 35$ dBm, $V_{DS} = 50$ V, $I_{DQ} = 400$ mA, $T_C = 25^\circ\text{C}$

Frequency (GHz)	Output Power (dBm)	Gain (dB)	η_D (%)
1.2	55.1	20.1	68.8
1.3	54.9	19.9	71.2
1.4	54.6	19.6	67.1



AC-230B-2

Functional Schematic



Pin Configuration

Pin #	Pin Name	Function
1	RF_{IN} / V_G	RF Input / Gate
2	RF_{OUT} / V_D	RF Output / Drain
3	Flange ¹	Ground / Source

1. The flange on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	MOQ Increment
MAPC-A3001-AB000	Bulk
MAPC-A3001-ABSB1	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

RF Electrical Characteristics: in Evaluation Fixture

Freq. = 1.2 - 1.4 GHz, $T_C = 25^\circ\text{C}$, $V_{DS} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$, Pulse Width = 100 μs , Duty Cycle = 10%
Performance in MACOM Evaluation Test Fixture, 50 Ω system

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Output Power	Pulsed, $P_{IN} = 35\text{ dBm}$	P_{OUT}	-	300	-	dBm
Drain Efficiency	Pulsed, $P_{IN} = 35\text{ dBm}$	DE	-	73	-	%
Large Signal Gain	Pulsed, $P_{IN} = 35\text{ dBm}$	G_P	-	20	-	dB
Small Signal Gain	CW, $P_{IN} = -20\text{ dBm}$	S21	-	23.6	-	dB
Input Return Loss	CW, $P_{IN} = -20\text{ dBm}$	S11	-	-13.6	-	dB
Output Return Loss	CW, $P_{IN} = -20\text{ dBm}$	S22	-	-6	-	dB
Output Mismatch Stress	All Phase Angles	ψ	VSWR = 10:1, No Device Damage			

RF Electrical Specifications: in Production Test Fixture

Freq. = 1.3 GHz, $P_{IN} = 35\text{ dBm}$, $T_A = 25^\circ\text{C}$, $V_{DS} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$,
Pulse Width = 100 μs , Duty Cycle = 10%

Note: Final testing and screening for all transistor sales is performed using the MAPC-A3001-AB production test fixture at 1.3 GHz.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Output Power	Pulsed, $P_{IN} = 35\text{ dBm}$	P_{OUT}	250	300	-	W
Drain Efficiency	Pulsed, $P_{IN} = 35\text{ dBm}$	η	68	72.0	-	%
Power Gain	Pulsed, $P_{IN} = 35\text{ dBm}$	G_P	18	20.0	-	dB

DC Electrical Characteristics $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Drain-Source Leakage Current	$V_{GS} = -8\text{ V}$, $V_{DS} = 10\text{ V}$	I_{DLK}	-	-	3.6	mA
Gate-Source Leakage Current	$V_{GS} = -8\text{ V}$, $V_{DS} = 10\text{ V}$	I_{GLK}	-3.6	-	-	mA
Gate Threshold Voltage	$V_{DS} = 10\text{ V}$, $I_D = 25.6\text{ mA}$	V_T	-3.5	-2.7	-1.9	V
Gate Quiescent Voltage	$V_{DS} = 50\text{ V}$, $I_D = 400\text{ mA}$	V_{GSQ}	-	-2.3	-	V

Thermal Characteristics

Parameter	Symbol	Test Conditions	Units	Rating
Operating Junction Temperature	T_J	CW, $P_{DISS} = 100\text{ W}$, $T_C = 85.0^\circ\text{C}$	$^\circ\text{C}$	223
Thermal Resistance, Junction to Case	$R_{\theta JC}$		$^\circ\text{C/W}$	1.38

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
Drain-Source Voltage	150 V
Gate Voltage	-8 +2 V
Drain Current	24.5 A
Gate Current	25.6 mA
Input Power	39 dBm
Storage Temperature	-65°C to +150°C
Mounting Temperature	+245°C
Junction Temperature ^{3,4,5}	+275°C
Operating Temperature	-40°C to +85°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.
3. Mounting temperature for 30 seconds.
4. Operating at nominal conditions with $T_J \leq +225^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.

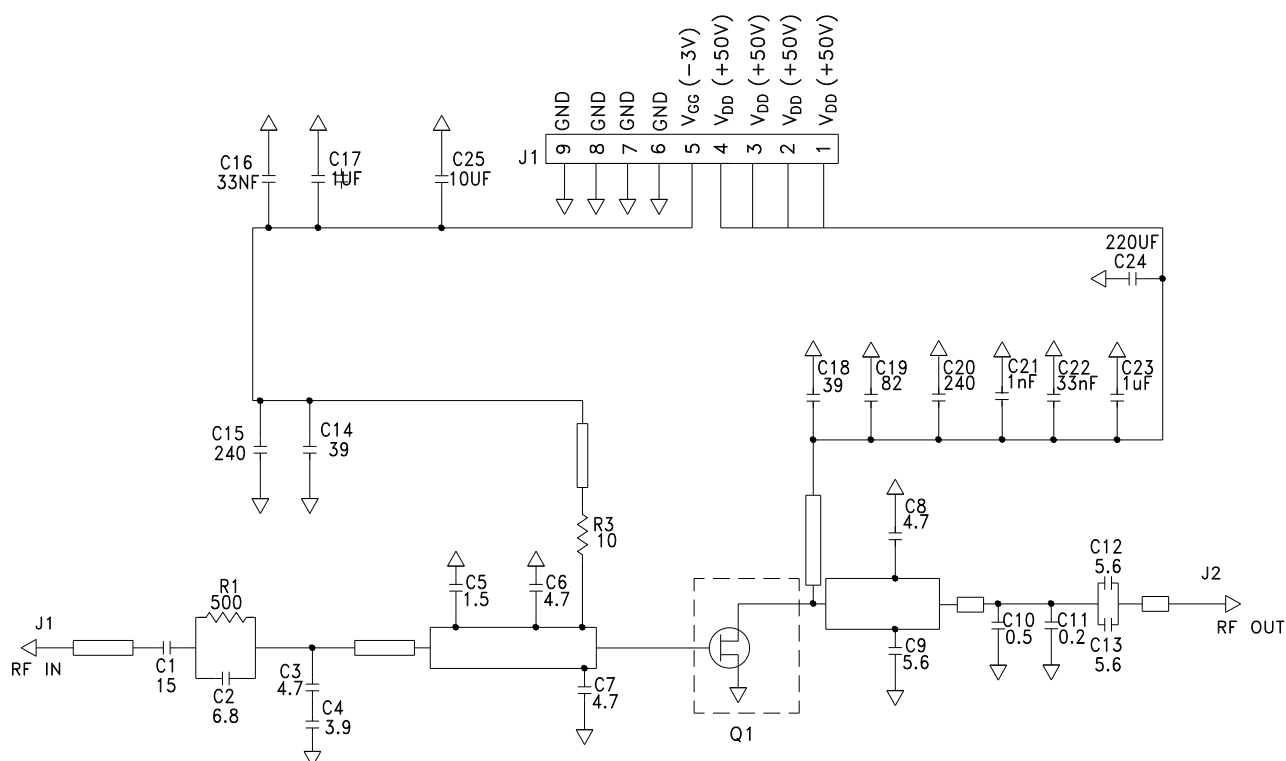
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Evaluation Test Fixture and Recommended Tuning Solution, 1.2 - 1.4 GHz



NOTE: UNITS ARE pF, OHM AND nH UNLESS OTHERWISE SPECIFIED

Description

Parts measured on evaluation board (20-mil thick RO4350B). Matching is provided using a combination of lumped elements and transmission lines as shown in the simplified schematic above. Recommended tuning solution component placement, transmission lines, and details are shown on the next page.

Biasing Sequence

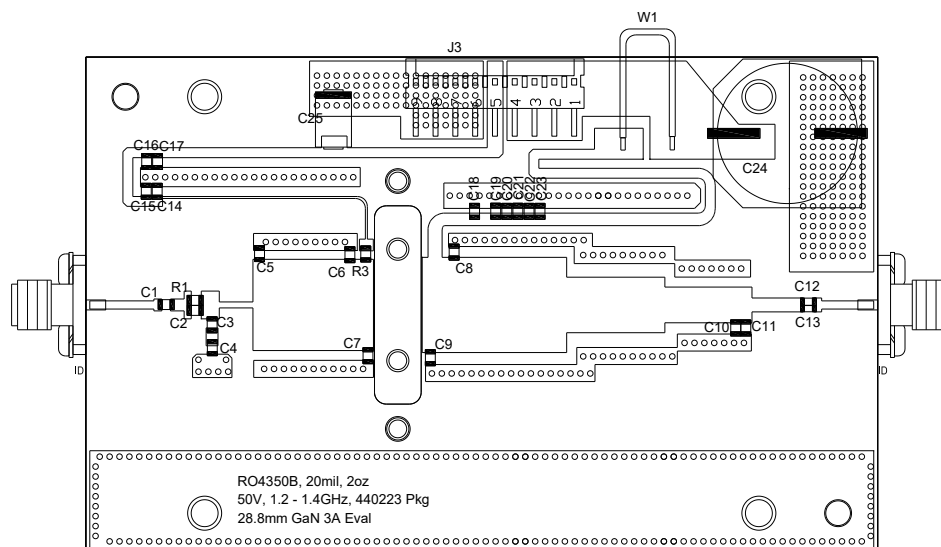
Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

1. Turn RF off
2. Apply pinch-off voltage of -5 V to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Evaluation Test Fixture and Recommended Tuning Solution, 1.2 - 1.4 GHz



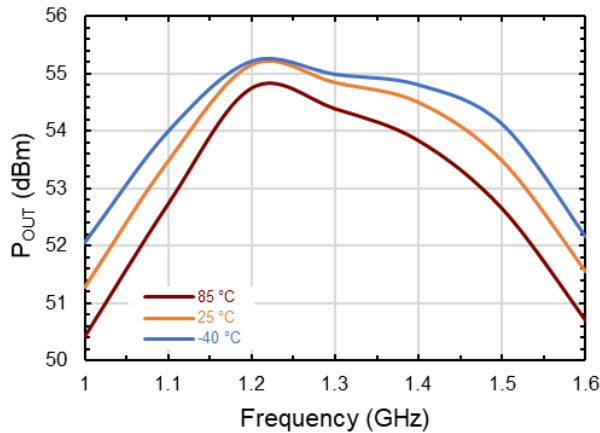
Assembly Parts List

Ref Des	Description	Manufacturer	Manufacturer PN	Qty
C1	15 pF 0805in T5% 125C 250V	Kyocera AVX	600F150JT250XT	1
C2	6.8 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F6R8BT250XT	1
C3, C6, C7, C8	4.7 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F4R7BT250XT	4
C4	3.9 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F3R9BT250XT	1
C5	1.5 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F1R5BT250XT	1
C9	5.6 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F5R6BT250XT	1
C12, C13	5.6 pF 0805in T0.1p 125C 250V (Mount Vertically)	Kyocera AVX	600F5R6BT250XT	2
C10	0.5 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F0R5BT250XT	1
C11	0.2 pF 0805in T0.1p 125C 250V	Kyocera AVX	600F0R2BT250XT	1
C14, C18	39 pF 0805in T2% 125C 250V	Kyocera AVX	600F390GT250XT	2
C15, C20	240 pF 0805in T1% 125C 250V	Kyocera AVX	600F241JT250XT	2
C16, C22	0.033 μ F 0805in T10% 125C	Murata	GRM21BR72A333KA01	2
C17, C23	1 μ F 0805in T10% 125C 100V	Murata	GCM21BC72A105KE36	2
C19	82 pF 0805in T5% 125C 250V	Kyocera AVX	600F820JT250XT	1
C21	1 nF 0603in T10% 125C 100V	Murata	GRM188R72A102KA01	1
C24	220 μ F, +/-20%, 100V, ELECTROLYTIC, CASE SIZE K21	Panasonic	ECA-2AHG221	1
C25	10 μ F TC2312in T10% 16V 125C	Kyocera AVX	TAJC106M016RNJ	1
R1	499 Ω 0805in T1% 155C 1/8W	Yageo	RC0805FR-07499RL	1
R3	10 Ω 0805in T5% 155C 1/8W	Yageo	RC0805FR-0710RL	1
W1	12 AWG 3.0" Wire			1
J1, J2	SMA, PANEL MOUNT , FLANGE, 4-HOLE, BLUNT POST	AMPHENOL CONNEX	132150	2
J3	HEADER RT>PLZ .1CEN LK 9POS	TE Connectivity	640457-9	1
Q1	MAPC-A3001-AB GaN Amplifier			1

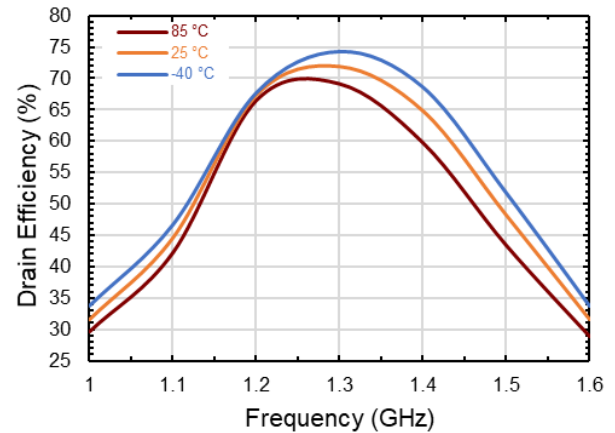
Typical Performance Curves as Measured in the 1.2– 1.4 GHz Evaluation Test Fixture

Pulsed 100 μ sec/10%, $P_{in} = 35$ dBm, $V_{DS} = 50$ V, $I_{DQ} = 400$ mA, Frequency = 1.3 GHz (Unless Otherwise Noted)
For Engineering Evaluation Only – This data does not Modify MACOM's Datasheet Limits.

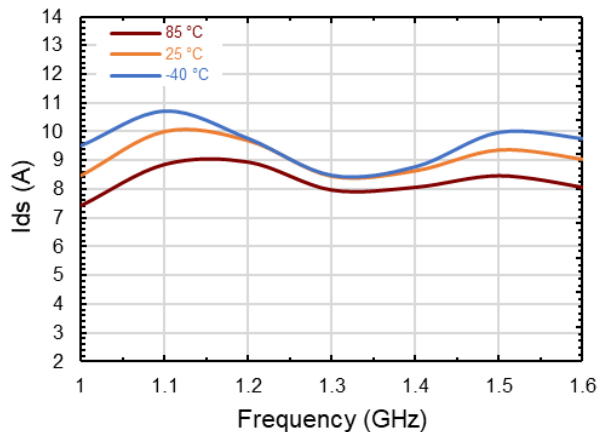
Output Power vs. Temperature and Frequency



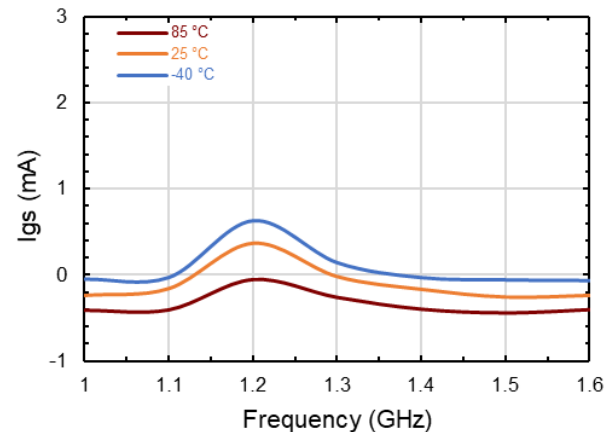
Drain Efficiency vs. Temperature and Frequency



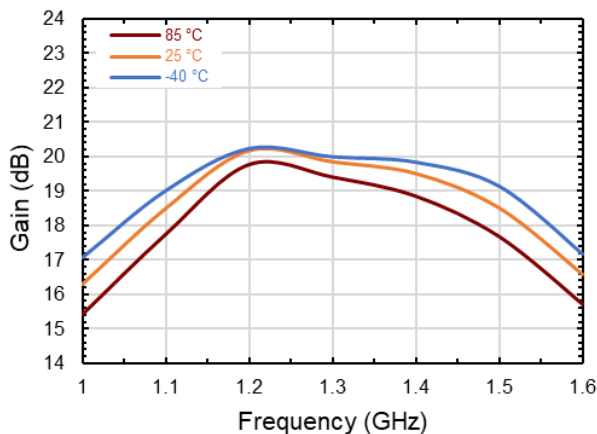
Drain Current vs. Temperature and Frequency



Gate Current vs. Temperature and Frequency



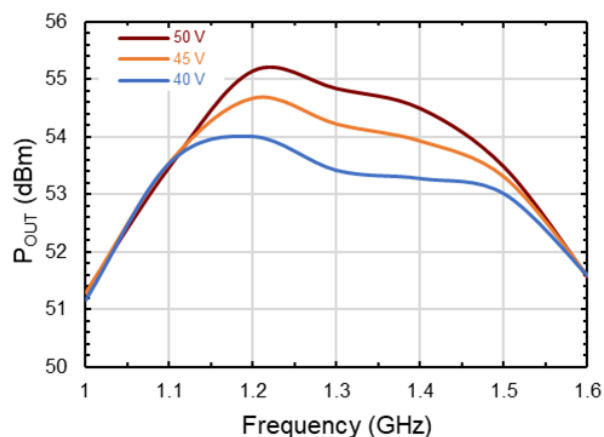
Large Signal Gain vs. Temperature and Frequency



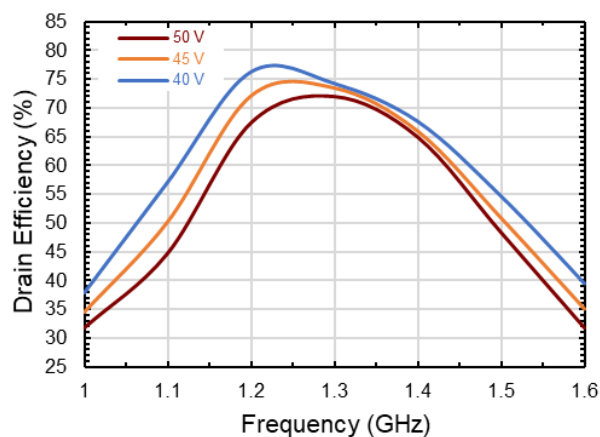
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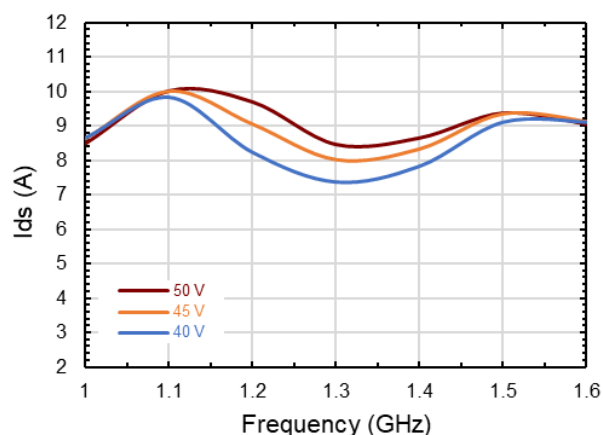
Output Power vs. V_{DS} and Frequency



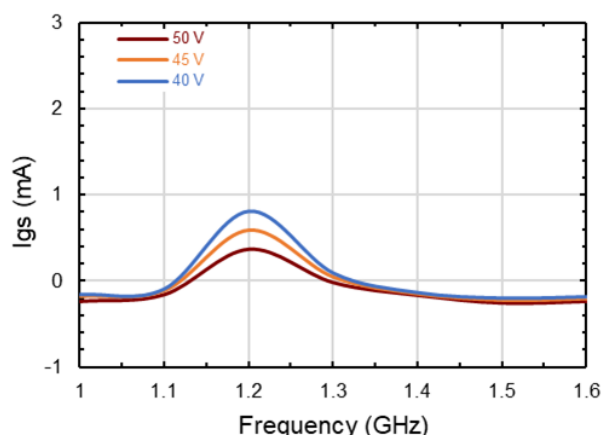
Drain Efficiency vs. V_{DS} and Frequency



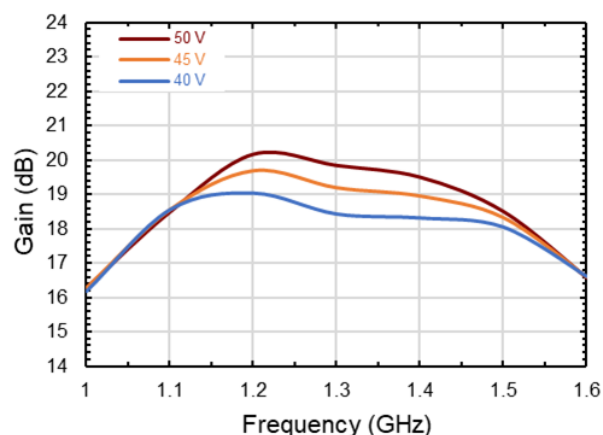
Drain Current vs. V_{DS} and Frequency



Gate Current vs. V_{DS} and Frequency



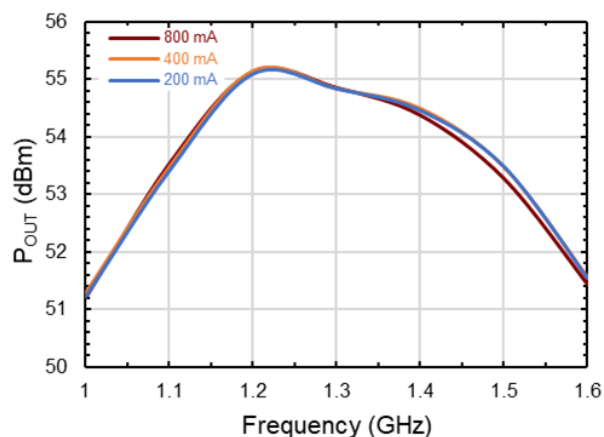
Large Signal Gain vs. V_{DS} and Frequency



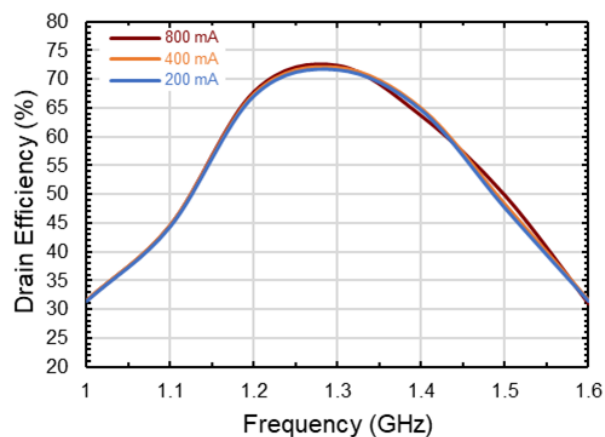
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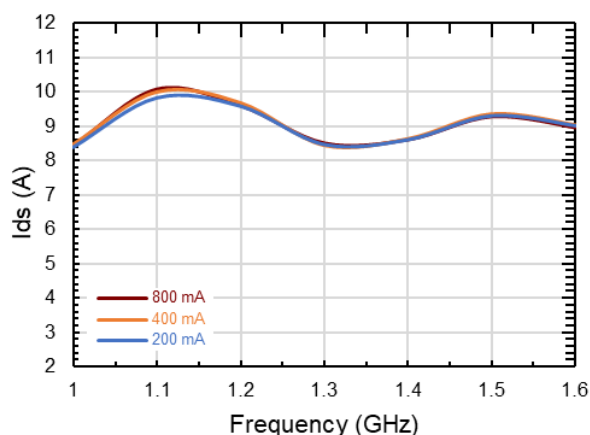
Output Power vs. I_{DQ} and Frequency



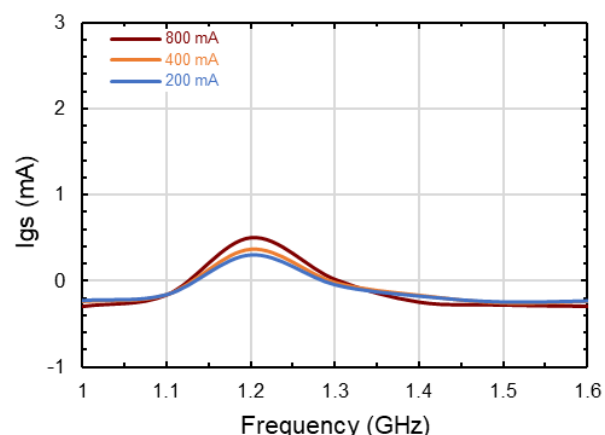
Drain Efficiency vs. I_{DQ} and Frequency



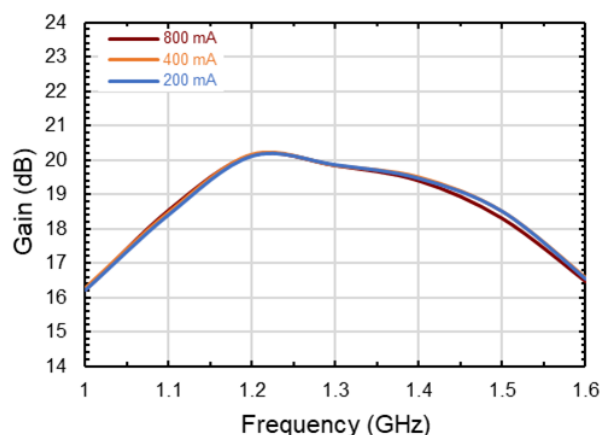
Drain Current vs. I_{DQ} and Frequency



Gate Current vs. I_{DQ} and Frequency



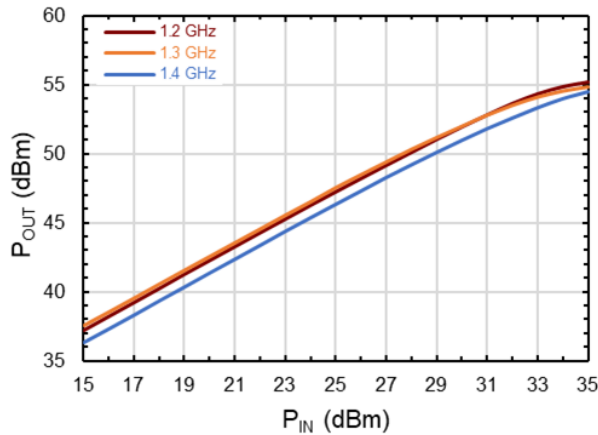
Large Signal Gain vs. I_{DQ} and Frequency



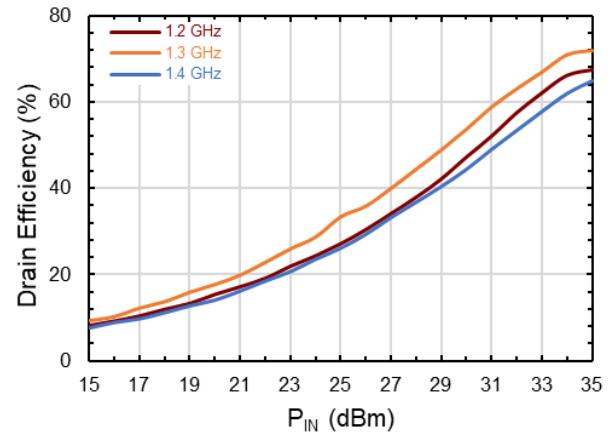
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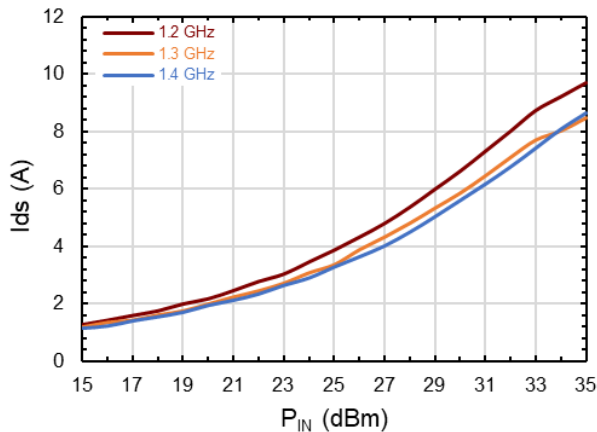
Output Power vs. Frequency and P_{IN}



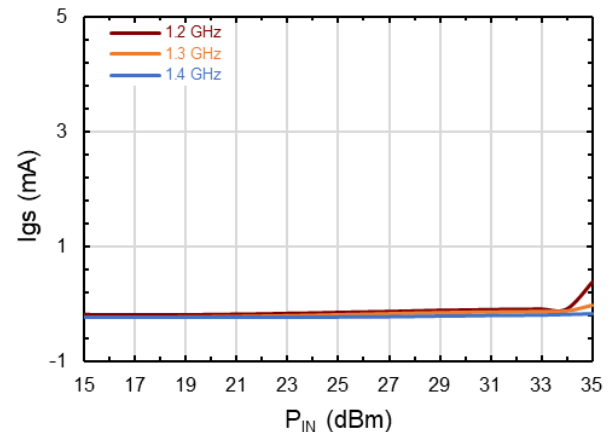
Drain Efficiency vs. Frequency and P_{IN}



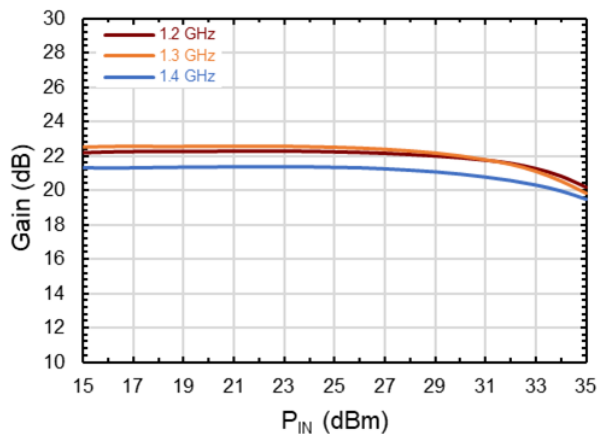
Drain Current vs. Frequency and P_{IN}



Gate Current vs. Frequency and P_{IN}



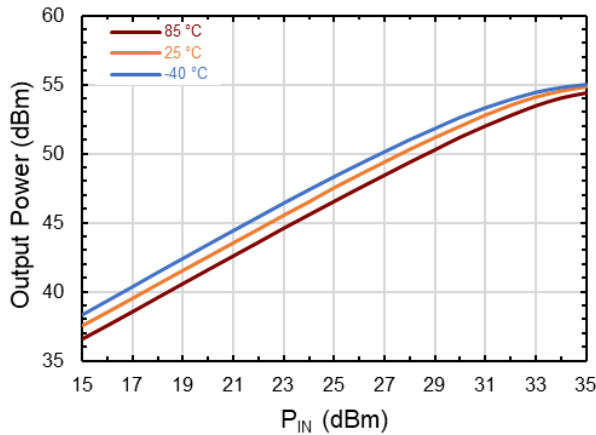
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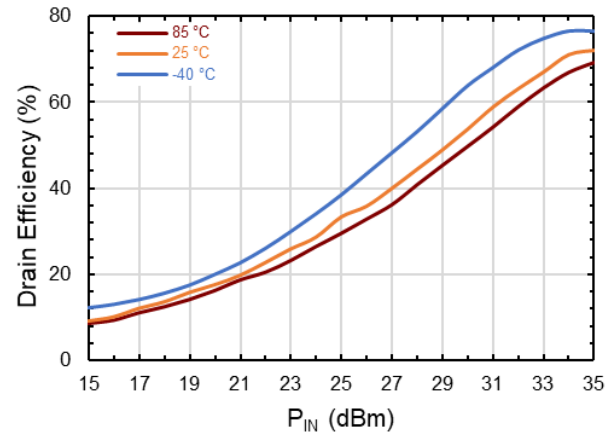
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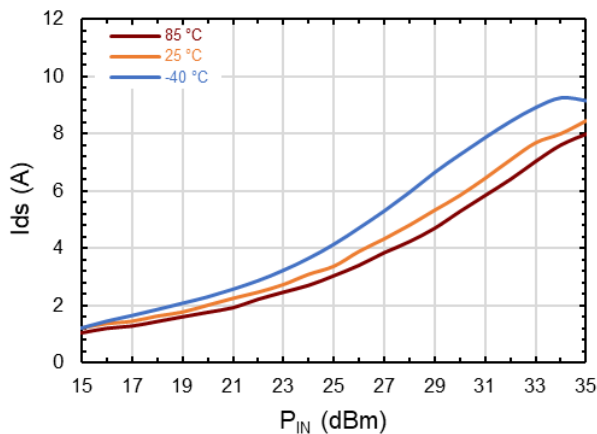
Output Power vs. Temperature and P_{IN}



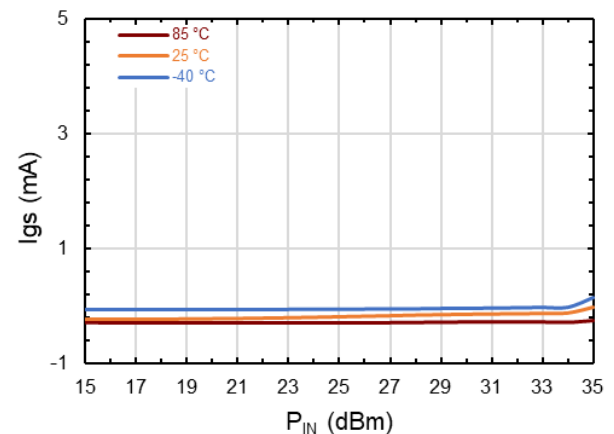
Drain Efficiency vs. Temperature and P_{IN}



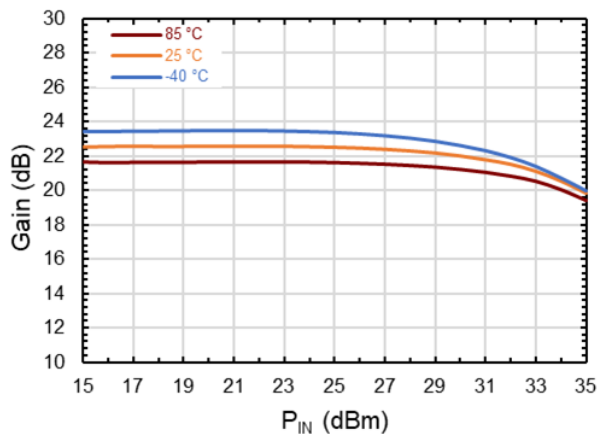
Drain Current vs. Temperature and P_{IN}



Gate Current vs. Temperature and P_{IN}



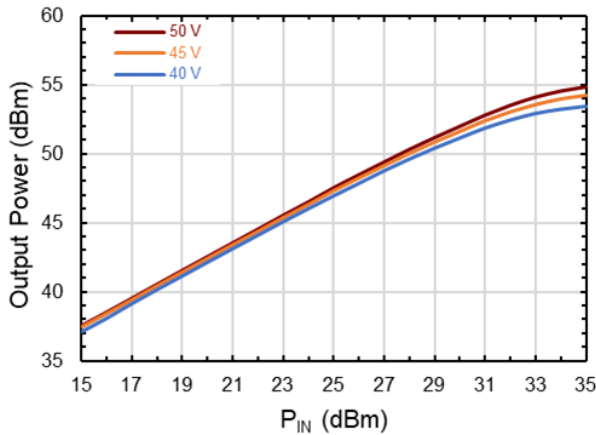
Large Signal Gain vs. Temperature and P_{IN}



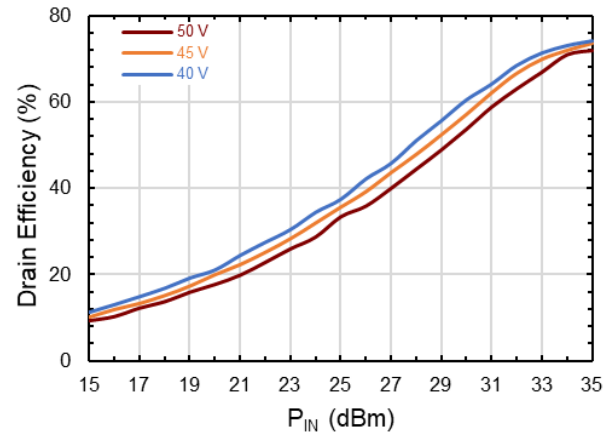
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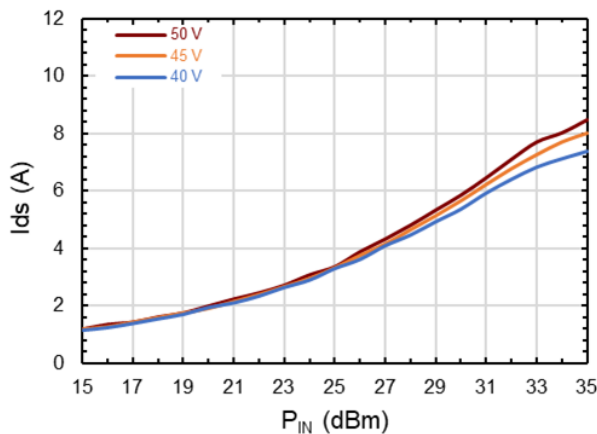
Output Power vs. V_{DS} and P_{IN}



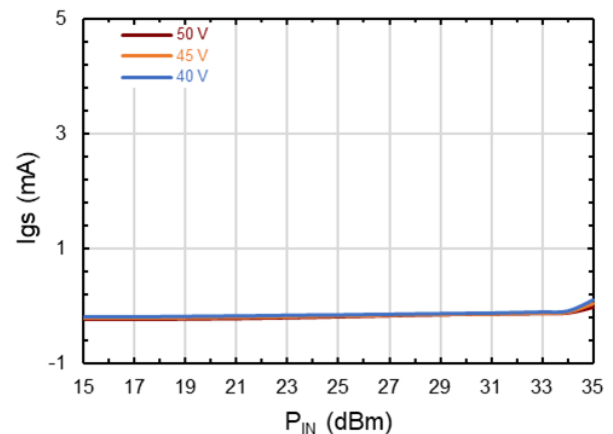
Drain Efficiency vs. V_{DS} and P_{IN}



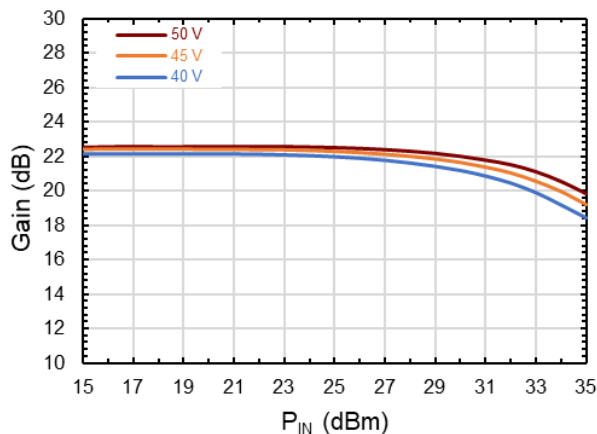
Drain Current vs. V_{DS} and P_{IN}



Gate Current vs. V_{DS} and P_{IN}



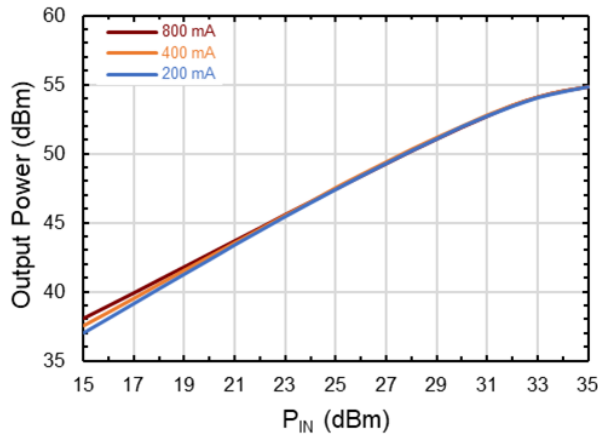
Large Signal Gain vs. V_{DS} and P_{IN}



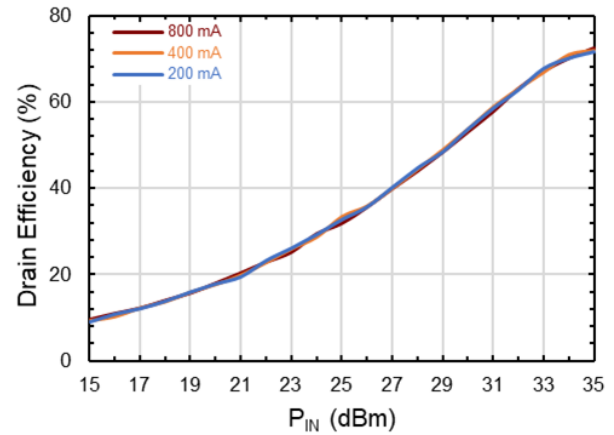
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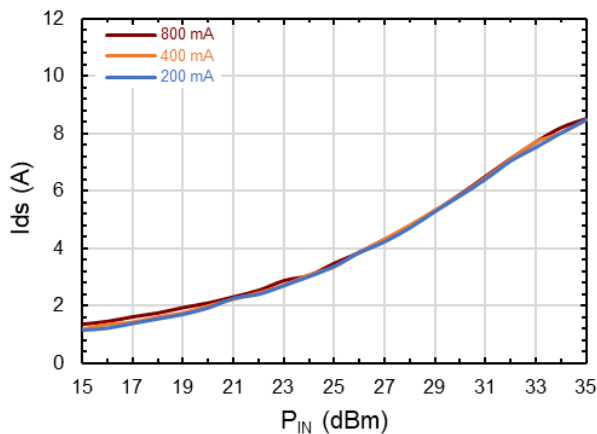
Output Power vs. I_{DQ} and P_{IN}



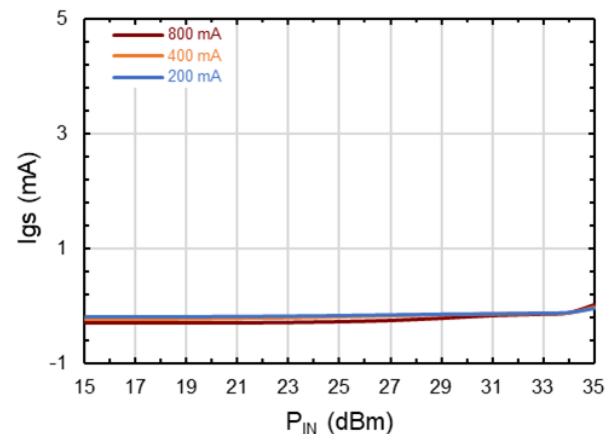
Drain Efficiency vs. I_{DQ} and P_{IN}



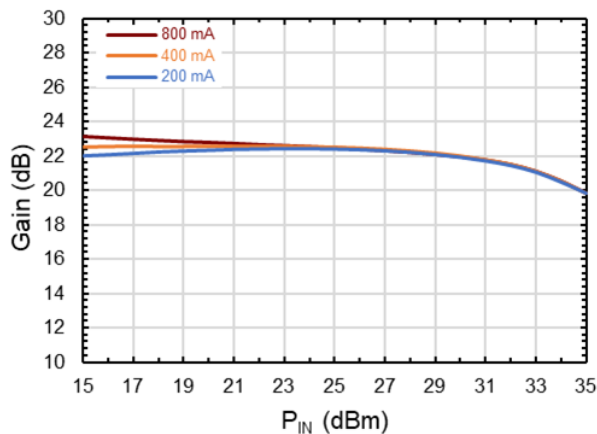
Drain Current vs. I_{DQ} and P_{IN}



Gate Current vs. I_{DQ} and P_{IN}



Large Signal Gain vs. I_{DQ} and P_{IN}

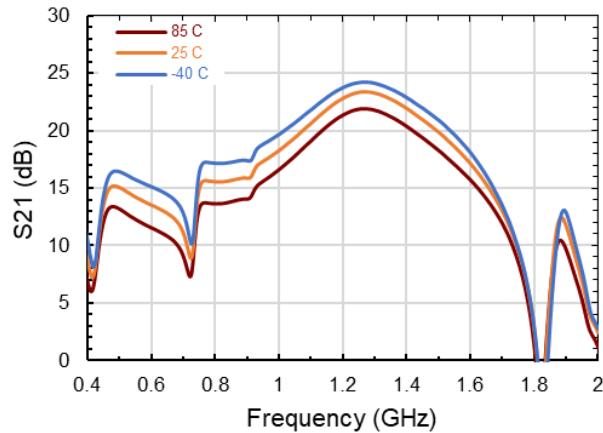


Typical Performance Curves as Measured in the 1.2 - 1.4 GHz Evaluation Test Fixture:

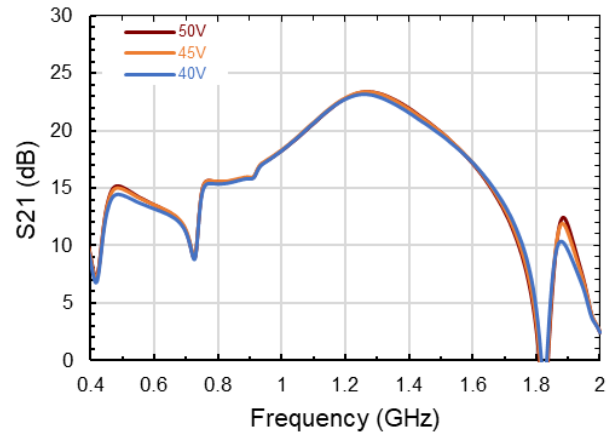
CW, $V_{DS} = 50V$, $I_{DQ} = 400$ mA, $P_{in} = -20$ dBm

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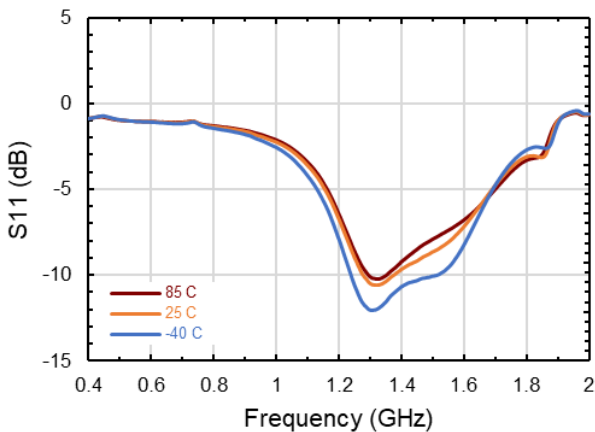
S₂₁ vs Frequency and Temperature



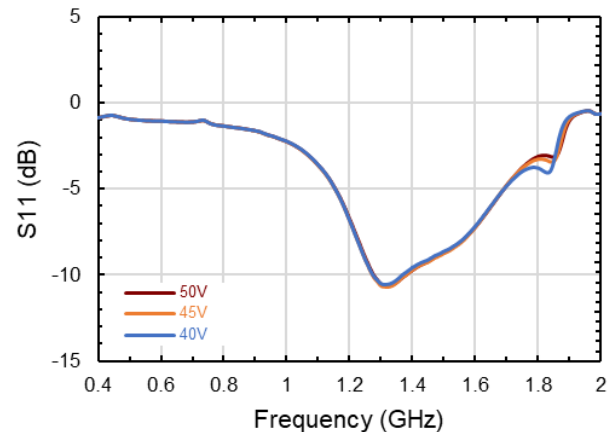
S₂₁ vs Frequency and V_{DS}



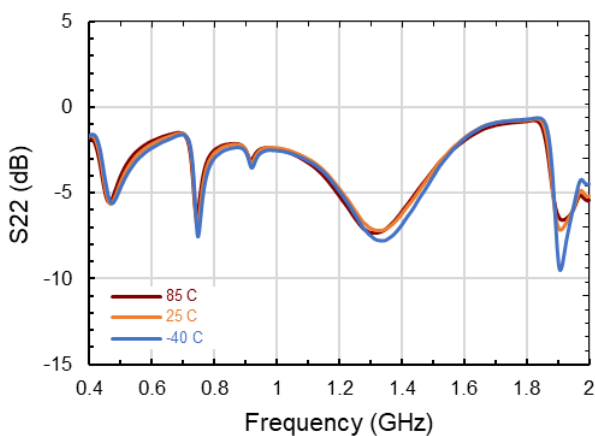
S₁₁ vs Frequency and Temperature



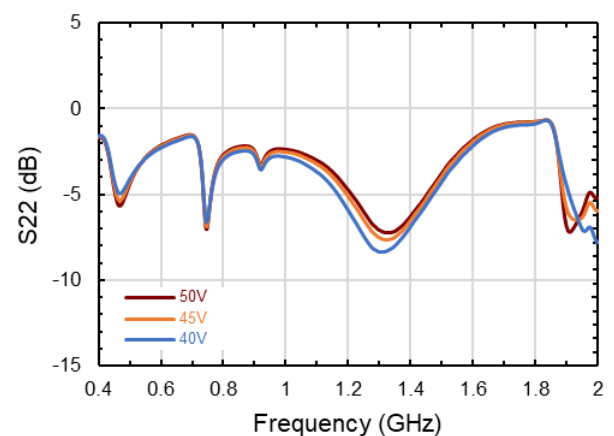
S₁₁ vs Frequency and V_{DS}



S₂₂ vs Frequency and Temperature



S₂₂ vs Frequency and V_{DS}

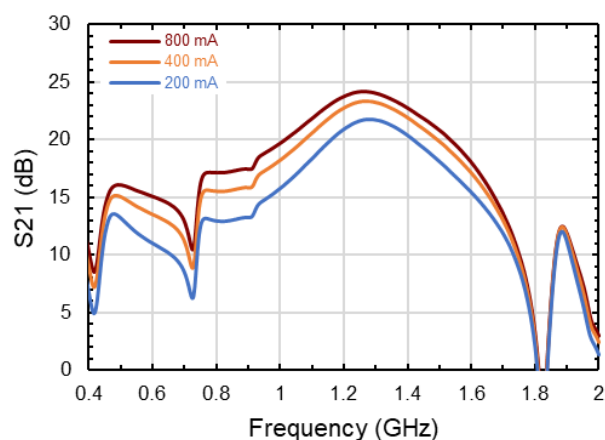


Typical Performance Curves as Measured in the 1.2 - 1.4 GHz Evaluation Test Fixture:

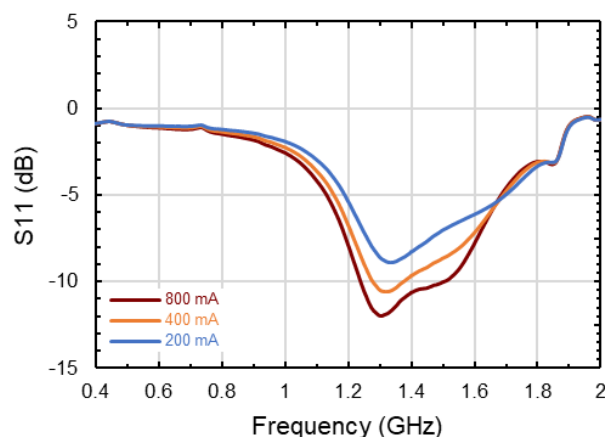
CW, $V_{DS} = 50V$, $I_{DQ} = 400\text{ mA}$, $P_{in} = -20\text{ dBm}$

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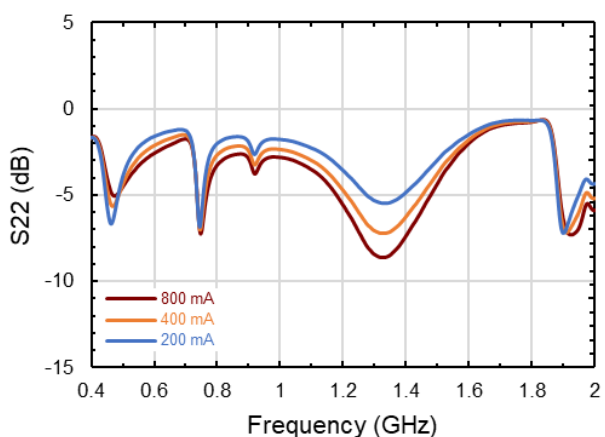
S₂₁ vs Frequency and I_{DQ}



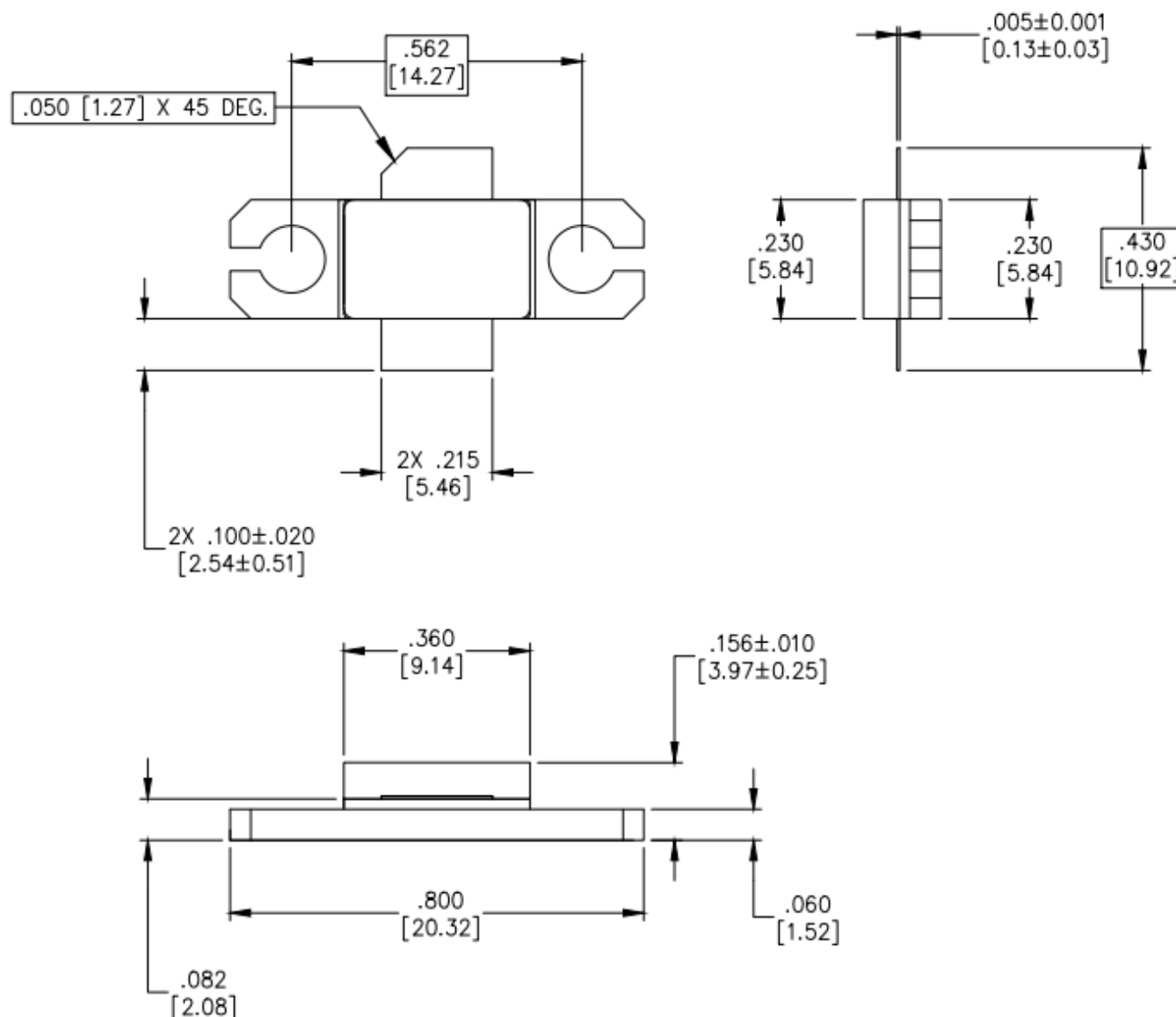
S₁₁ vs Frequency and I_{DQ}



S₂₂ vs Frequency and I_{DQ}



AC-360B-2 Package Dimensions



NOTES:

1. ALL DIMENSIONS SHOWN AS in[mm]. CONTROLLING DIMENSIONS ARE IN in AND CONVERTED mm DIMENSIONS ARE NOT NECESSARILY EXACT.
2. ALL TOLERANCES ARE $\pm .005 [0.13]$ UNLESS OTHERWISE NOTED
3. LEAD FINISH: AU
FLANGE FINISH: AU
4. LID SEAL EPOXY MAY FLOW OUT A MAXIMUM OF $.020 [0.51]$ FROM EDGE OF LID
5. LID MAY BE MIS-ALIGNED UP TO $.010 [0.25]$ FROM PACKAGE IN ANY DIRECTION

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