Features

- High Power Switch and 2-Stage LNA with Integrated DC converter and Switch Driver
- Bypass Switch on Second LNA Stage
- High RF Input Power, TX mode
  Up to 80 W CW Power Handling @ +100ºC
- Gain, RX High Gain Mode: 37 dB @ 1.8 GHz
  34 dB @ 2.7 GHz; 31 dB @ 3.5 GHz
- Gain, RX Low Gain Mode: 19 dB @ 1.8 GHz
  20 dB @ 2.7 GHz; 19 dB @ 3.5 GHz
- Noise Figure, RX Mode: 1.1 dB @ 1.8 GHz
  1.4 dB @ 2.7 GHz; 1.7 dB @ 3.5 GHz
- Fast Switching Speed 350 ns
- +5 V DC Supply only
- Compatible with 1.8 V and 3.3 V logic
- Lead-Free 6 mm 40-Lead HQFN Package
- RoHS* Compliant

Applications

- High Power TDD 4G and 5G Base Stations
- Wireless Infrastructure
- TDD based Communication System

Description

The MAMF-011150 is a highly integrated compact surface mount module containing a PIN diode high power SPDT switch and 2-stage LNA with a 5 V power management chip in a 6 mm 40-lead HQFN plastic package.

The device features high power handling, high isolation at Tx mode, and high gain, low noise figure RX mode. It has an integrated bias controller utilizing a boost circuit. The switch portion requires only a single 5 V supply, and a single TX / RX control signal that is 1.8/3.3 V logic compatible.

The 2-stage LNA has an additional bypass feature for the second stage and has a separate Enable pin which can be used independently or tied to the VCTRL pin on the board for simple TX/RX switching.

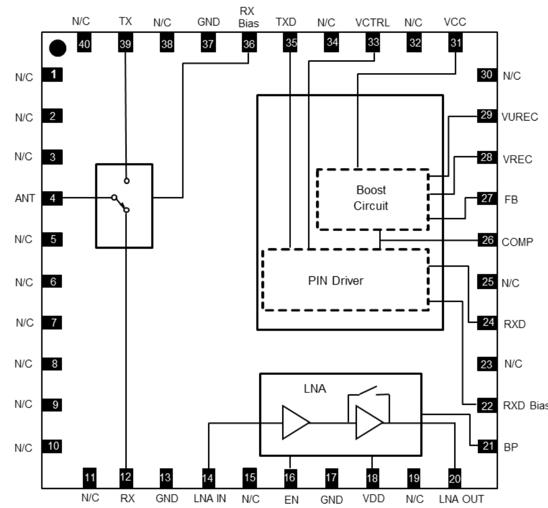
Ordering Information[1]

Part Number	Package
MAMF-011150-TR1000	1000 piece reel
MAMF-011150-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Functional Schematic



Pin Configuration[2]

Pin #	Pin Name	Description
1-3, 5-11, 15, 19, 23, 25, 30, 32, 34, 38, 40	N/C	Internally No Connect
13, 17, 37	GND	Ground
4	ANT	RF Input
12	RX	SWITCH RX Output
14	LNA IN	LNA Input
16	EN	LNA Enable Pin
18	VDD	LNA Supply
20	LNA OUT	LNA output
21	BP	Bypass switch control
22	RXD Bias	RX shunt Driver Output
24	RXD	RX Series Driver Output
26	COMP	DC-DC Comp
27	FB	DC-DC Feedback
28	VREC	DC-DC Boost Voltage
29	VUREC	DC-DC VUREC
31	VCC	Switch 5V Supply
33	VCTRL	T/R Logic Signal
35	TXD	TX Driver Output
36	RX Bias	RX Shunt Bias
39	TX	TX Output/Bias
41	Paddle[3]	Ground

2. MACOM recommends connecting unused package pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC & thermal ground.

Electrical Specifications: T_A= +25°C, V_{CC} = V_{DD} = 5 V, Z_0 = 50 Ω, TX State: ANT to TX ON, VCTRL = EN = 1.8 V, RX State: ANT to LNA OUT ON, VCTRL = EN = 0 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Input RF Power @ +100°C ANT to TX ON	1.8 GHz, 2.7 GHz, 3.5 GHz	W	—	80	—
Switch Insertion Loss ANT to TX ON	1.8 GHz 2.7 GHz 3.5 GHz	dB	—	0.3 0.4 0.5	— 0.7 —
Input and Output Return Loss ANT to TX ON	1.8 GHz 2.7 GHz 3.5 GHz	dB	—	23 20 21	—
Noise Figure in Both Modes ANT to LNA OUT	1.8 GHz 2.7 GHz 3.5 GHz	dB	—	1.1 1.4 1.7	—
Gain in High Gain Mode ANT to LNA OUT	1.8 GHz 2.7 GHz 3.5 GHz	dB	— 30 —	37 34 31	—
Gain in Low Gain Mode ANT to LNA OUT	1.8 GHz 2.7 GHz 3.5 GHz	dB	— 17.5 —	19 20 19	—
Isolation ANT to RX	Switch State = ANT to TX ON	dB	—	50	—
Output IP3 in High Gain Mode ANT to LNA OUT	P_{OUT} = +10 dBm per tone, 11 MHz spacing	dBm	—	32	—
Output IP3 in Low Gain Mode ANT to LNA OUT	P_{OUT} = +3 dBm per tone, 11 MHz spacing	dBm	—	27	—
Output P1dB in High Gain Mode	ANT to LNA OUT	dBm	—	19	—
Output P1dB in Low Gain Mode	ANT to LNA OUT	dBm	—	13	—
V_{DD} Bias Current (LNA)	High Gain Mode Low Gain Mode	mA	—	108 44	—
Logic Control Voltage	Logic High Logic Low	V	1.2 0	—	3.45 0.6
Logic Input Current	Logic High Logic Low	µA	—	60 0.01	—
RX mode V_{CC} Supply Current [4]	—	mA	—	102	—
TX mode V_{CC} Supply Current [4]	—	mA	—	150	—

4. The average current for the switch is set with external resistors. The resistor values can be adjusted higher to reduce the V_{CC} average current.

TX/RX Switch Bias Table

ANT - TX	ANT - RX	VCTRL
ON	OFF	High
OFF	ON	Low

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Parameter	Rating	Standard
Human Body Model (HBM)	Class 1B	ESDA/JEDEC JS-001
Charged Device Model (CDM)	Class C3	ESDA/JEDEC JS-002

LNA Logic Truth Table[5]

Mode	EN	BP	Note
RX Mode, High Gain	Low	Low	LNA1 and LNA2 ON, Bypass Switch OFF
RX Mode, Low Gain	Low	High	LNA1 ON, LNA2 OFF, Bypass Switch ON
TX Mode, High Isolation	High	Low	LNA1 and LNA2 OFF, Bypass Switch OFF
TX Mode, Low Isolation	High	High	LNA1 and LNA2 OFF, Bypass Switch ON

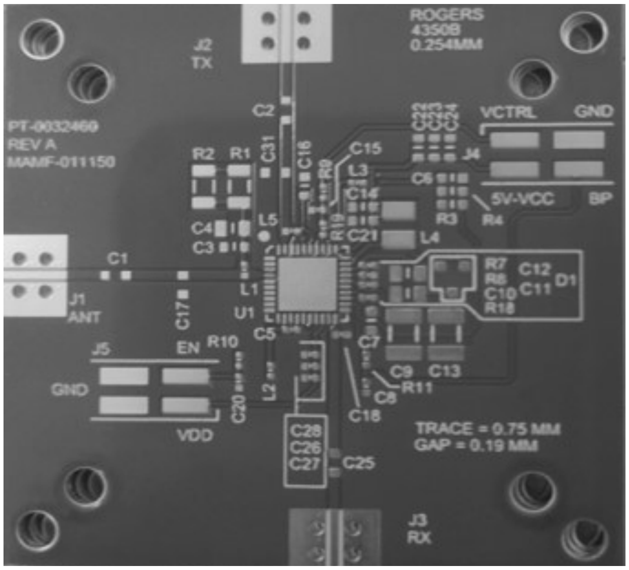
5. If V_{DD} pin is used to turn the LNAs ON and OFF, the logic pins need to stay at Logic Low during V_{DD} ramp up and ramp down.

Absolute Maximum Ratings[6,7,8]

Parameter	Absolute Maximum
RF Input Power ANT to RX LNA to LNA OUT ANT to TX ON	48 dBm CW 19 dBm 50 dBm CW @ +100°C, 3.5 GHz
DC Voltages: V_{CC}, V_{DD} VCTRL, EN, BP	-0.5 to +5.5 V -0.3 to 3.6 V
Junction Temperature Switch[8] LNA[8,9]	+175°C +150°C
Case (Paddle) Temperature	-40°C to +120°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $T_J \leq +150°C$ (LNA) and $T_J \leq +175°C$ (Switch) will ensure MTTF >> 1 x 10^6 hours.
9. LNA Junction Temperature (T_J) = $T_C + \Theta_{JC}*(P_{DISS})$ where P_{DISS} is the total DC & RF dissipated power.
   - LNA: Typical thermal resistance (Θ_{JC}) = 33.4 ºC/W.

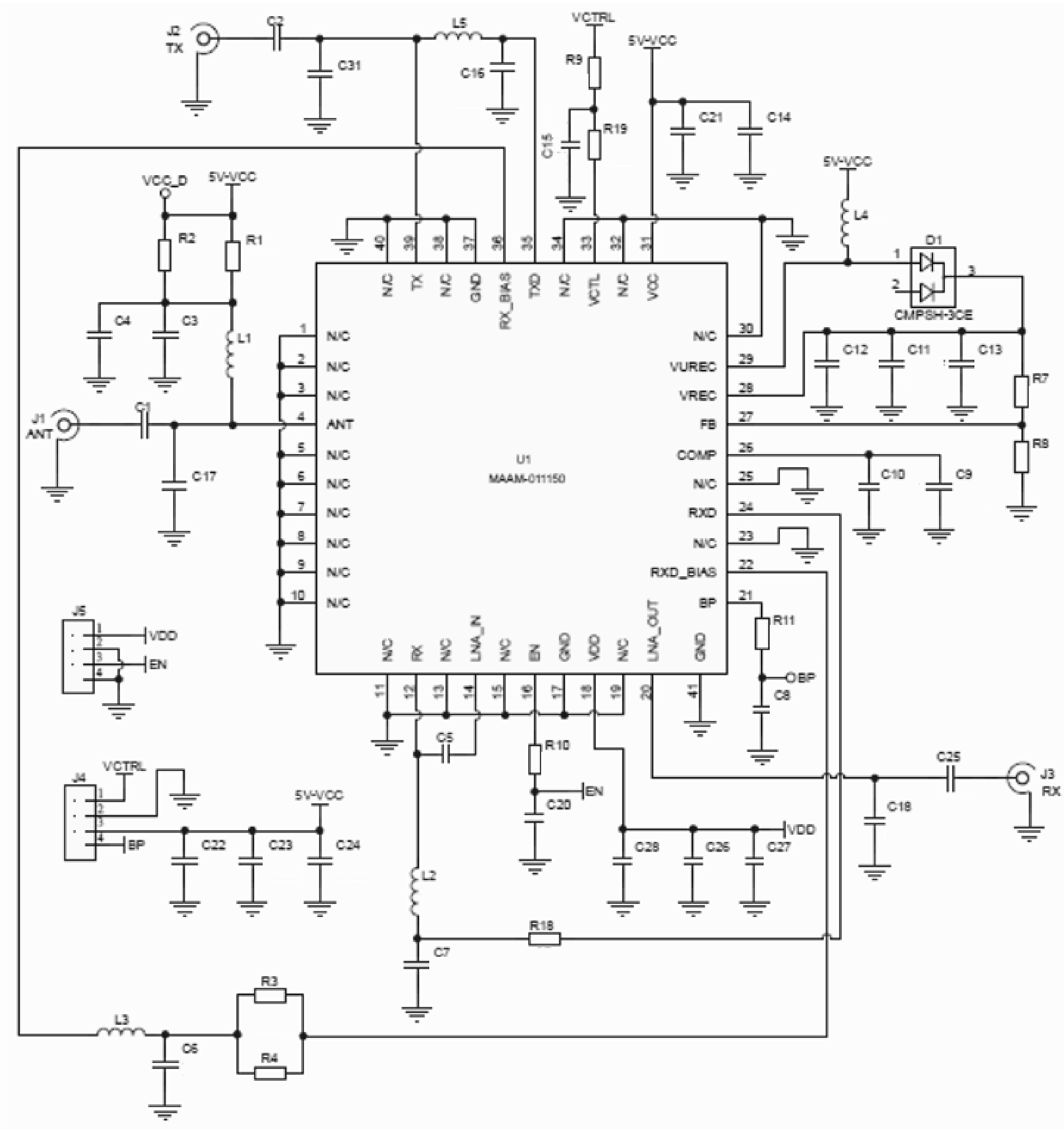
PCB Layout



Parts List

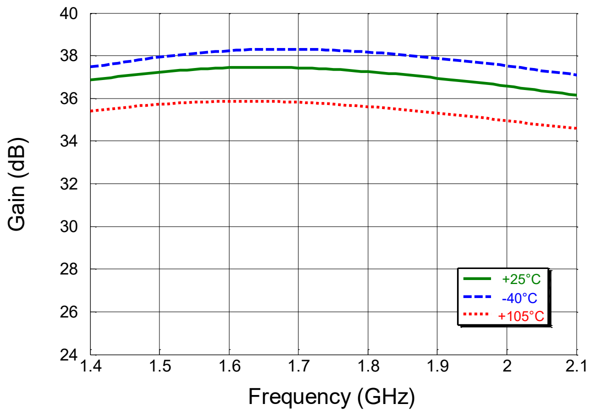
Part	Value	Case Style (Min Rating)
C1,C2,C25	27 pF	0603
C3,C7,C16	1 nF	0603 (≥100V)
C4	1 µF	0805
C5	10 pF	0402
C6	100 pF	0603 (≥100V)
C8,C17,C18,C19	DNP	0402
C9,C13	2.2 µF	1210
C10	470 pF	0402
C11	100 nF	0805
C12	10 nF	0805
C14,C24	10 µF	0603
C15	10 pF	0402
C20	4.7 pF	0402
C21,C22,C23	10 nF	0603
C26,C27	10 nF	0402
C28	0.1 µF	0402
C31	0.1 pF	0603
L1,L2	33 nH	0402
L3	10 nH	0402
L4	10 µH	2.5 x 2 mm
L5	47 nH	0402
R1,R2	69.8 Ω	1206 (≥0.25W)
R3,R4	3.6 kΩ	0603 (≥0.2W)
R7	1.6 MΩ	0402
R8	115 KΩ	0402
R9,R10,R19	100 Ω	0402
R11,R18	0 Ω	0402
D1	CMPSH-3CE TR	750mA/40V/155ºC SOT23

Application Schematic

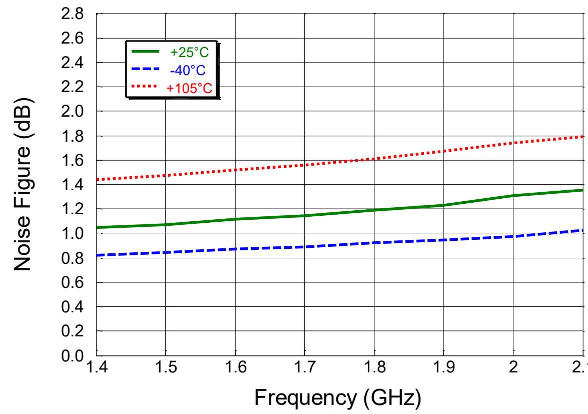


RX High Gain mode. Typical Performance Curves mode. P_{IN} = -30 dBm, $V_{CC} = V_{DD}$ = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

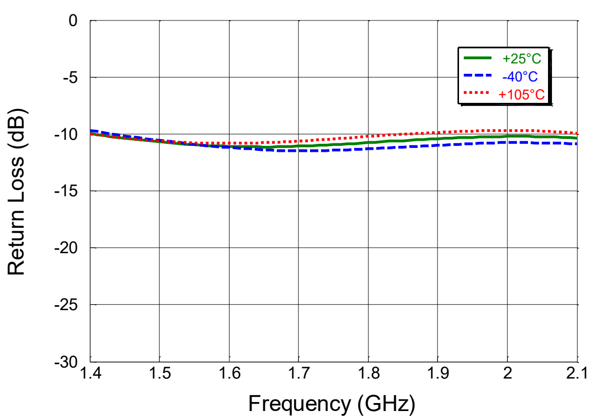
LNA Gain over swept Frequency (& Temp.) in High Gain Mode



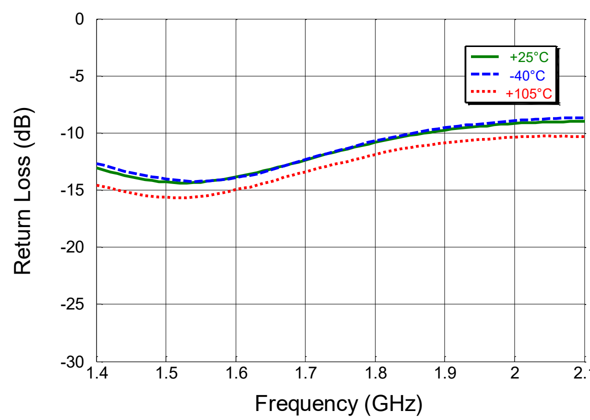
Noise Figure over swept Frequency (& Temp.) in High Gain Mode



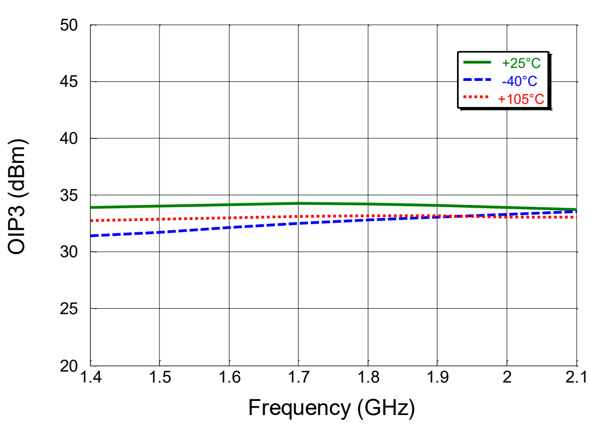
ANT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



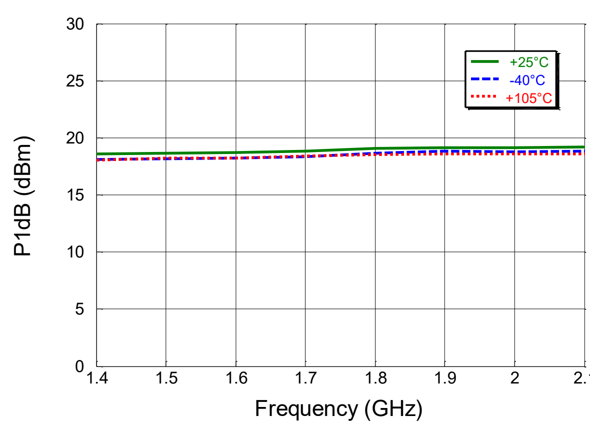
LNA OUT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in High Gain Mode

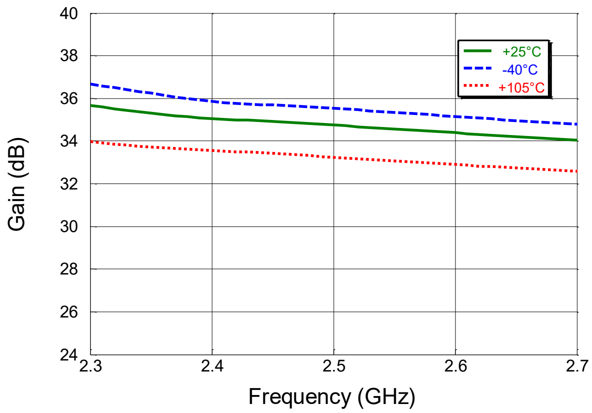


Output P1dB Compression over swept Frequency (& Temp.) in High Gain Mode

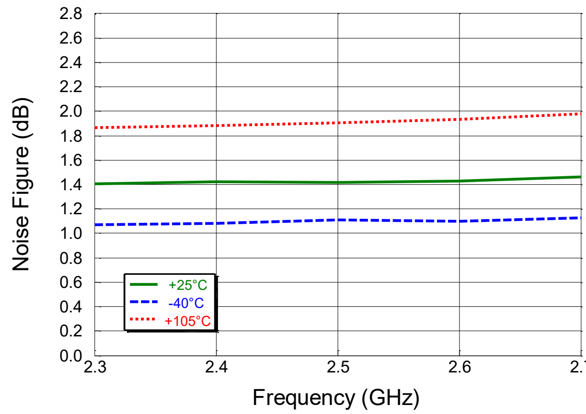


RX High Gain mode. Typical Performance Curves
P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

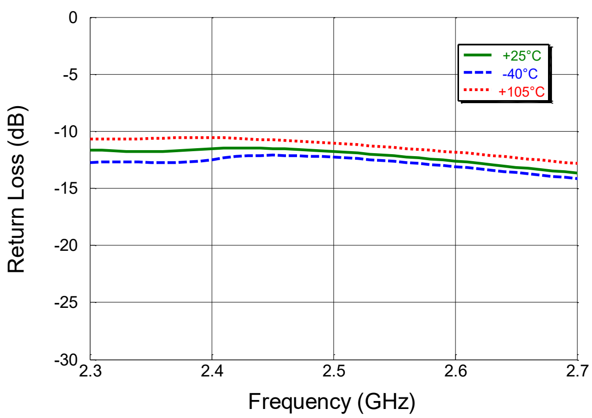
LNA Gain over swept Frequency (& Temp.) in High Gain Mode



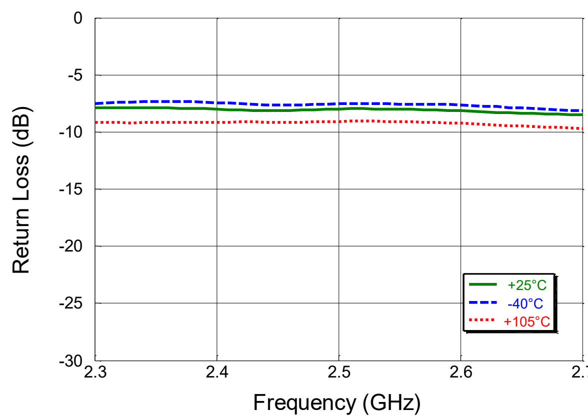
Noise Figure over swept Frequency (& Temp.) in High Gain Mode



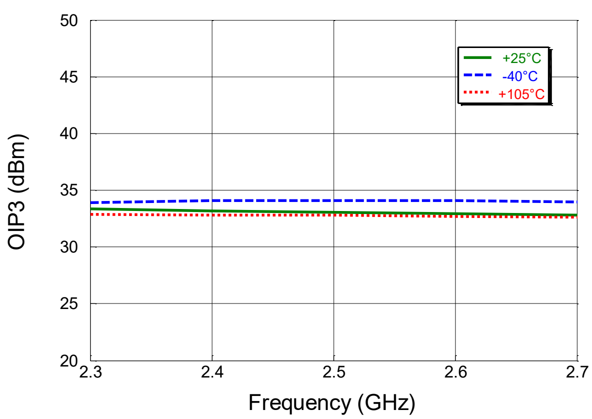
ANT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



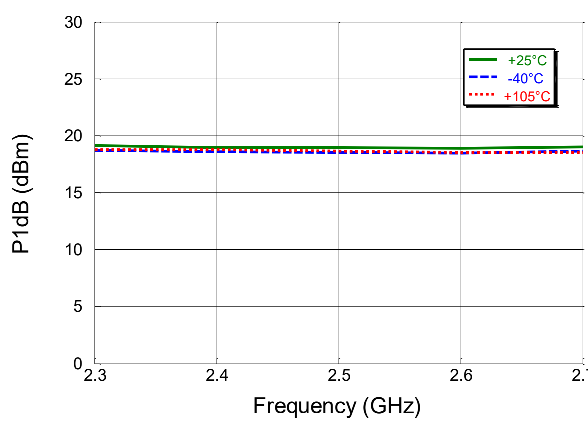
LNA OUT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in High Gain Mode



Output P1dB Compression over swept Frequency (& Temp.) in High Gain Mode



RX High Gain mode. Typical Performance Curves

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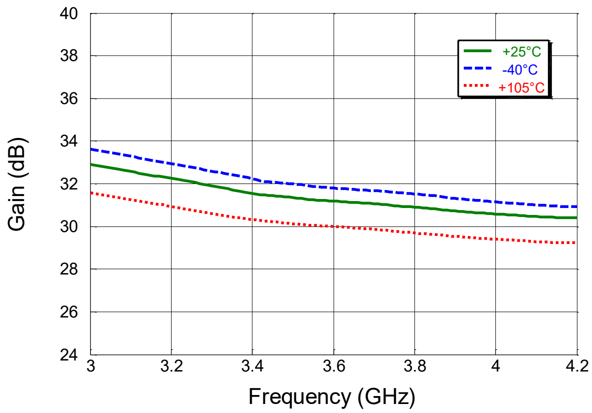
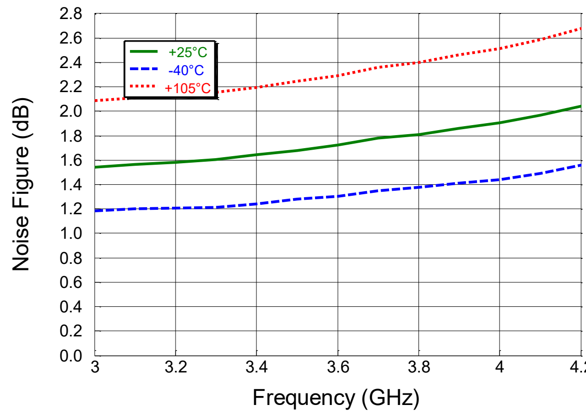
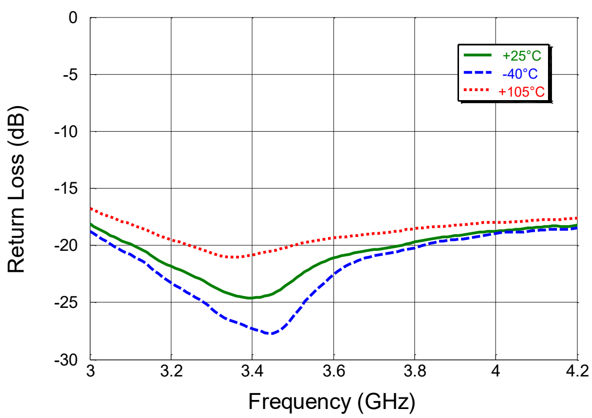
LNA Gain over swept Frequency (& Temp.) in High Gain Mode



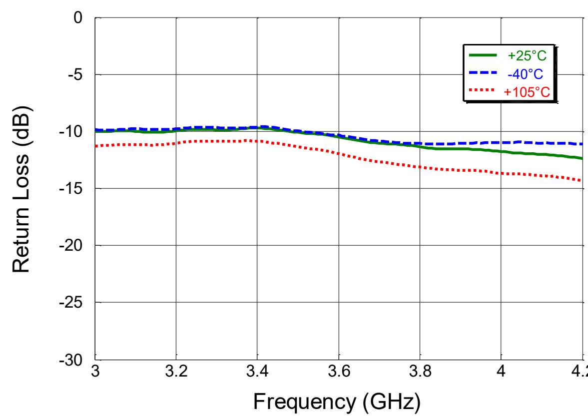
Noise Figure over swept Frequency (& Temp.) in High Gain Mode



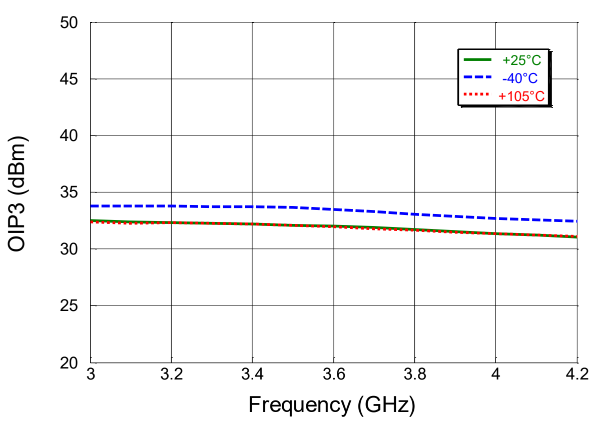
ANT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



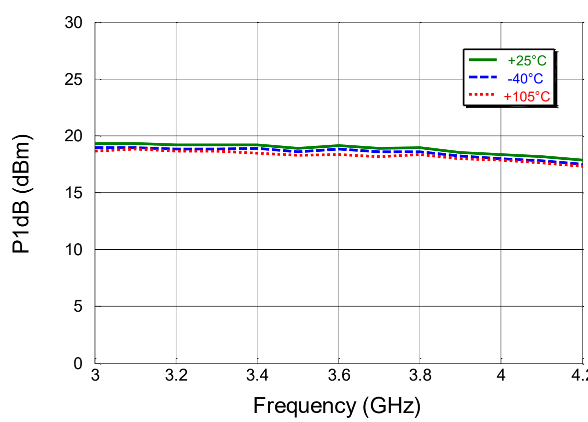
LNA OUT Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in High Gain Mode

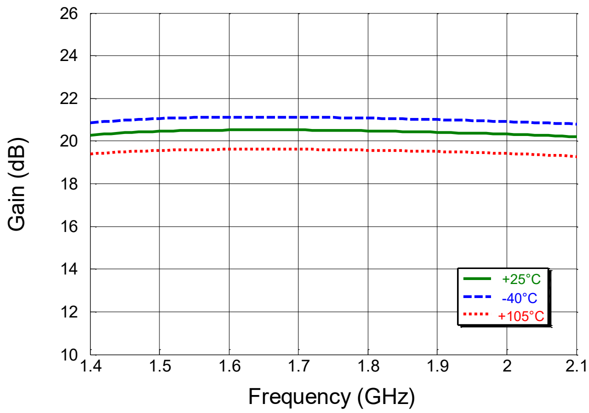


Output P1dB Compression over swept Frequency (& Temp.) in High Gain Mode

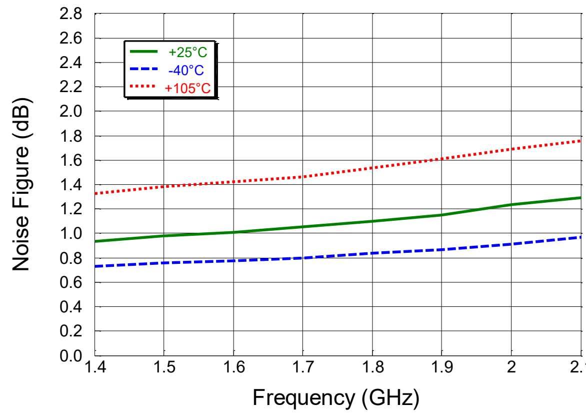


RX Low Gain mode. Typical Performance Curves
P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

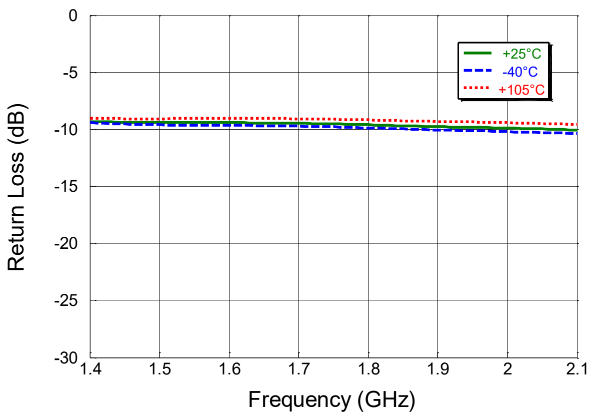
LNA Gain over swept Frequency (& Temp.) in Low Gain Mode



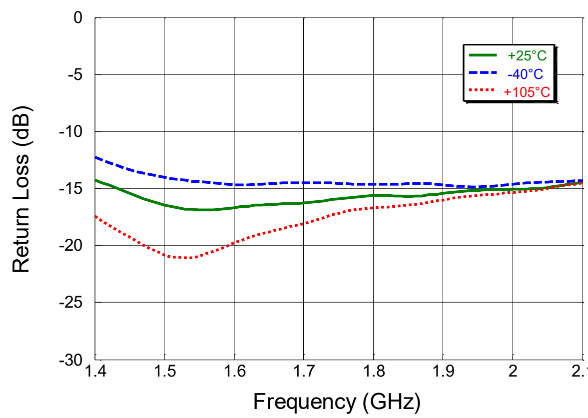
Noise Figure over swept Frequency (& Temp.) in Low Gain Mode



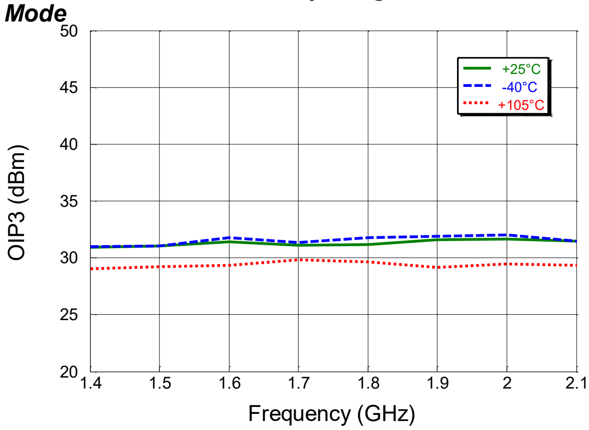
ANT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



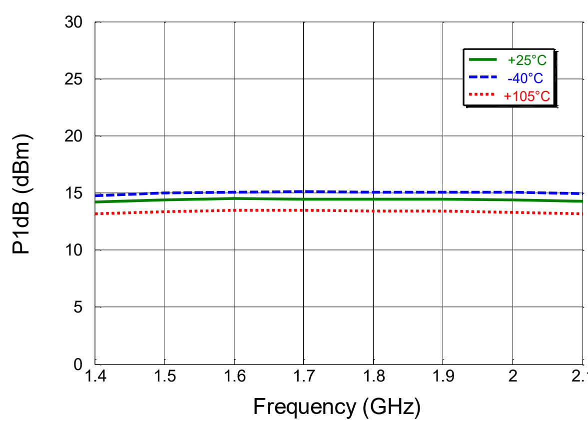
LNA OUT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in in Low Gain-Mode

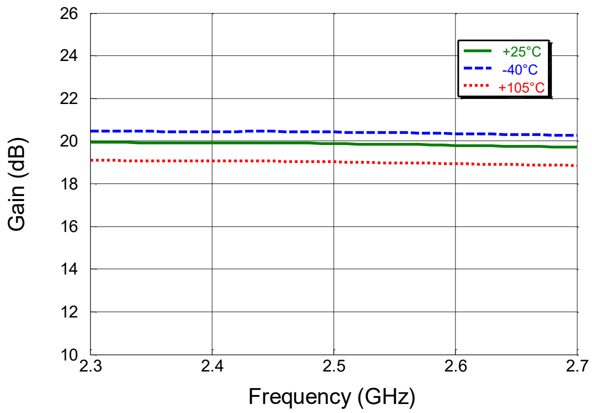


Output P1dB Compression over swept Frequency (& Temp.) in Low Gain Mode

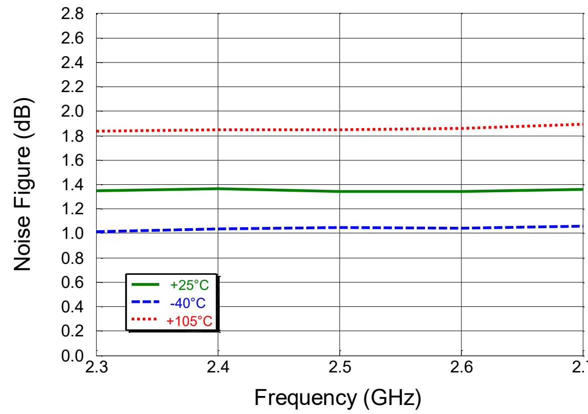


RX Low Gain mode. Typical Performance Curves
P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

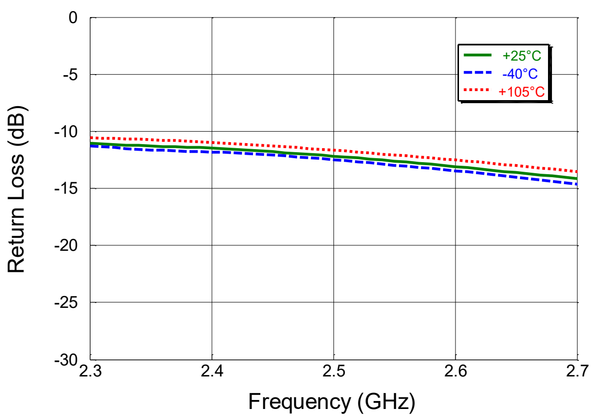
LNA Gain over swept Frequency (& Temp.) in Low Gain Mode



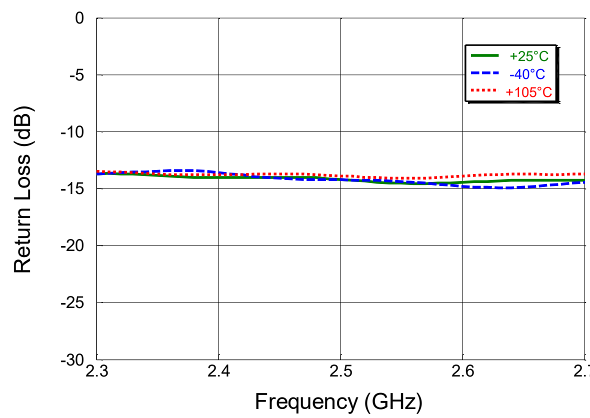
Noise Figure over swept Frequency (& Temp.) in Low Gain Mode



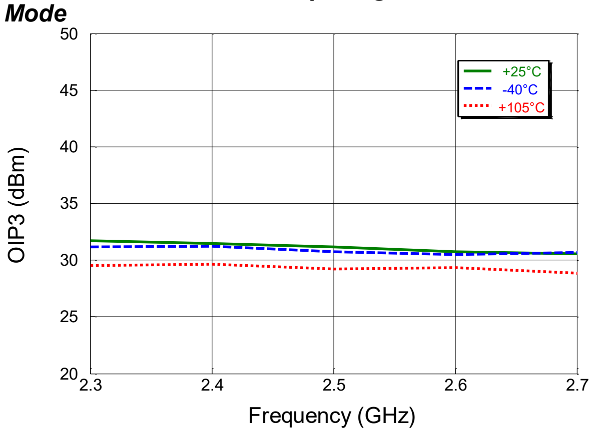
ANT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



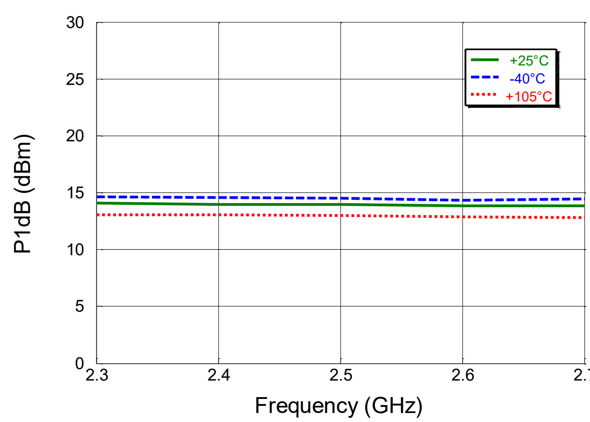
LNA OUT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in in Low Gain Mode

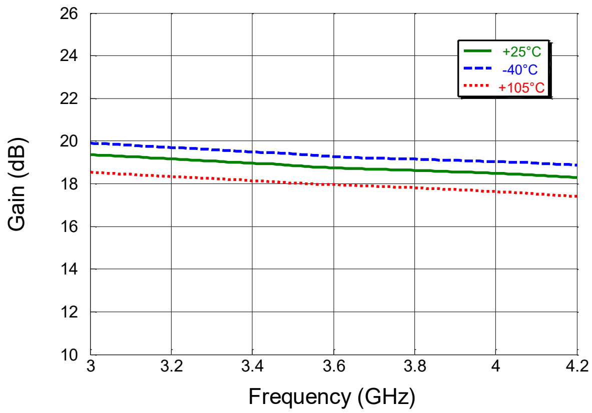


Output P1dB Compression over swept Frequency (& Temp.) in Low Gain Mode

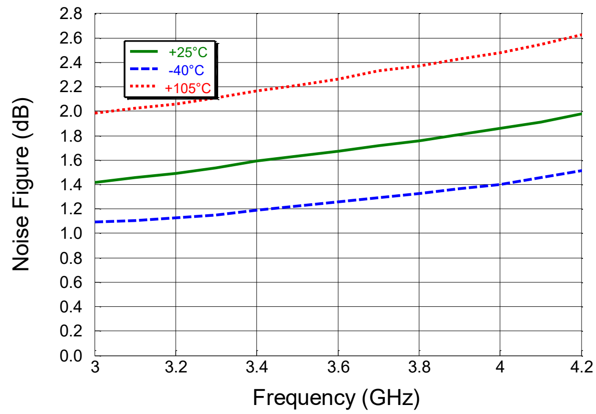


RX Low Gain mode. Typical Performance Curves
P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

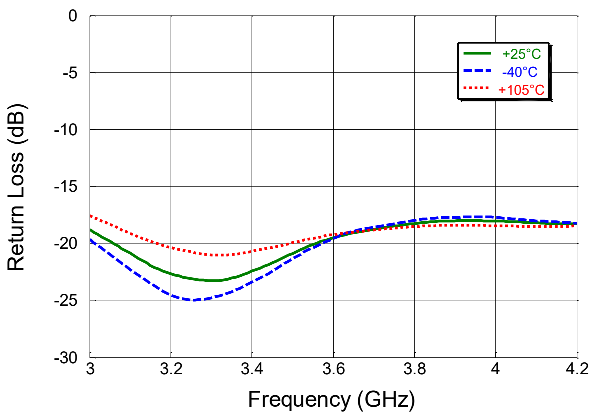
LNA Gain over swept Frequency (& Temp.) in Low Gain Mode



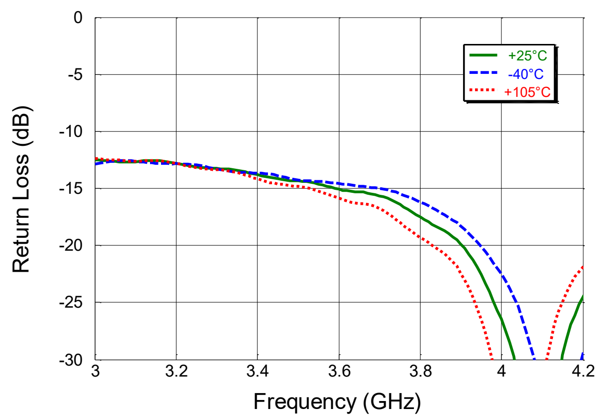
Noise Figure over swept Frequency (& Temp.) in Low Gain Mode



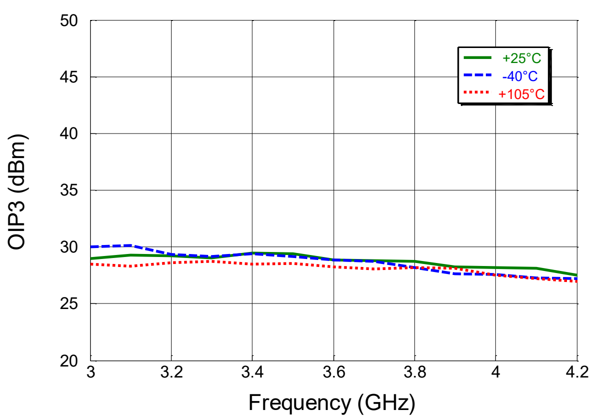
ANT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



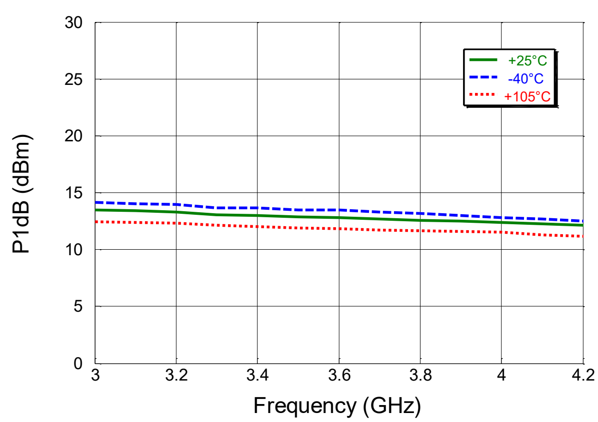
LNA OUT Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = -30 dBm & 10 MHz tone spacing in Low Gain Mode



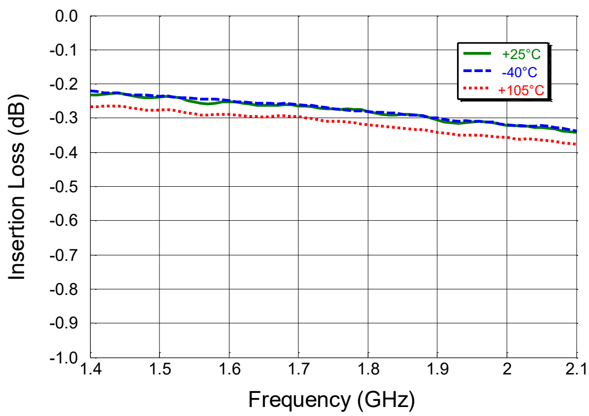
Output P1dB Compression over swept Frequency (& Temp.) in Low Gain Mode



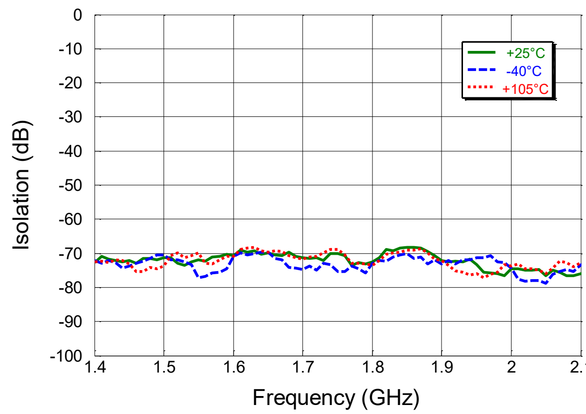
TX mode. Typical Performance Curves

P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

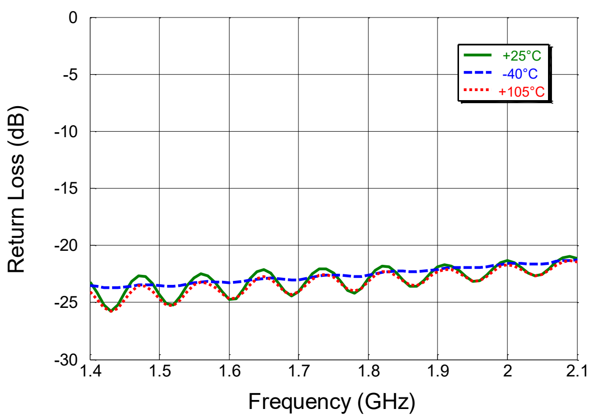
Switch Insertion Loss over swept Frequency (& Temp.)



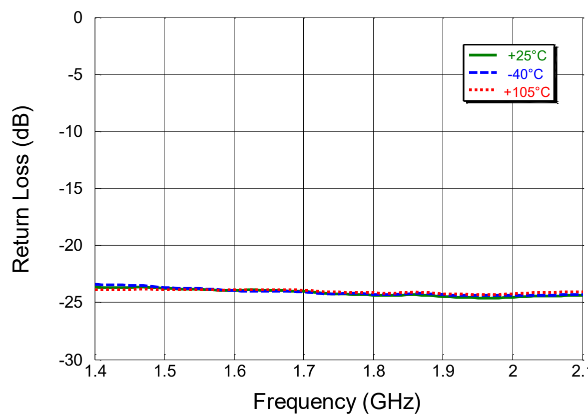
ANT to LNA OUT Isolation over swept Frequency (& Temp.)



ANT Port Return Loss over swept Frequency (& Temp.)

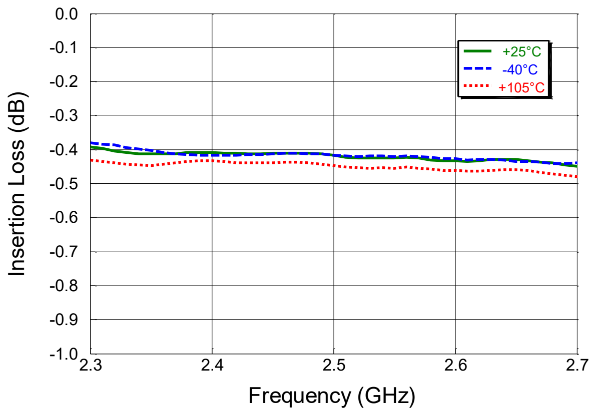


TX Port Return Loss over swept Frequency (& Temp.)

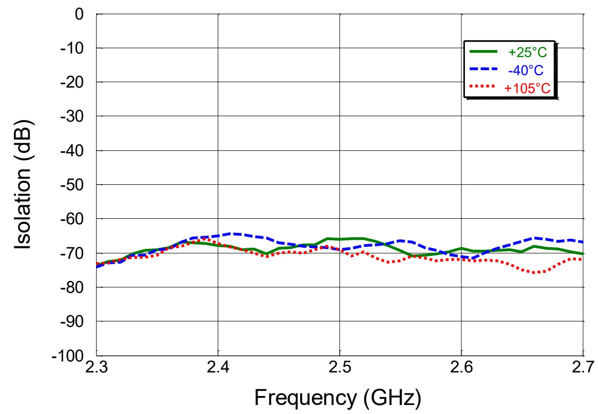


TX mode. Typical Performance Curves
P_{IN} = -30 dBm, $V_{CC} = V_{DD}$ = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

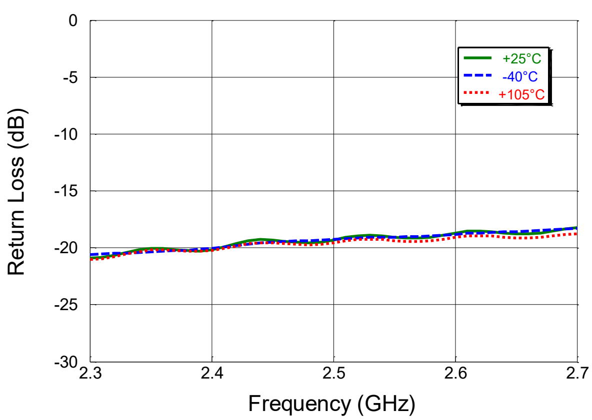
Switch Insertion Loss over swept Frequency (& Temp.)



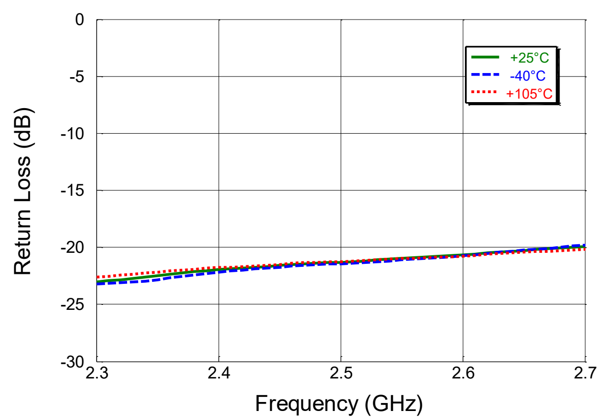
ANT to LNA OUT Isolation over swept Frequency (& Temp.)



ANT Port Return Loss over swept Frequency (& Temp.)

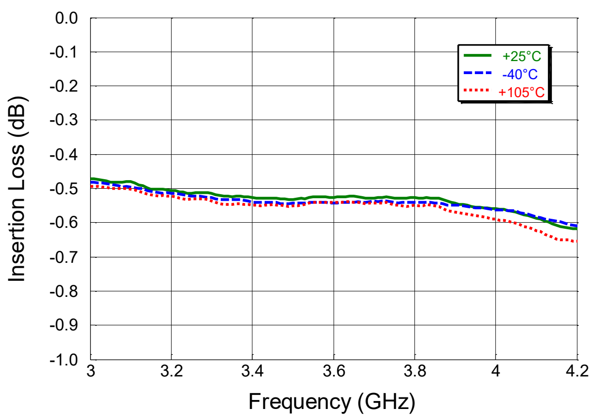


TX Port Return Loss over swept Frequency (& Temp.)

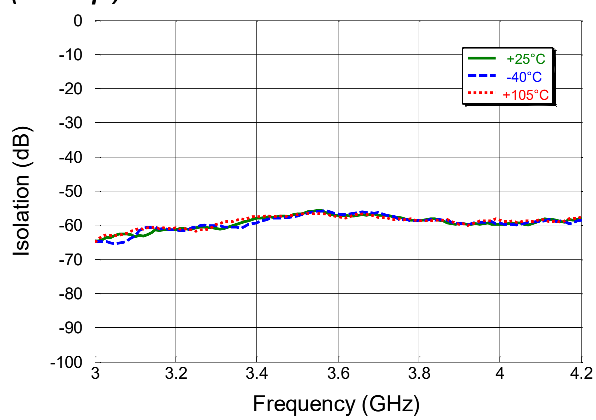


TX mode. Typical Performance Curves
P_{IN} = -30 dBm, V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

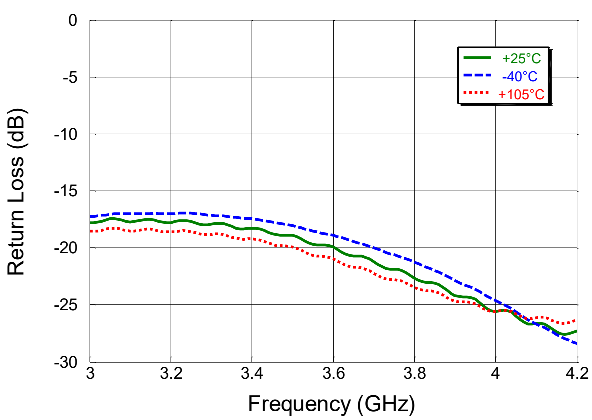
Switch Insertion Loss over swept Frequency (& Temp.)



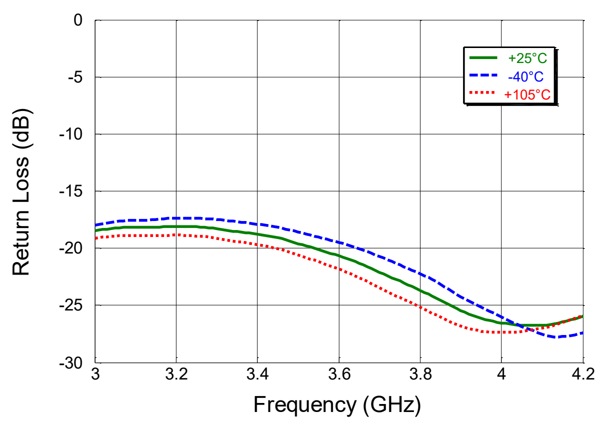
ANT to LNA OUT Isolation over swept Frequency (& Temp.)



ANT Port Return Loss over swept Frequency (& Temp.)

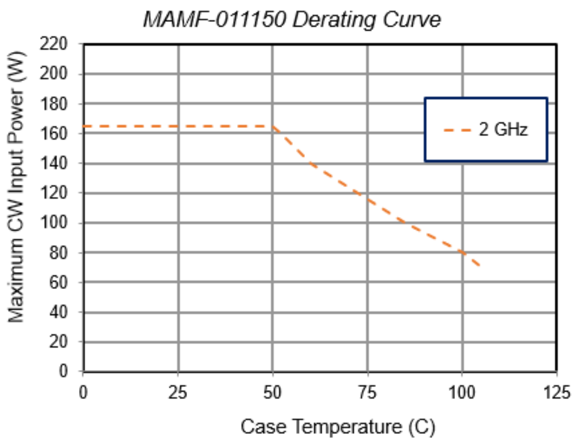


TX Port Return Loss over swept Frequency (& Temp.)

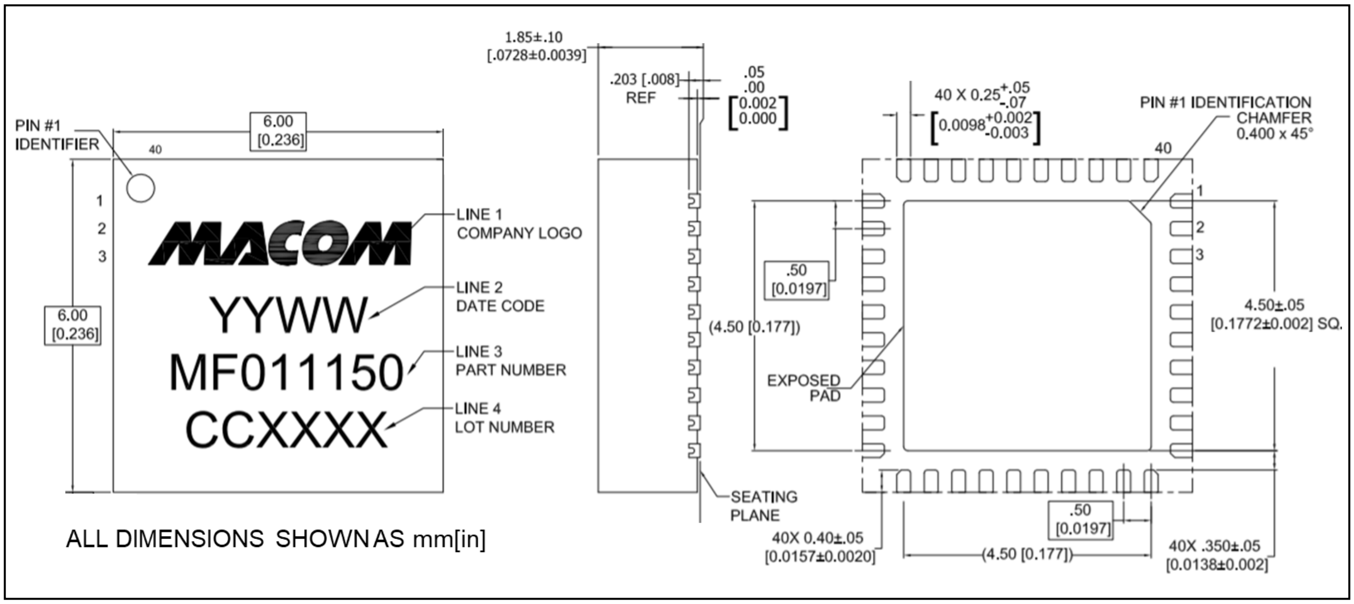


Typical Performance Curves
V_{CC} = V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

ANT to LOAD Input Power Derating Curve @ 2GHz



Lead-Free 6 mm 40-Lead HQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements in accordance to JEDEC J-STD-020D.
Plating is NiPdAuAg over Copper