Upconverter
71 - 86 GHz

MAMF-011142
Rev. V1

Features

- E-Band Upconverter
- Direct Up-Conversion with I/Q BW up to 2.25 GHz
- WR12 Interface for the RF Output
- LO×8 with Buffer
- Wide Dynamic Range Power Detector
- 30 dB Conversion Gain
- 25.5 dBm Saturated Output Power
- 40 dB of Linear Gain Turn-Down
- Tunable Carrier and Sideband Suppression
- RoHS* Compliant Surface Mount Package
- Size: 12000 × 8000 × 2220 µm

Applications

- Point to Point
- Infrastructure

Description

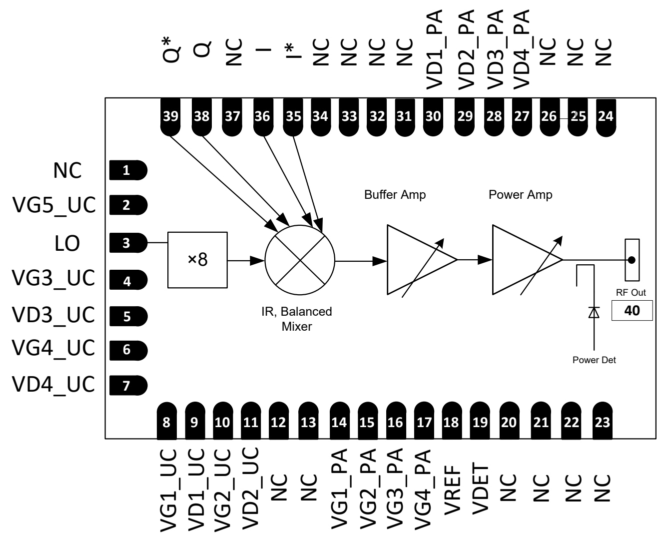
The MAMF-011142 is a surface mount E-band transmitter. The module operates from 71 - 86 GHz and is designed to be used in direct conversion or heterodyne applications. The RF output is a WR12 interface.

The module provides 30 dB small signal gain and a saturated output power of 25.5 dBm at the optimum bias. Linear turn-down of the gain allows for a wide range of output powers from the radio, over temperature and process variation. Carrier leakage and sideband rejection performance can be enhanced by tuning the DC offsets on the IF lines.

Other features include a local oscillator ×8 multiplier and buffer, and a wide dynamic range power detector on the output. The module is ideally suited for low to high capacity, high power E-band point to point radios.

Each device is 100% RF tested to ensure performance compliance.

Functional Schematic[1]



1. The exposed pad centered on the package bottom must be connected to RF, DC and Thermal GROUND.

Ordering Information

Part Number	Package
MAMF-011142	Parts shipped in tray
MAMF-011142-TR0200	200 part reel
MAMF-011142-TR0500	500 part reel
MAMF-011142-001SMB	Evaluation Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
VD = 4 V, UC ID1,2,3,4 = 90, 190, 105, 65 mA, PA ID1,2,3,4 = 120, 120, 200, 320 mA, VG5 = -1.5 V, PLO = -5 dBm, Backside Temperature (T_B) = +25°C

Parameters	Test Conditions	Units	Min.	Typ.	Max.
RF Frequency	—	GHz	71	—	86
IF Bandwidth	—	GHz	DC	—	2.25
LO Frequency	—	GHz	8.625	—	11
LO Multiplication Factor	—	–		8	
LO Input Power	—	dBm	—	-5	—
Conversion Gain	IF = 700 MHz	dB	24	30	—
Output P_{SAT}	IF = 700 MHz	dBm	23	25.5	—
Output IP3	P_{IN} = -10 dBm total, IF = 21.4 MHz, ΔIF = 4.6 MHz	dBm	—	31	—
Total P_{OUT} at C/I3 = 25 dBc	P_{IN} = -10 dBm total, IF = 21.4 MHz, ΔIF = 4.6 MHz, RF = 86 GHz	dBm	—	20	—
Total P_{OUT} at C/I3 = 20 dBc	P_{IN} = -10 dBm total, IF = 21.4 MHz, ΔIF = 4.6 MHz, RF = 86 GHz	dBm	—	22	—
Total P_{OUT} at C/I2 = 43 dBc	P_{IN} = -10 dBm total, IF = 21.4 MHz, ΔIF = 4.6 MHz, RF = 76 GHz	dBm	—	18	—
Conversion Gain Variation Over 2 GHz BW	IF = 700 MHz	dB/GHz	—	2	—
Gain Adjust Dynamic Range	—	dB	—	40	—
Carrier Leakage Tuning (DC) Range	—	V	—	+/-1	—
Tunable Carrier Leakage with 1 mV Tuning Step	—	dBc	—	-30	—
LO×7 Leakage	P_{IN} = -10 dBm, RF = 83.5 GHz	dBc	—	36	—
LO×9 Leakage	P_{IN} = -10 dBm, RF = 73.5 GHz	dBc	—	37	—
Image Rejection	IF = 21.4 MHz	dBc	—	20	—
Noise Figure	IF = 2.25 GHz	dB	—	16	—
Return Loss	RF LO IF	dB	—	8 12 10	—
Power Detector Directivity	—	dB		18	
Output Power Detector	—	–		10 mV @ -10 dBm	
Drain Voltage	—	V	—	4	—
Quiescent Drain Current (DC)	—	A	—	1.21	—

Biasing over Temperature

It is recommended to have a current controlled biasing method.
Temperature data presented here is at the following bias levels unless otherwise specified.
For graphs labelled ID12_UC, stages 1 and 2 of the upconverter are combined to create ID1_UC + ID2_UC; similarly for ID34_UC.

Pin Label	Current @ -40°C (mA)	Gate Voltage @ -40°C (V)	Current @ +25°C (mA)	Gate Voltage @ +25°C (V)	Current @ +85°C (mA)	Gate Voltage @ +85°C (V)
VD1_UC	52.5	-0.62	90	-0.48	105	-0.35
VD2_UC	107.5	-0.62	190	-0.48	205	-0.35
VD3_UC	100	-0.73	105	-0.65	120	-0.55
VD4_UC	60	-0.73	65	-0.65	80	-0.55
VG5_UC	-2	-1.50	-2	-1.50	-2	-1.50
VD1_PA	120	-0.42	120	-0.41	120	-0.39
VD2_PA	120	-0.42	120	-0.41	120	-0.39
VD3_PA	200	-0.42	200	-0.41	200	-0.39
VD4_PA	320	-0.42	320	-0.41	320	-0.39

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Drain Voltage	+4.3 V
Gate Bias Voltage (VG1,2,3,4_UC and PA)	-1.5 V < VG < +0.3 V
Gate Bias Voltage (VG5_UC)	-5 V < VG < 0 V
Total Input Power	+10 dBm
Input Power per IF	+4 dBm
LO Input Power	+5 dBm
Junction Temperature[4,5]	+150°C
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1×10^6 hours.
5. Junction Temperature (T_J) = $T_B + \Theta_{jc} \times (V \times I)$, where T_B is backside temperature of package and Θ_{jc} is thermal resistance of the device.
   See table below for Junction Temperature for each stage of the module. Each stage must remain below 150°C.

Handling Procedures

Please observe the following precautions to avoid damage:

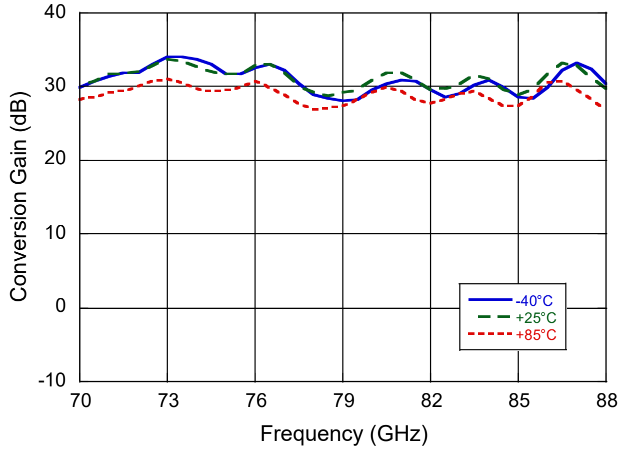
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B static sensitive devices.

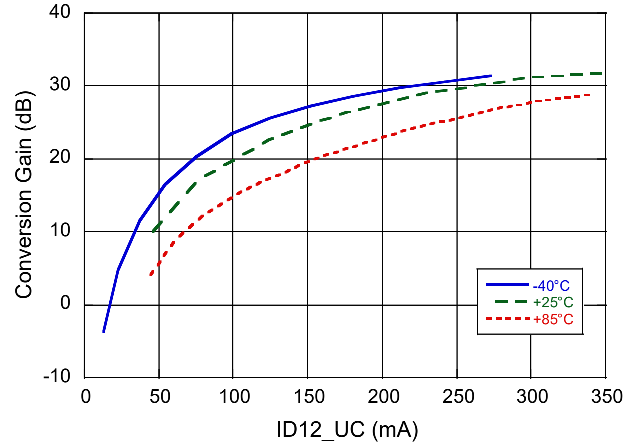
Pin Label	Thermal Resistance (°C/W)	Current @ +85°C (mA)	T_J for T_B = +85°C (°C)	Maximum Drain Current Rating (mA)
VD1_UC	116	105	134	140
VD2_UC	66	205	139	240
VD3_UC	75	120	121	135
VD4_UC	116	80	122	140
VD1_PA	75	120	121	200
VD2_PA	79	120	123	200
VD3_PA	59	200	132	275
VD4_PA	35	320	130	460

Typical Performance Curves over Temperature at Total P_{IN} = -10 dBm

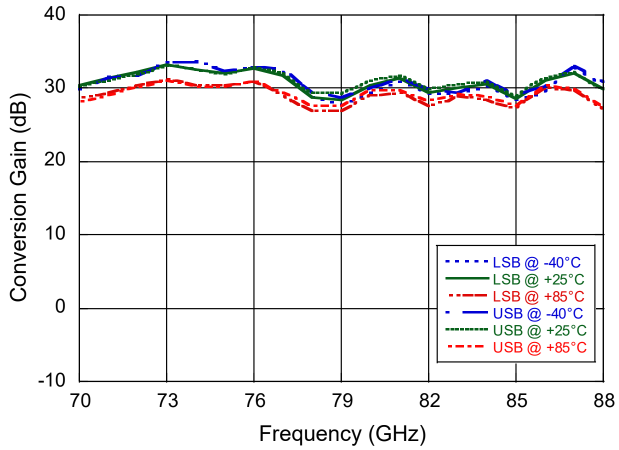
Conversion Gain at Nominal Bias at IF = 21.4 MHz



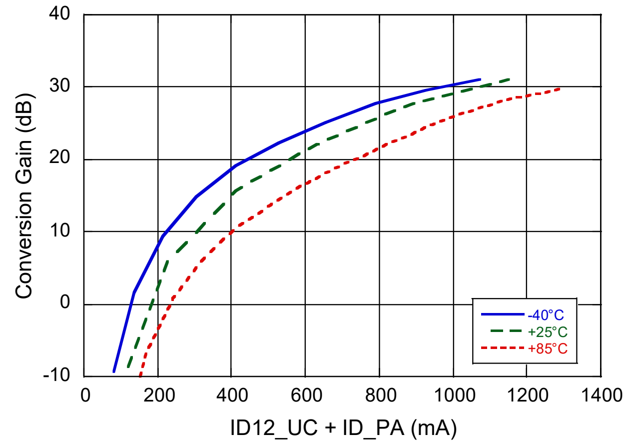
Gain vs. RF Buffer Bias at IF = 21.4 MHz, RF = 86 GHz



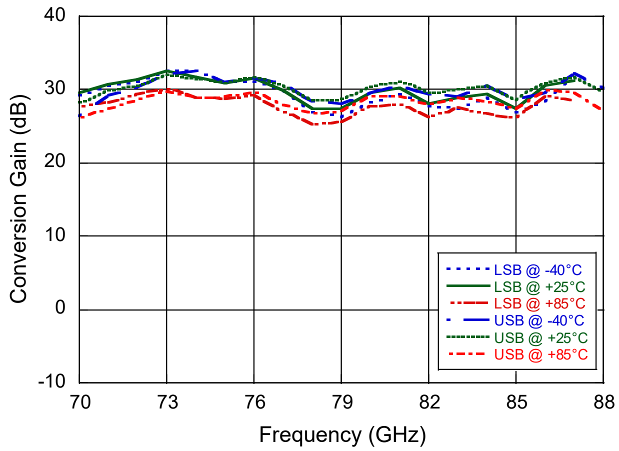
Conversion Gain at Nominal Bias at IF = 700 MHz



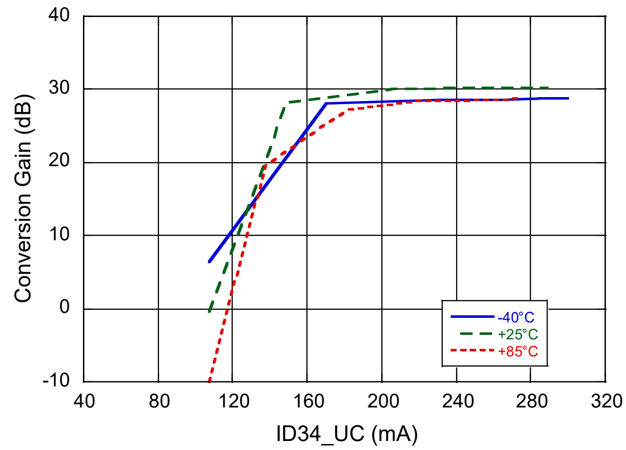
Gain vs. RF Buffer and PA at IF = 21.4 MHz, RF = 86 GHz



Conversion Gain at Nominal Bias at IF = 2.25 GHz



Gain vs. LO Bias at IF = 21.4 MHz, RF = 86 GHz



Typical Performance Curves over Temperature at Total P_{IN} = -10 dBm

Gain vs. Mixer Bias at IF = 21.4 MHz, RF = 86 GHz

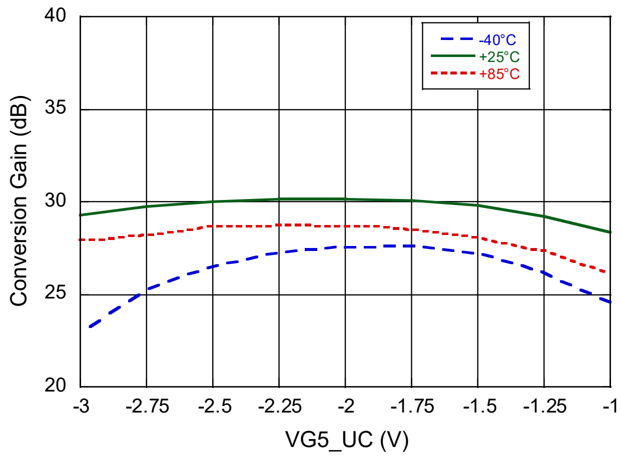
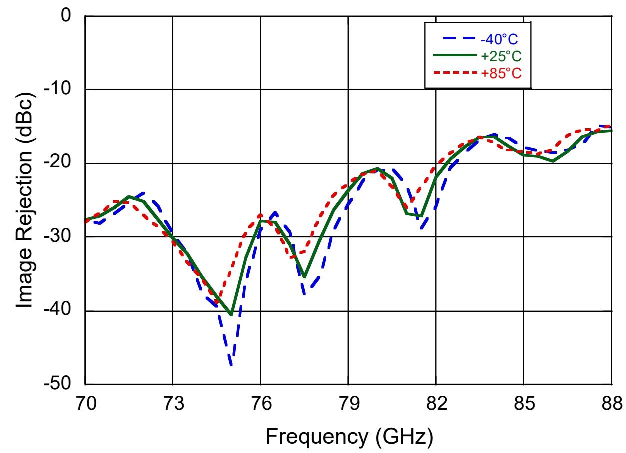


Image Rejection at IF = 21.4 MHz



Gain vs. LO Power at IF = 21.4 MHz, +25°C

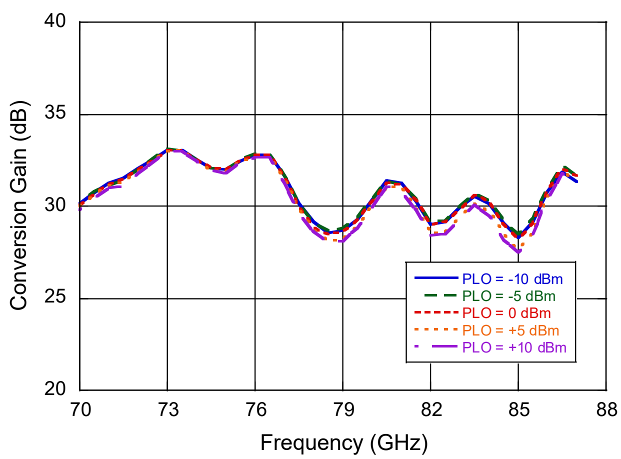


Image Rejection at IF = 700 MHz

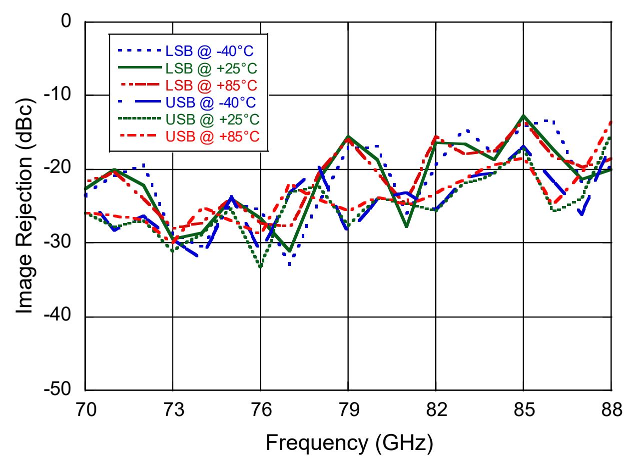
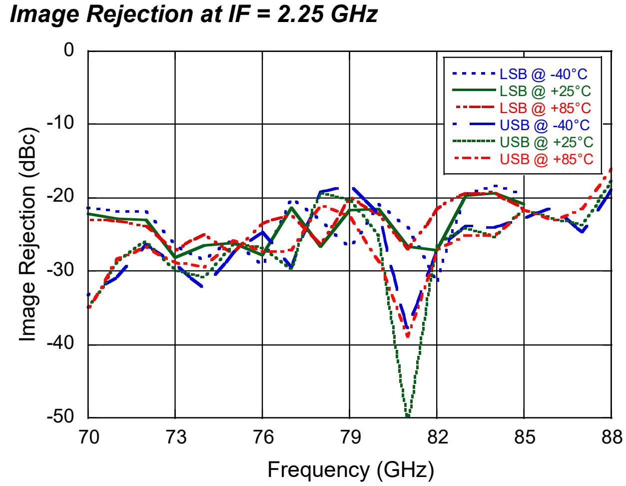
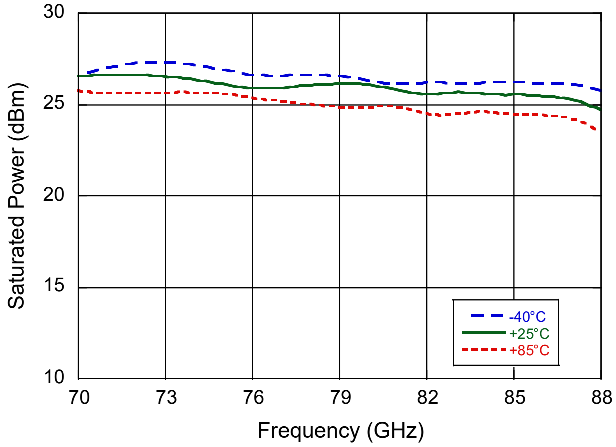


Image Rejection at IF = 2.25 GHz

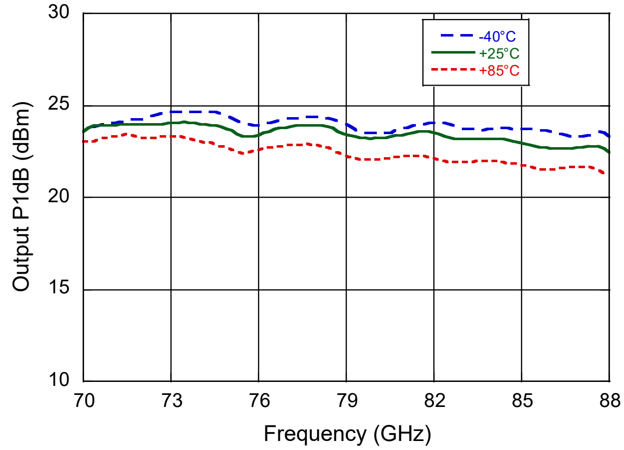


Typical Performance Curves over Temperature

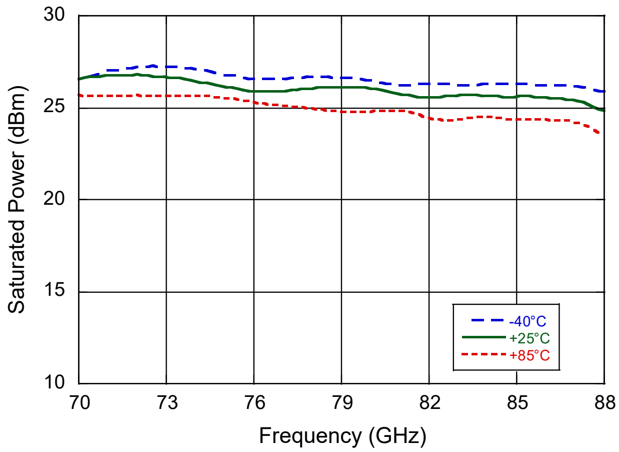
Saturated Power at Nominal Bias, IF = 21.4 MHz



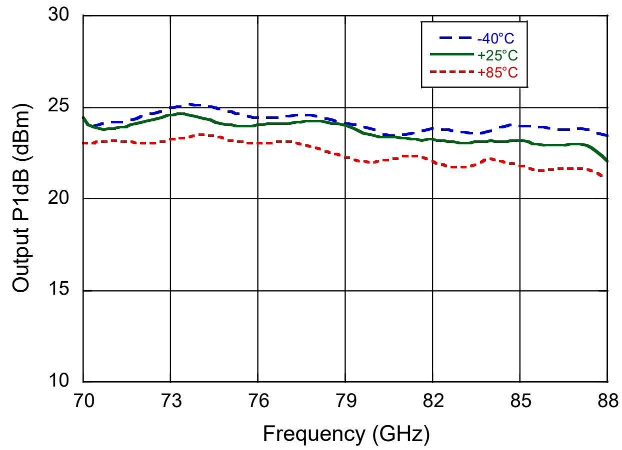
P1dB at Nominal Bias, IF = 21.4 MHz



Saturated Power at Nominal Bias, IF = 700 MHz

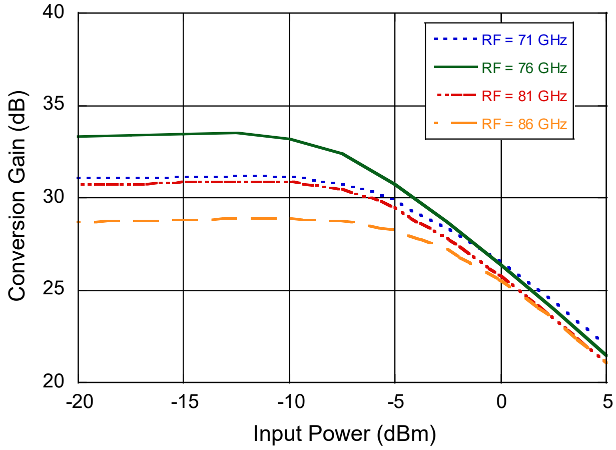


P1dB at Nominal Bias, IF = 700 MHz

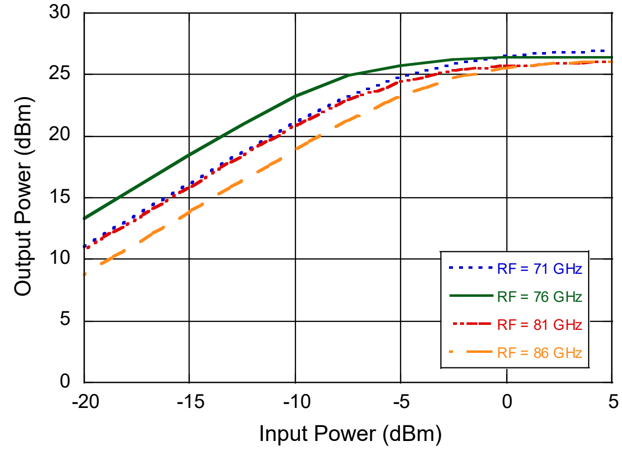


Typical Performance Curves over Temperature at IF = 21.4 MHz

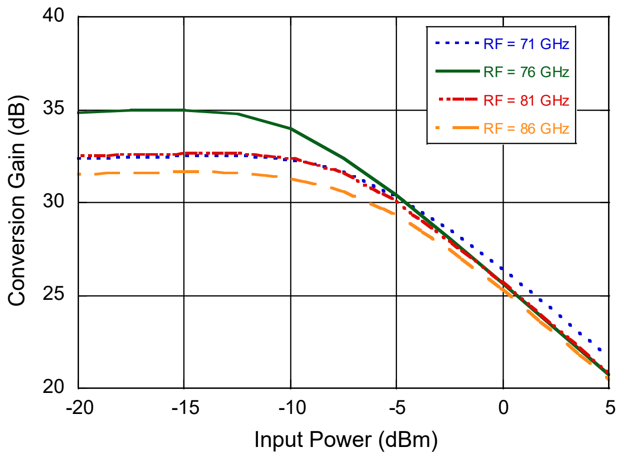
Gain vs. Input Power at -40°C



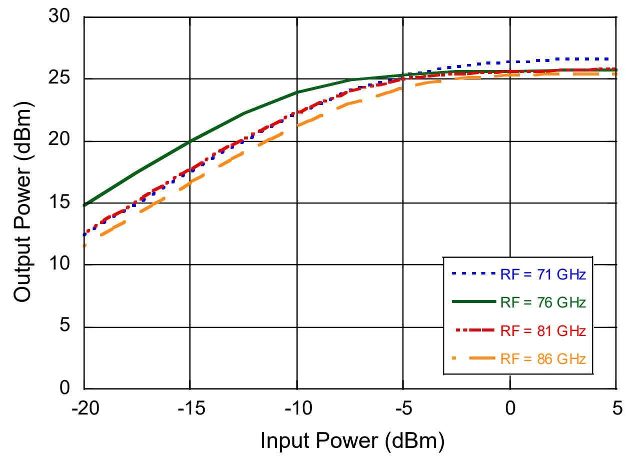
Pout vs. Input Power at -40°C



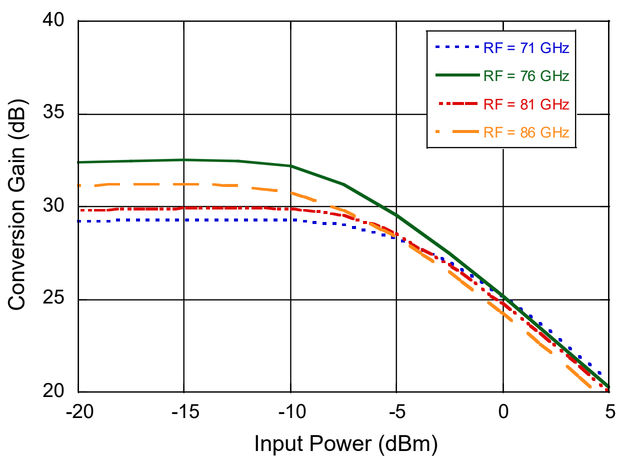
Gain vs. Input Power at +25°C



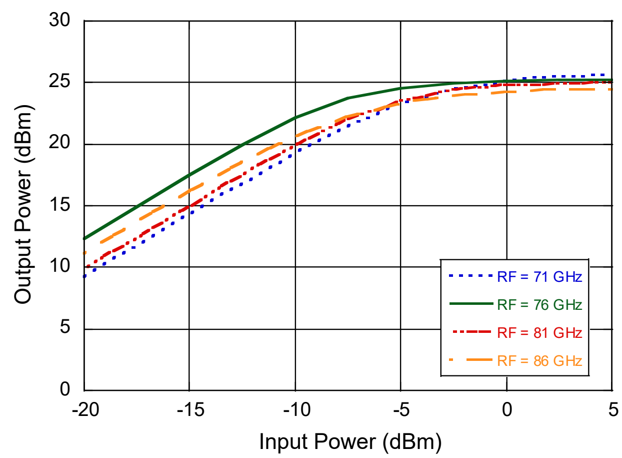
Pout vs. Input Power at +25°C



Gain vs. Input Power at +85°C

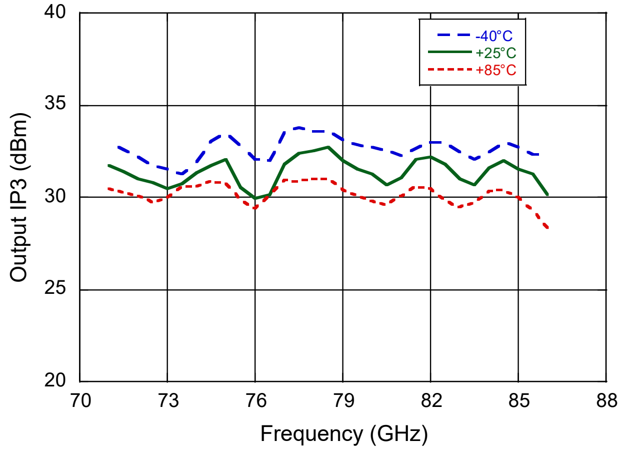


Pout vs. Input Power at +85°C

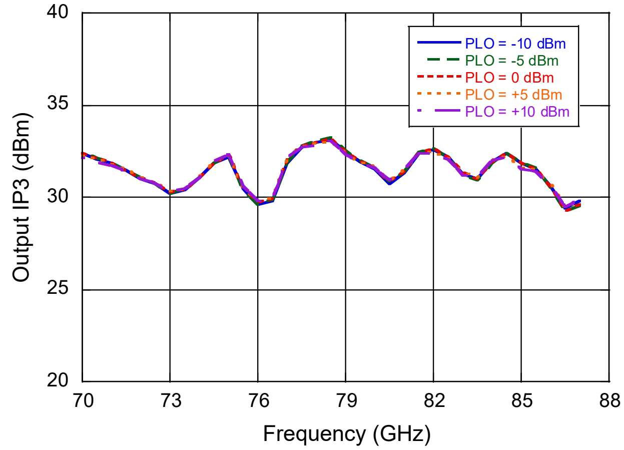


Typical Performance Curves over Temperature at Total P_{IN} = -10 dBm

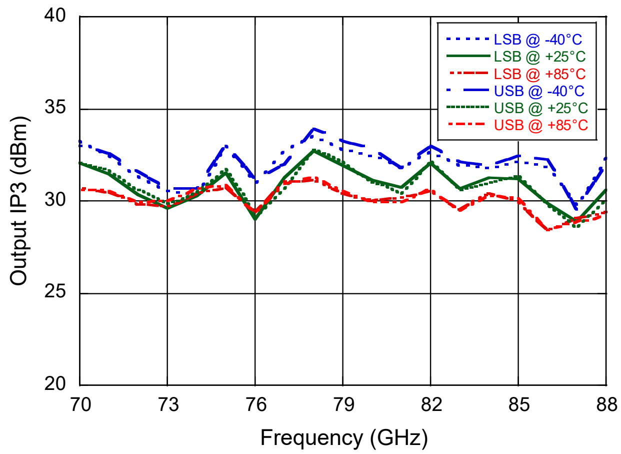
OIP3 at Nominal Bias at IF = 21.4 and 26.0 MHz



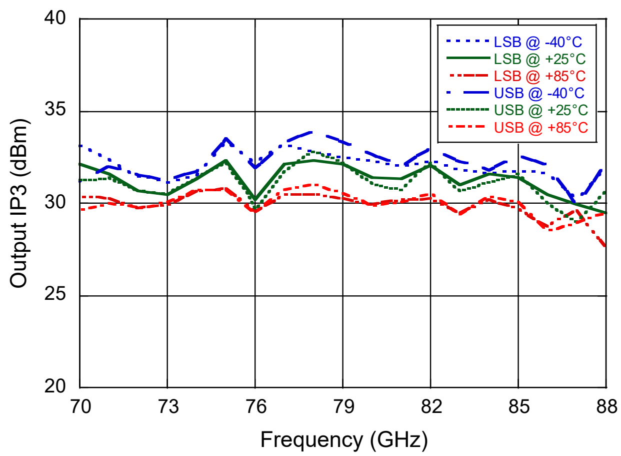
OIP3 vs. LO Power at IF = 21.4 and 26.0 MHz, +25°C



OIP3 at Nominal Bias at IF = 700 and 704.6 MHz

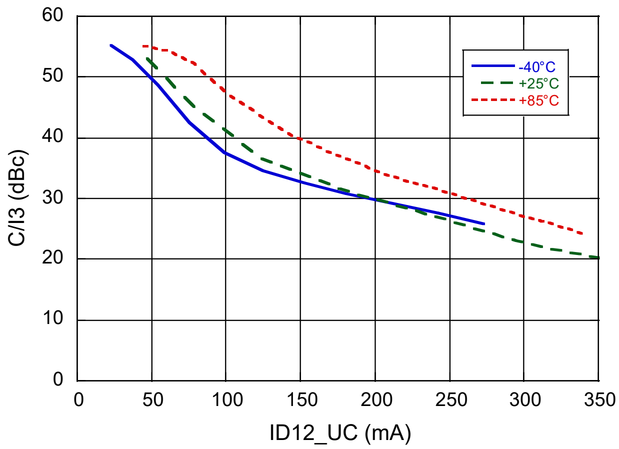


OIP3 at Nominal Bias at IF = 2.25 and 2.261 GHz

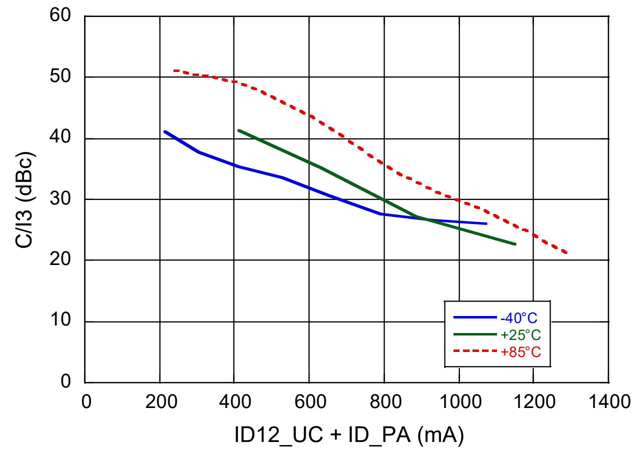


Typical Performance Curves over Temp. at Total P_{IN} = -10 dBm, IF = 21.4 and 26 MHz

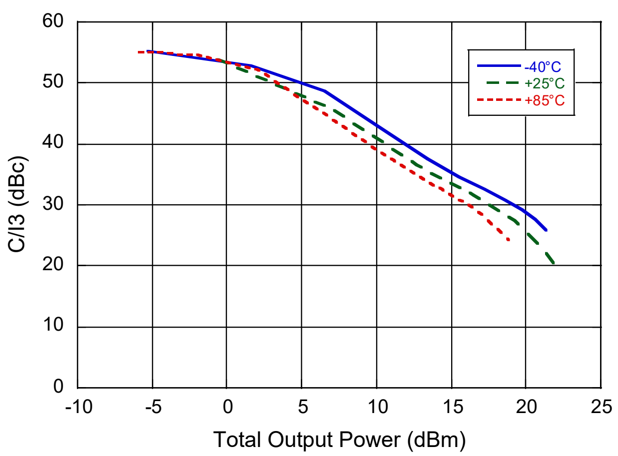
C/I3 vs. RF Buffer bias, RF = 86 GHz



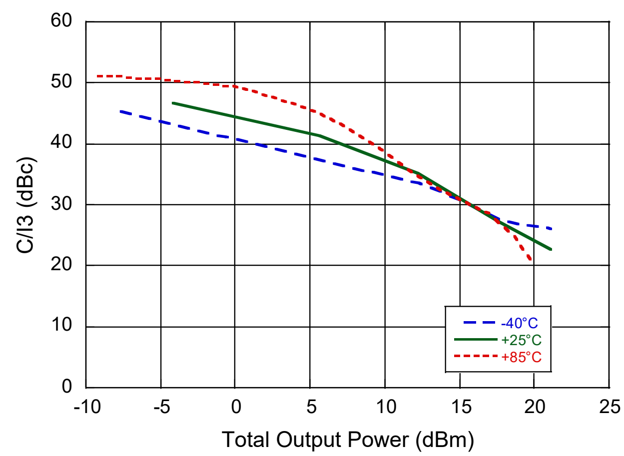
C/I3 vs. RF Buffer and PA Bias, RF = 86 GHz



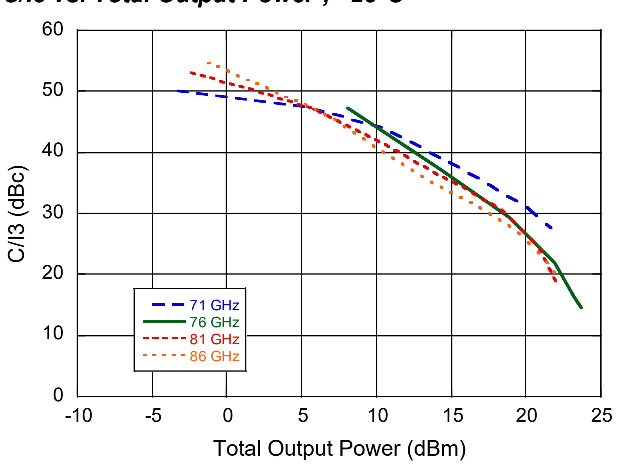
C/I3 vs. Total Output Power[7], RF = 86 GHz



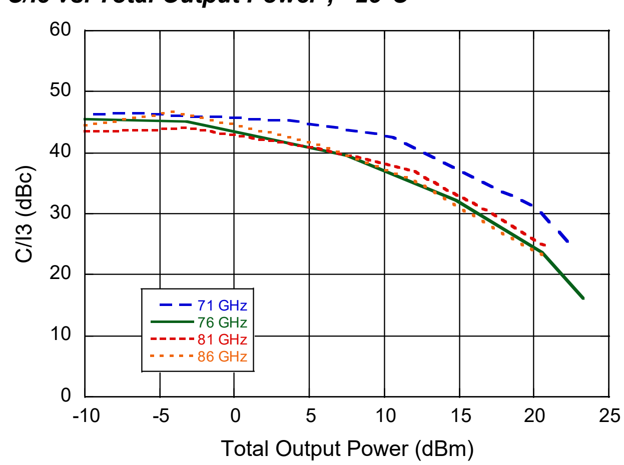
C/I3 vs. Total Output Power[8], RF = 86 GHz



C/I3 vs. Total Output Power[6], +25°C



C/I3 vs. Total Output Power[7], +25°C

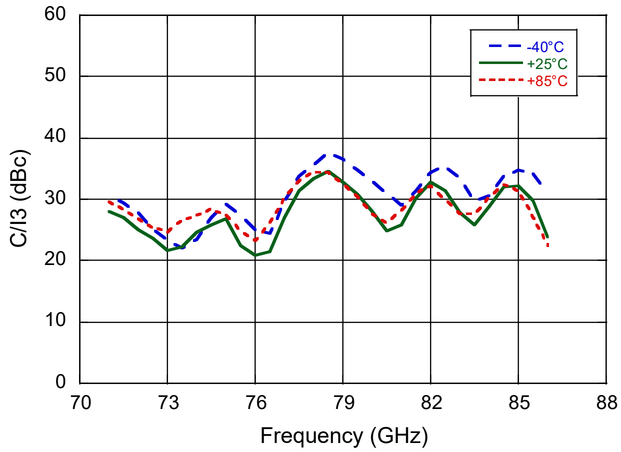


6. Output power controlled by RF buffer current.

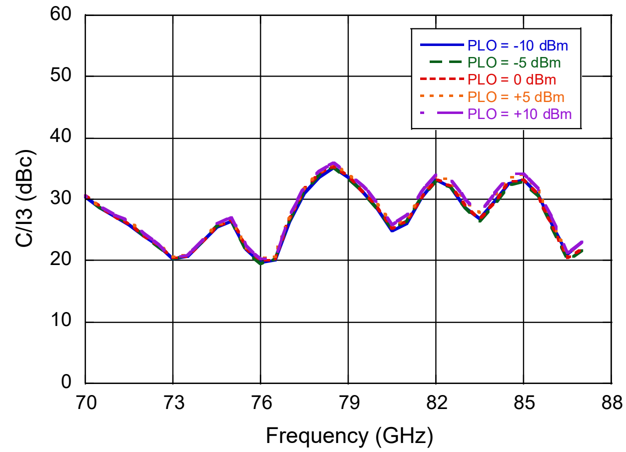
7. Output power controlled by RF buffer and PA currents.

Typical Performance Curves over Temp. at Total P_{IN} = -10 dBm, IF = 21.4 and 26 MHz

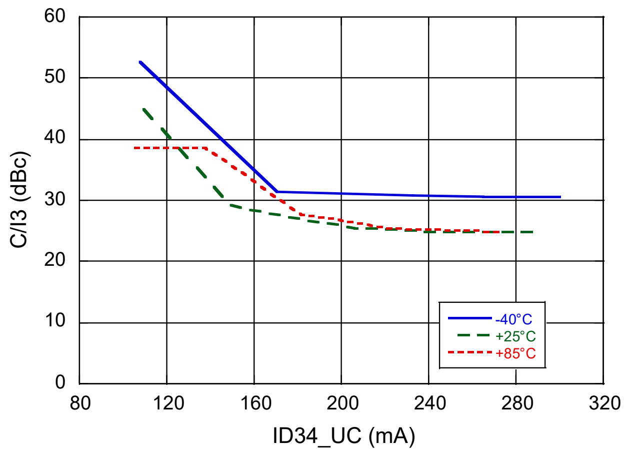
C/I3 at Nominal Bias



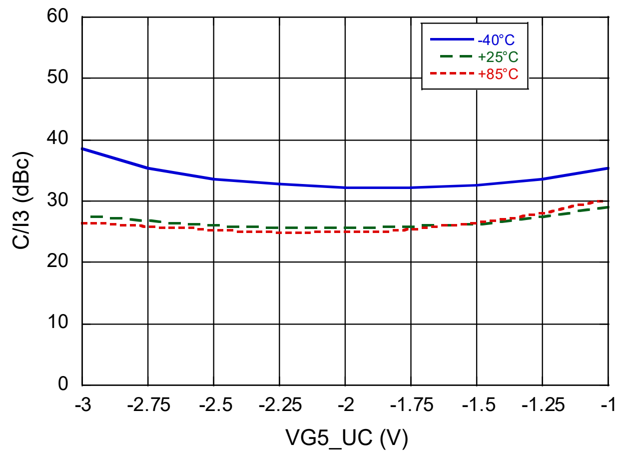
C/I3 vs. LO Power, +25°C



C/I3 vs. LO Bias, RF = 86 GHz

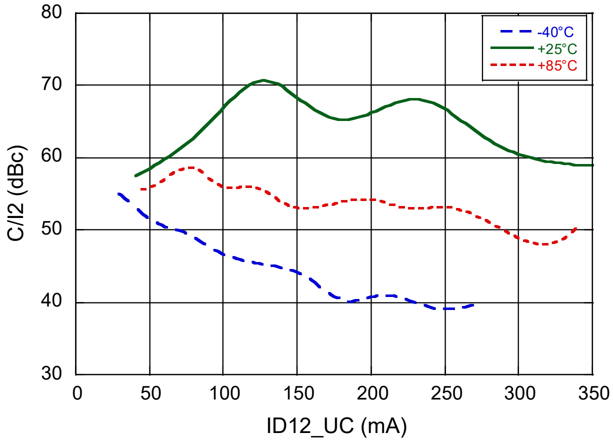


C/I3 vs. Mixer Bias, RF = 86 GHz

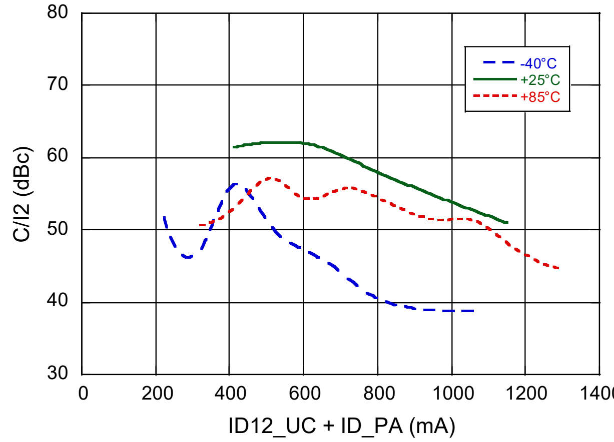


Typical Performance Curves over Temp. at Total P_{IN} = -10 dBm, IF = 21.4 and 26 MHz

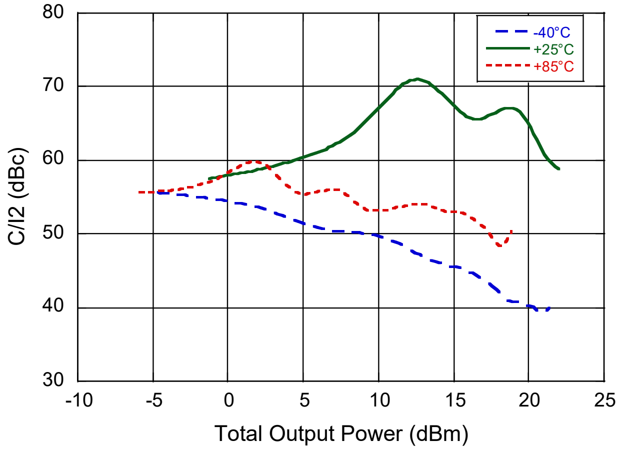
C/I2 vs. RF Buffer Bias, RF = 86 GHz



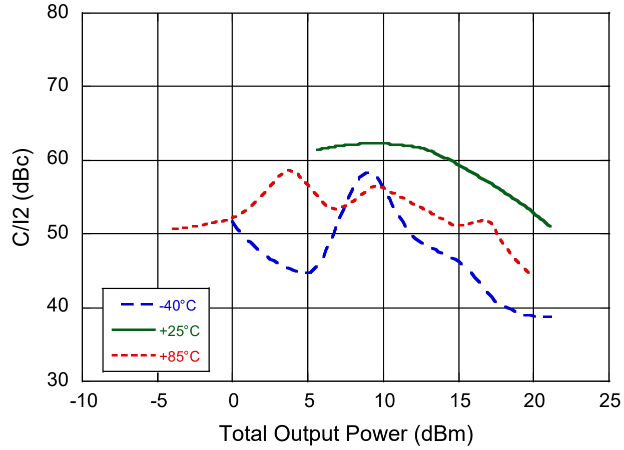
C/I2 vs. RF Buffer and PA Bias, RF = 86 GHz



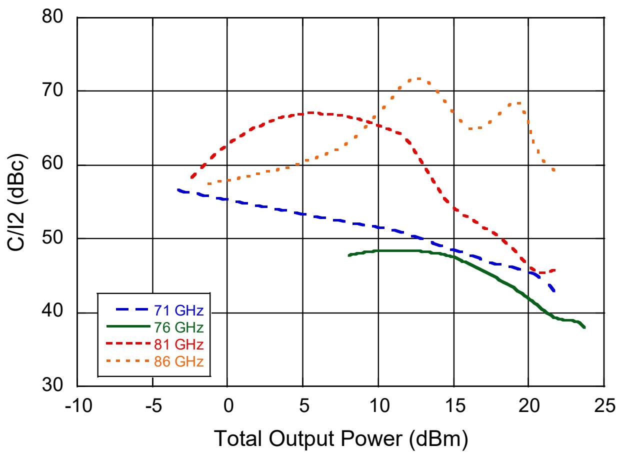
C/I2 vs. Total Output Power[9], RF = 86 GHz



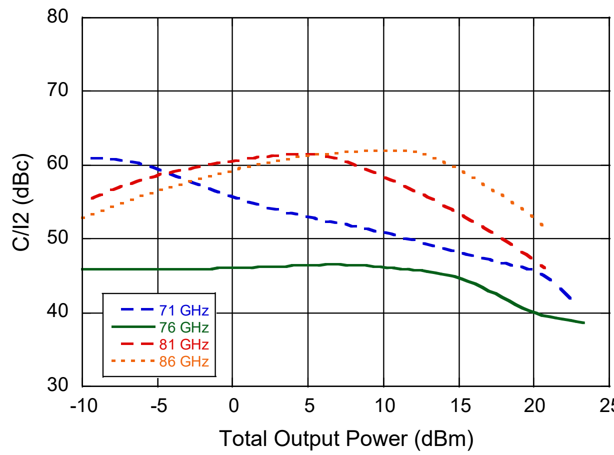
C/I2 vs. Total Output Power[10], RF = 86 GHz



C/I2 vs. Total Output Power[8], +25°C



C/I2 vs. Total Output Power[9], +25°C

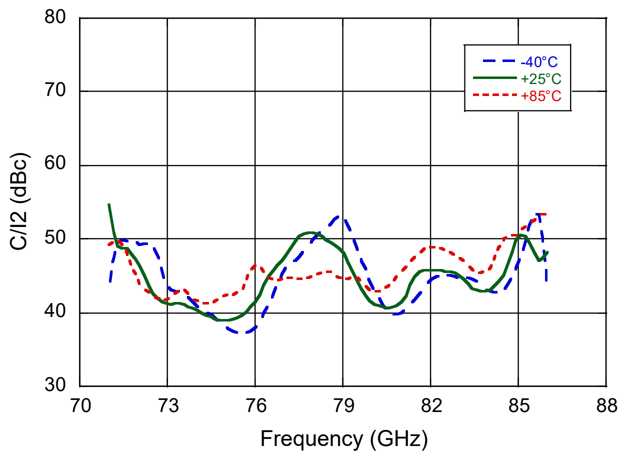


8. Output power controlled by RF buffer current.

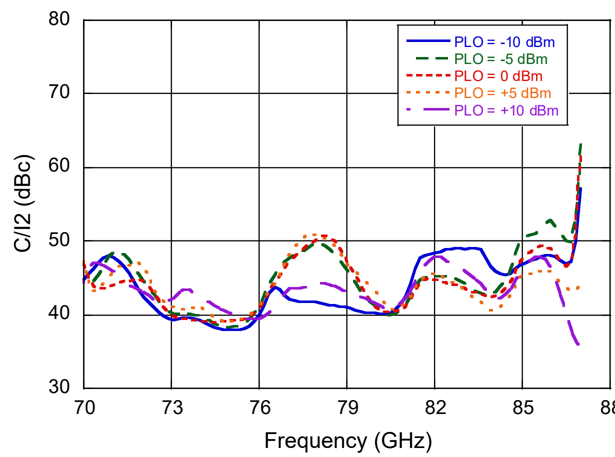
9. Output power controlled by RF buffer and PA currents.

Typical Performance Curves over Temp. at Total P_{IN} = -10 dBm, IF = 21.4 and 26 MHz

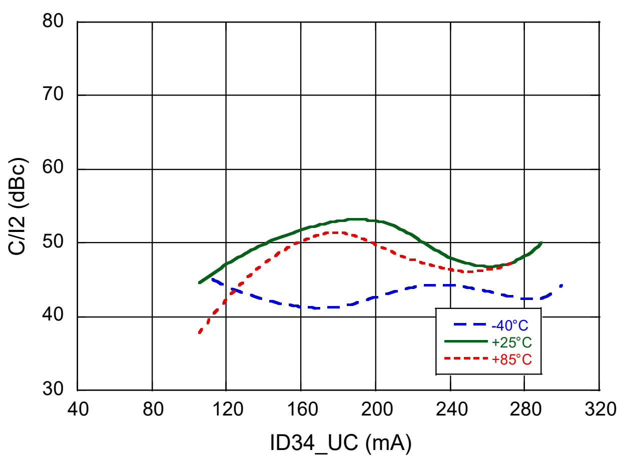
C/I2 at Nominal Bias



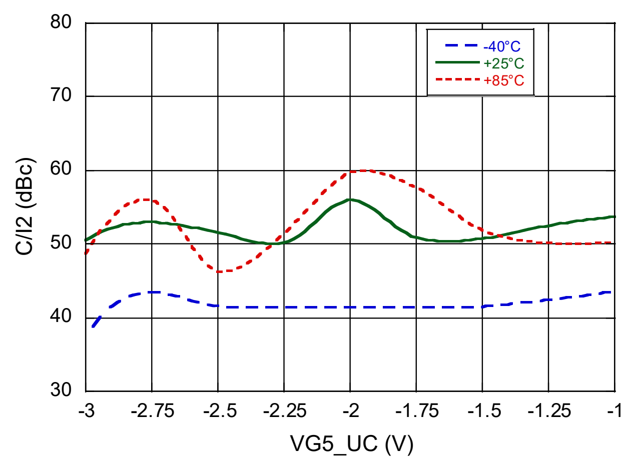
C/I2 vs. LO Power



C/I2 vs. LO Bias, RF = 86 GHz

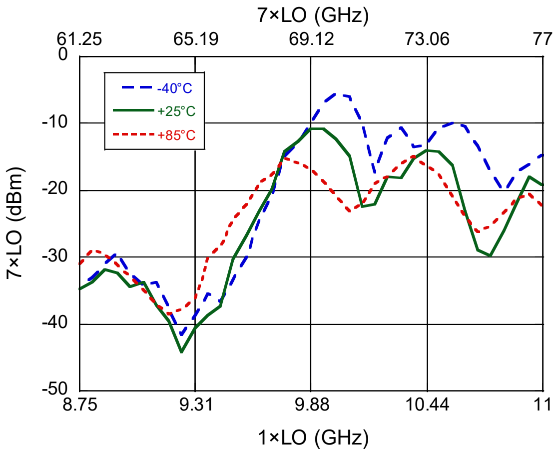


C/I2 vs. Mixer Bias, RF = 86 GHz

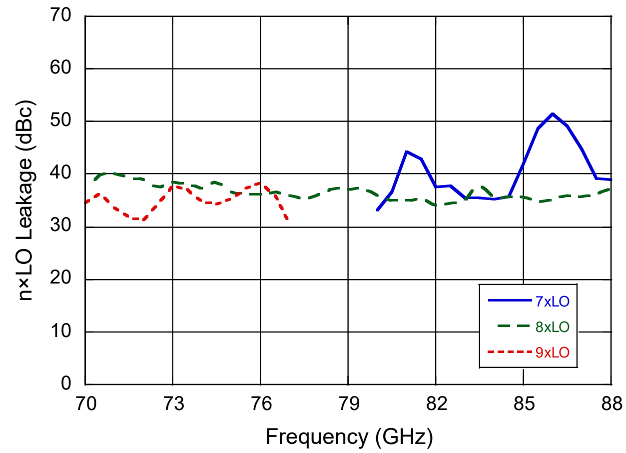


Typical Performance Curves over Temperature, P_{IN} = -10 dBm, IF = 21.4 MHz

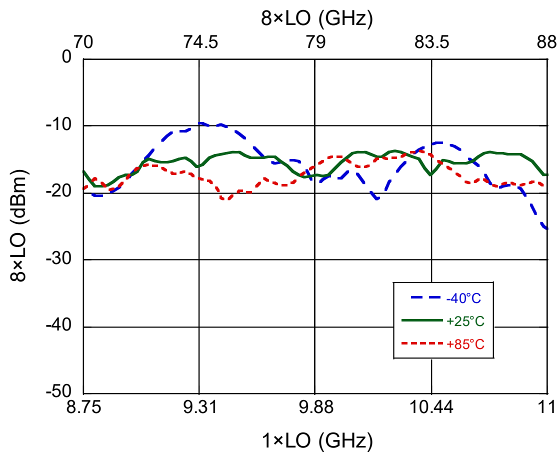
7×LO Leakage at Nominal Bias



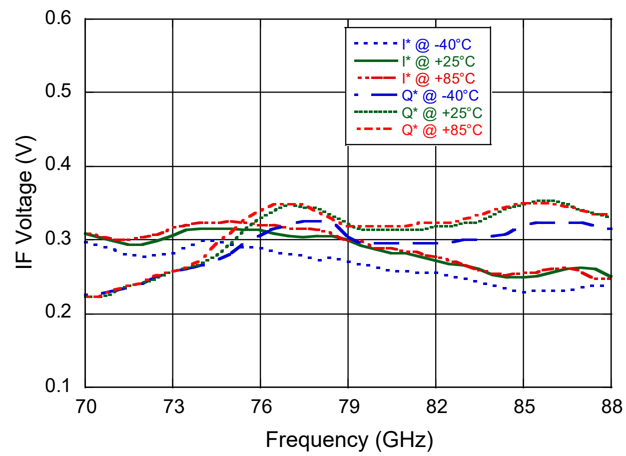
7,8,9×LO Spurs at +25°C



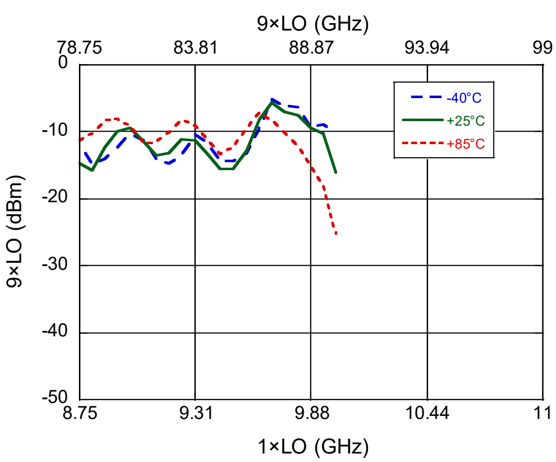
8×LO Leakage at Nominal Bias



8×LO Nulling Voltages, I and Q = 0.2 V

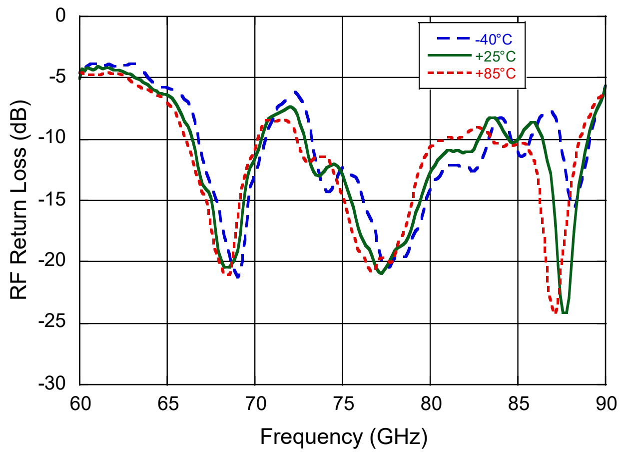


9×LO Leakage at Nominal Bias

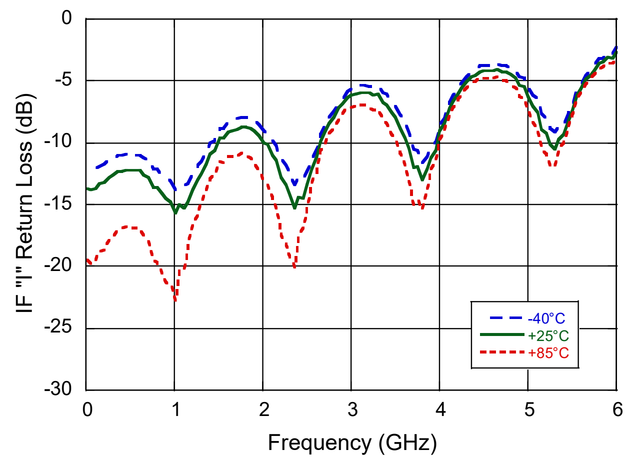


Typical Performance Curves over Temperature

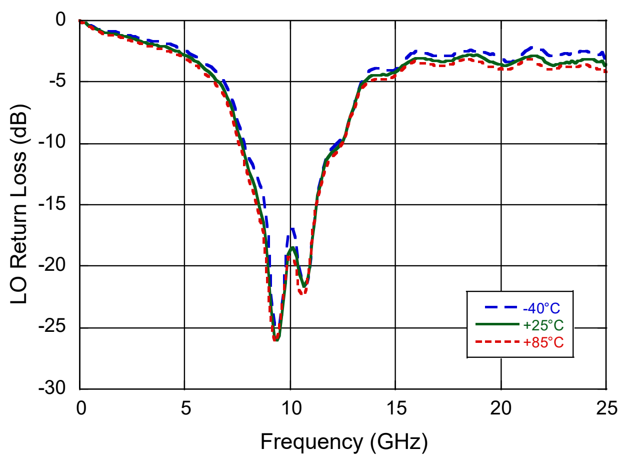
RF Return Loss



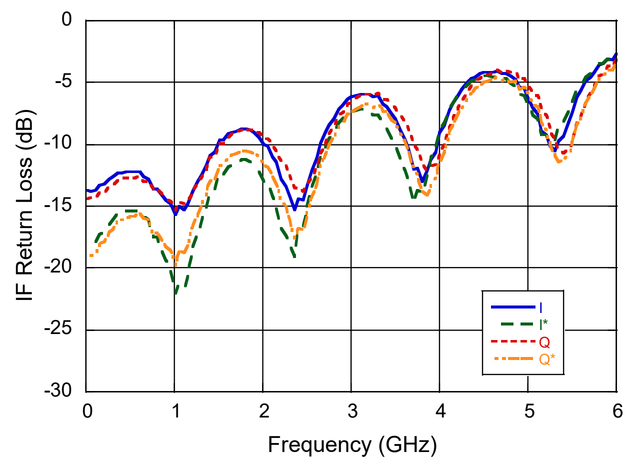
IF "I" Return Loss



LO Return Loss

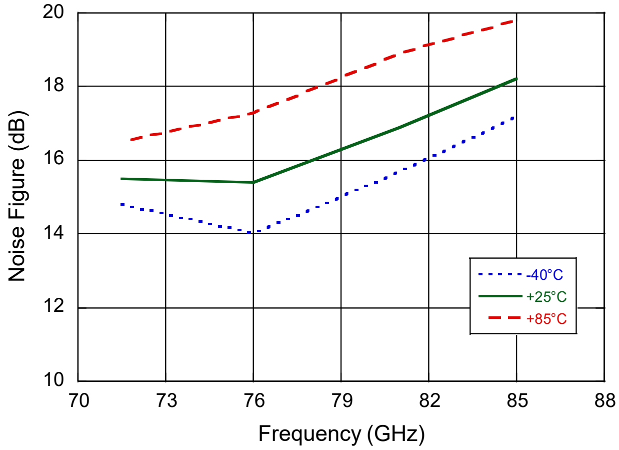


All IF Return Loss at +25°C

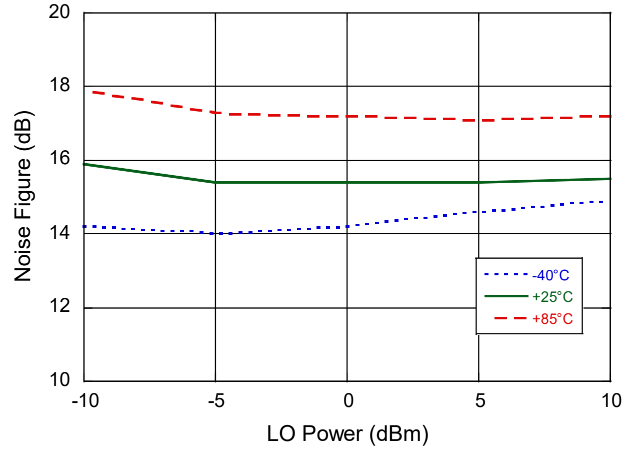


Typical Performance Curves over Temperature

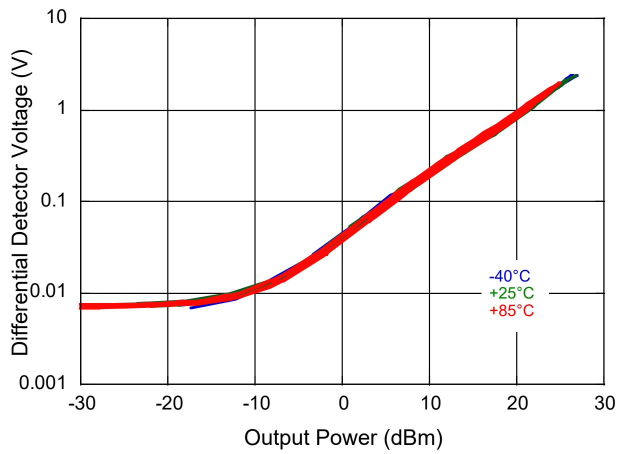
Noise Figure, IF = 2.25 GHz



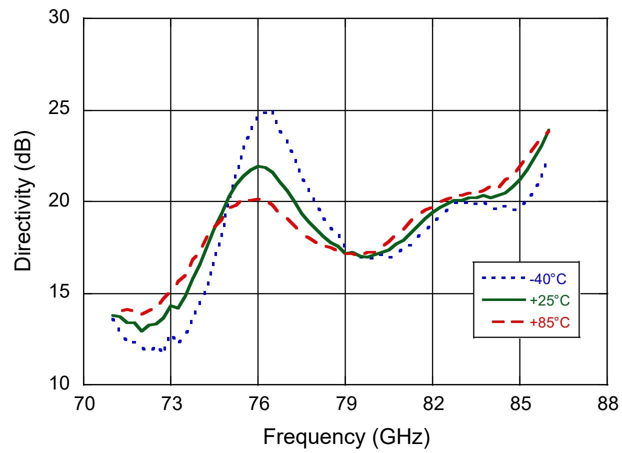
Noise Figure vs. LO Power, RF = 76 GHz, IF = 2.25 GHz



Power Detector, RF = 71, 76, 81, 86 GHz

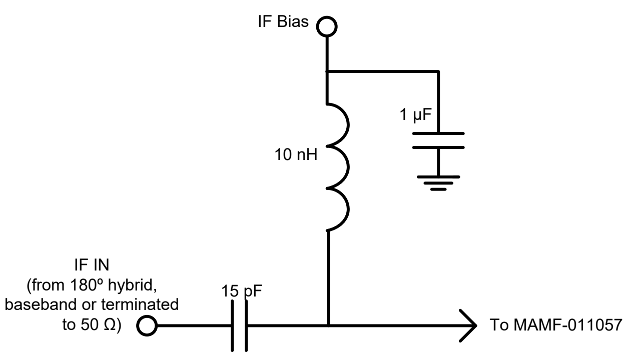


Detector Directivity at Nominal Bias



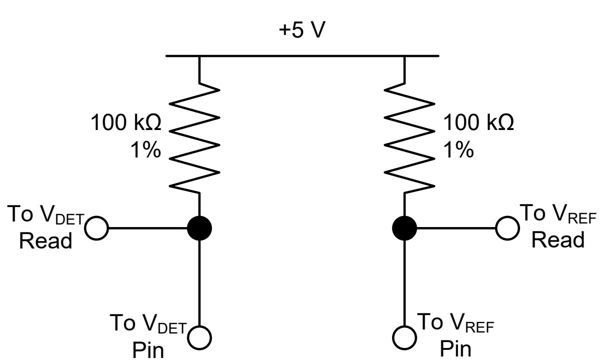
LO Nulling

LO nulling is achieved by applying a fixed voltage on ports I and Q while tuning the voltages on I* and Q*. Typically I and Q are set to 0.2 V; however, any voltage between -1 V and +1 V may be used. DACs with a common mode voltage offset may be sufficient for the fixed voltage. If a separate voltage is used, bias tees are required for the implementation of LO suppression. Below is an example of a potential bias tee however depending on the input frequency (be it baseband or at an intermediate frequency) the inductor may require tuning to generate the appropriate performance. Depending on the resolution of the DAC, suppression of the LO should be able to reach with minimal effort values exceeding -30 dBc.

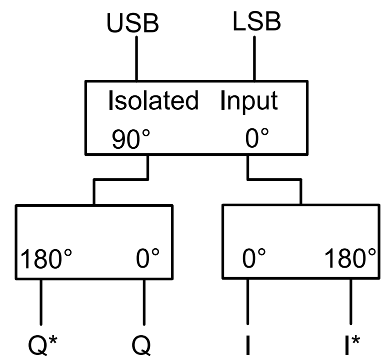


Detector Application Schematic

As shown in the schematic below, the power detector is implemented by providing 5 V bias and measuring the difference in output voltage. This measure can be achieved by means of either standard op-amp in a differential mode configuration or analog-to-digital converters.



LSB/USB Operation

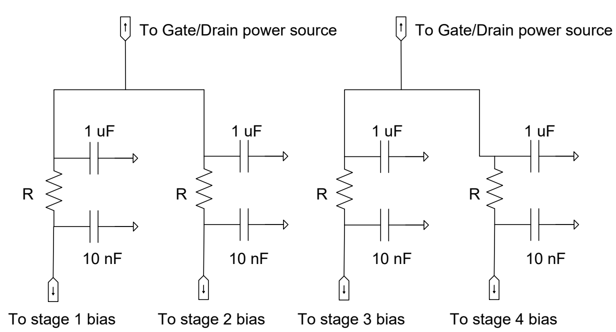


Combined DC Stages

There is a number of bias stages that are accessible for the user. It is not necessary to have individual bias supplies for each stage. Combining stages of similar purpose creates a stable system. That is, the RF buffer stages can be combined (Vx1_UC and Vx2_UC), the LO multiplier stages can be combined (Vx3_UC and Vx4_UC) and lastly the PA stages can be combined (Vx1_PA, Vx2_PA, Px3_PA and Vx4_PA).

It is not recommended to directly connect stages together, rather the stages should have some isolation between them. On the gates, a 10 nF capacitor and a series 10 Ω resistor should be used before combining the stages. On the drains, a 10 nF capacitor should be used. Evaluation boards also have a ferrite bead with impedance of 100 Ω at 100 MHz to minimize feedback through PCB having an effect on the performance of the device. The ferrite bead minimizes any voltage drop that could occur if a resistor is used.

If there are multiple capacitors in parallel to ground it is recommended that one of the capacitors has a small series resistor to dequeue the network to avoid parallel capacitor resonances.



Bias Sequencing

All gates should be pinched off (VG < -2 V) before the drain voltage (VD = 4 V) is applied. This requirement includes VG5 even though there is no external drain voltage. The gate voltages should then be adjusted as per bias table on Page 3. The current will change when LO is applied to stages three and four.
The currents that are listed are the quiescent currents for operation. This is these currents are without RF applied. For maximum performance, it is recommended to set the drain quiescent drain current and then fix the gate voltage for this quiescent current before applying the RF signals. This will ensure the best performance for the device.

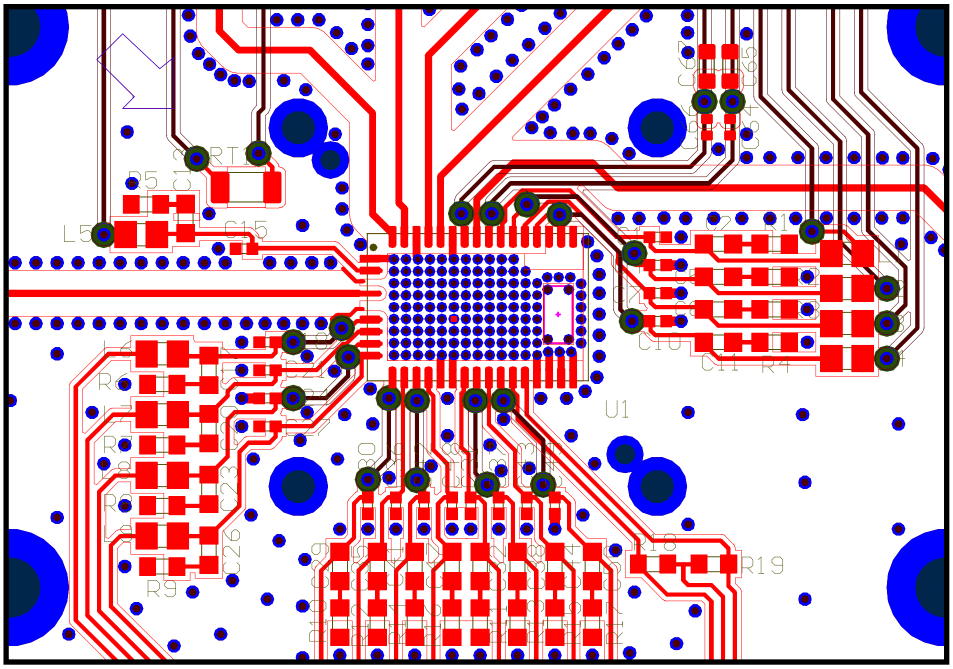
Package Alignment

The SMD package is ideal for pick and place assembly. The package should self align. It is recommended that a solder stencil is used complying with Application Note S2083. To minimize solder flowing into waveguide area, stencil can be inset an additional 25 µm.

Reflow Profile

This package is capable of lead free reflow. The recommended reflow profile depends on the solder used however Application Note S2083 has guidelines that can be applied to this product.

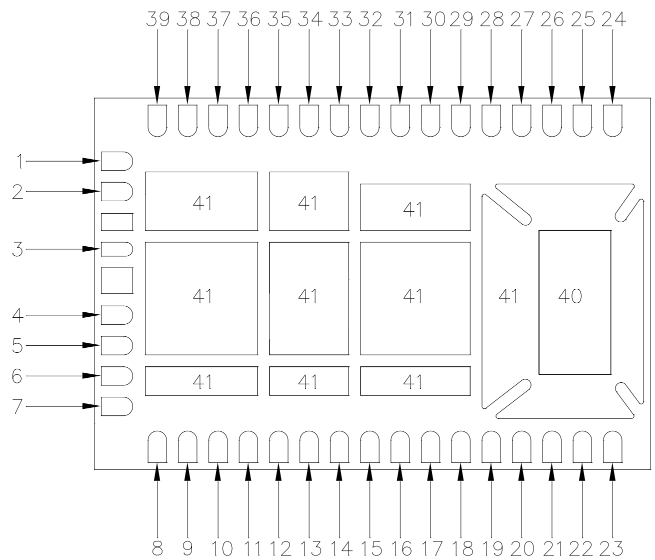
Layout of Evaluation Board



PCB Layout Recommendations

The gerbers, DXF and Altium files for the evaluation board are available on request. It is recommended that all traces are separated to minimize on board coupling. A simple way to separate traces is to have them running on different PCB layers on the board. The image above is a capture of the evaluation board.

Pad Diagram



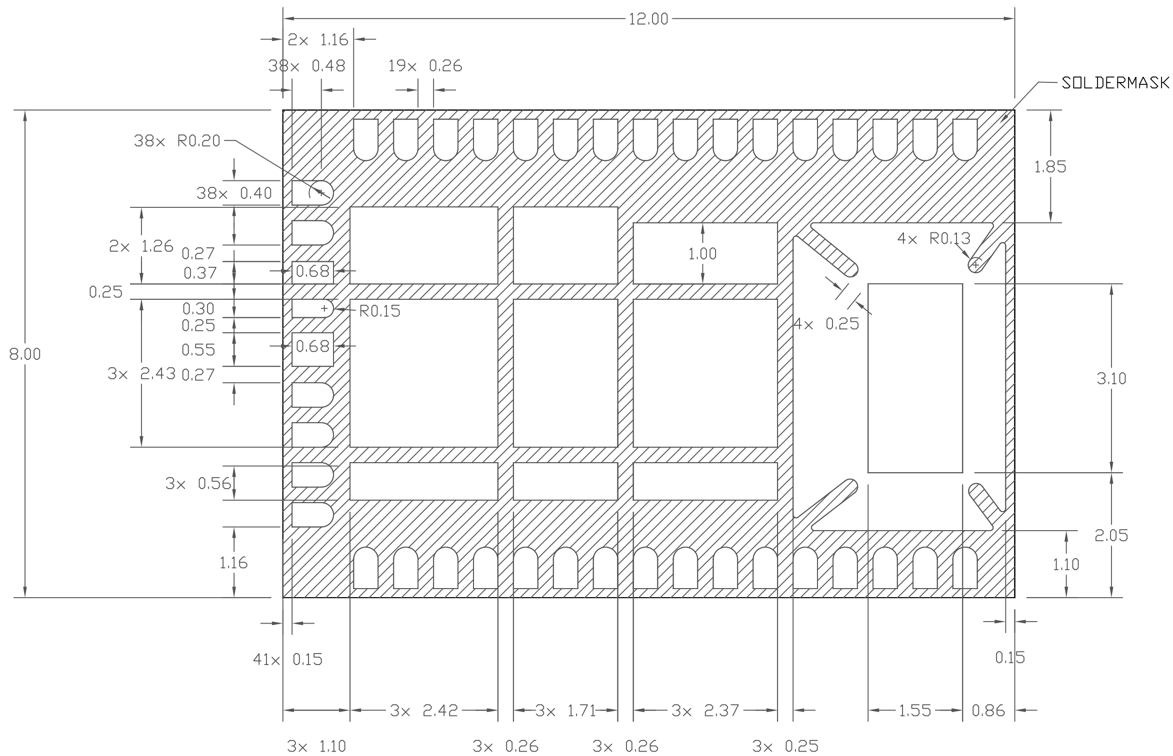
Bottom Layer Viewed From The Top

Pin Table

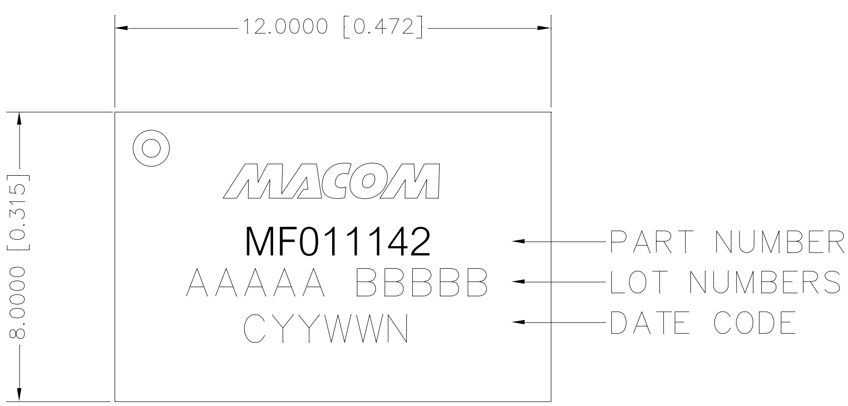
Pin #	Pin Name	Function	Pin #	Pin Name	Function
1	NC[10]	Not Connected	22	NC[10]	Not Connected
2	VG5_UC	Mixer Bias	23	NC[10]	Not Connected
3	LO_IN	LO Input	24	NC[10]	Not Connected
4	VG3_UC	LO Multiplier	25	NC[10]	Not Connected
5	VD3_UC	LO Multiplier	26	NC[10]	Not Connected
6	VG4_UC	LO Multiplier Post Amplifier	27	VD4_PA	Stage 4 Power Amplifier
7	VD4_UC	LO Multiplier Post Amplifier	28	VD3_PA	Stage 3 Power Amplifier
8	VG1_UC	RF Buffer Stage 1	29	VD2_PA	Stage 2 Power Amplifier
9	VD1_UC	RF Buffer Stage 1	30	VD1_PA	Stage 1 Power Amplifier
10	VG2_UC	RF Buffer Stage 2	31	NC[10]	Future Envelope Detector VSS
11	VD2_UC	RF Buffer Stage 2	32	NC[10]	Future Envelope Detector Output
12	NC[10]	Not Connected	33	NC[10]	Future Envelope Detector VDD
13	NC[10]	Not Connected	34	NC[10]	Not Connected
14	VG1_PA	Stage 1 Power Amplifier	35	I*	IF Port
15	VG2_PA	Stage 2 Power Amplifier	36	I	IF Port
16	VG3_PA	Stage 3 Power Amplifier	37	NC[10]	Not Connected
17	VG4_PA	Stage 4 Power Amplifier	38	Q	IF Port
18	VREF	Reference Detector Diode	39	Q*	IF Port
19	VDET	Detector Diode	40	RF_OUT	RF Output
20	NC[10]	Not Connected	41	Paddle[11]	Ground
21	NC[10]	Not Connected			

10.For optimum RF performance, all NCs should be terminated to ground.
11.The exposed paddle centered on the package bottom must be connected to RF, DC and thermal ground.

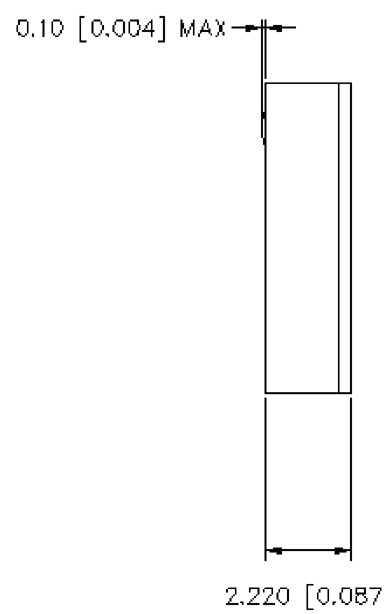
Layout Dimensions



Bottom Layer Viewed From The Top



Top View



Package Thickness

Major dimensions provided are in millimeters [inches]
DXF of footprint is available on request
Reference Application Note M538/S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level (MSL) 3 requirements.