## Features

- 2-Stage LNA and High Power Switch
- Bypass Switch on Second LNA Stage
- High RF Input Power:

160 W CW @ +105º , 2.6 GHz

- Noise Figure:
1.2 dB @ 2.6 GHz
$1.5 \mathrm{~dB} @ 3.5 \mathrm{GHz}$
1.8 dB @ 4.5 GHz
- Gain, High Gain Mode:

34 dB @ 2.6 GHz
33 dB @ 3.5 GHz
32 dB @ 4.5 GHz

- Output IP3: 35 dBm (High Gain Mode)
- Lead-Free 5 mm 32-lead HQFN
- Integrated ESD Protection
- RoHS* Compliant


## Applications

- High Power TDD 4G \& 5G Basestation
- Wireless Infrastructure
- TDD-based Communication System


## Description

The MAMF-011139 is a compact surface mount module containing a PIN diode switch and two low noise amplifiers assembled in a 5 mm 32-lead HQFN plastic package.

Some DC bias and matching SMT components are required for PIN switch operation and optimized noise figure. The second LNA, LNA2, may be bypassed through an integrated switch. LNA2 is powered down when bypassed.

Ordering Information ${ }^{1,2}$

| Part Number | Package |
| :---: | :---: |
| MAMF-011139-TR1000 | 1K Reel |
| MAMF-011139-001SMB | Sample Board |

[^0]
## Functional Schematic



Pin Configuration ${ }^{3,4}$

| Pin \# | Pin Name | Description |
| :---: | :---: | :---: |
| $1-4,6-10,12,14$, <br> $16,22,23,25$, <br> 27,32 | N/C $^{3}$ | No Connection |
| 5 | RF $_{\text {IN }}$ | Common RF Input / Bias |
| 11 | RX | RX Switch Output |
| $13,18,21,29,30$ | GND | RF Ground |
| 15 | LNA1 ${ }_{\text {IN }}$ | LNA1 Input |
| 17 | EN | LNA1/2 Enable |
| 19 | V $_{\text {DD }}$ | Drain Supply |
| 24 | RF $_{\text {OUT }}$ | LNA2 Output |
| 26 | BP $_{\text {CONTROL }}$ | Bypass Switch Control |
| 28 | V $_{\text {C }}$ | RX/TX Switch Control |
| 31 | LOAD $^{\text {TX Switch Output }}$ |  |

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
[^1]Electrical Specifications: $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{BP}_{\text {control }}=3.3 \mathrm{~V}, \mathrm{EN}=0 \mathrm{~V}$ See RX/TX Switch Bias Table

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input RF Power @ $+105^{\circ} \mathrm{C}$ RF ${ }_{\text {IN }}$ - LOAD 200 mA Bias Current | 2.6 GHz 3.5 GHz 4.5 GHz | W | - | $\begin{aligned} & 160 \\ & 140 \\ & 125 \end{aligned}$ | - |
| Input RF Power @ $+105^{\circ} \mathrm{C}$ RF ${ }_{\text {IN }}$ - LOAD 100 mA Bias Current | 2.6 GHz 3.5 GHz 4.5 GHz | W | - | $\begin{aligned} & 120 \\ & 105 \\ & 95 \end{aligned}$ | - |
| Switch Insertion Loss $R F_{\text {IN }}-\text { LOAD }$ | $\begin{aligned} & 2.6 \mathrm{GHz} \\ & 3.5 \mathrm{GHz} \\ & 4.5 \mathrm{GHz} \end{aligned}$ | dB | - | $\begin{aligned} & 0.3 \\ & 0.4 \\ & 0.6 \end{aligned}$ | $\overline{0.7}$ |
| Noise Figure in Both Modes RF ${ }_{\text {IN }}$ - RF $_{\text {out }}$ | 2.6 GHz 3.5 GHz 4.5 GHz | dB | - | $\begin{aligned} & 1.2 \\ & 1.5 \\ & 1.8 \end{aligned}$ | $\overline{1.9}$ |
| Input Return Loss in Both Modes RF $_{\text {IN }}$. FFout $^{\text {on }}$ | 2.6 GHz 3.5 GHz 4.5 GHz | dB | - | 12 22 12 | - |
| Output Return Loss in Both Modes $R F_{\text {IN }}$. $\mathrm{RF}_{\text {OUT }}$ | $\begin{aligned} & 2.6 \mathrm{GHz} \mathrm{HG} / \mathrm{LG} \\ & 3.5 \mathrm{GHz} \mathrm{HG} / \mathrm{LG} \\ & 4.5 \mathrm{GHz} \mathrm{HG} / \mathrm{LG} \end{aligned}$ | dB | - | $\begin{aligned} & 10 / 17 \\ & 15 / 13 \\ & 15 / 17 \end{aligned}$ | - |
| Gain in High Gain Mode RF $_{\text {IN }}$. RFout | $\begin{aligned} & 2.6 \mathrm{GHz} \\ & 3.5 \mathrm{GHz} \\ & 4.5 \mathrm{GHz} \end{aligned}$ | dB | $2 \overline{-7}$ | $\begin{aligned} & 34.1 \\ & 32.5 \\ & 32.0 \end{aligned}$ | - |
| Gain in Low Gain Mode $\mathrm{RF}_{\text {In }}$. $\mathrm{RF}_{\text {out }}$ | 2.6 GHz 3.5 GHz 4.5 GHz | dB | - | $\begin{aligned} & \hline 20.1 \\ & 19.3 \\ & 18.0 \end{aligned}$ | - |
| Isolation $R F_{\mathbb{I N}_{N}}-\mathrm{LNA} 1_{\mathbb{N}}$ | $\begin{gathered} \hline \text { Switch State }=\mathrm{RF}_{\mathbb{I N}}-\mathrm{LOAD} \\ 2.6 \mathrm{GHz} \\ 3.5 \mathrm{GHz} \\ 4.5 \mathrm{GHz} \end{gathered}$ | dB | - | $\begin{aligned} & 46 \\ & 47 \\ & 45 \end{aligned}$ | - |
| Output IP3 in High Gain Mode RF $_{\text {IN }}$. FF $_{\text {out }}$ | $P_{\text {OUt }}=+10 \mathrm{dBm}$ per tone, 11 MHz spacing | dBm | - | 35 | - |
| Output IP3 in Low Gain Mode RFin . RFout | $P_{\text {OUt }}=+3 \mathrm{dBm}$ per tone, 11 MHz spacing | dBm | - | 29.5 | - |
| Output P1dB in High Gain Mode | $\mathrm{RF}_{\text {IN }}$. $\mathrm{RF}_{\text {OUT }}$ | dBm | - | 19 | - |
| Output P1dB in Low Gain Mode | RFin - $\mathrm{RF}_{\text {OUT }}$ | dBm | - | 15.3 | - |
| $V_{\text {DD }}$ Bias Current | High Gain Mode Low Gain Mode | mA | - | $\begin{gathered} 108 \\ 44 \end{gathered}$ | - |
| Control Voltage | Logic High Logic Low | V | $\begin{gathered} 1.2 \\ 0 \end{gathered}$ | - | $\begin{gathered} 3.45 \\ 0.6 \end{gathered}$ |
| Logic Input Current | Logic High Logic Low | $\mu \mathrm{A}$ | - | $\begin{gathered} 60 \\ 0.01 \end{gathered}$ | - |

## RX/TX Switch Bias Table

| $\mathbf{R F}_{\text {IN }}$ - LOAD | RF $_{\text {IN }}-\mathbf{R F}_{\text {OUT }}$ | LOAD | $\mathbf{R X}$ | $\mathbf{V c}$ | $\mathbf{R F}_{\text {IN }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ON | OFF | $0 \vee(-100 \mathrm{~mA})$ | $+48 \mathrm{~V}(10 \mathrm{~mA})$ | $0 \vee(-10 \mathrm{~mA})$ | $5 \mathrm{~V}(100 \mathrm{~mA})$ |
| OFF | ON | $+48 \mathrm{~V}(0 \mathrm{~mA})$ | $0 \vee(-100 \mathrm{~mA})$ | $+48 \mathrm{~V}(0 \mathrm{~mA})$ | $5 \mathrm{~V}(100 \mathrm{~mA})$ |

## LNA Logic Truth Table ${ }^{5}$

| Mode | EN | BP control | Note |
| :---: | :---: | :---: | :---: |
| High Gain mode | Low | Low | LNA1 and LNA2 ON, Bypass Switch OFF |
| Low Gain mode | Low | High | LNA1 ON, LNA2 OFF, Bypass Switch ON |
| High Isolation mode | High | Low | LNA1 and LNA2 OFF, Bypass Switch OFF |
| Low Isolation mode | High | High | LNA1 and LNA2 OFF, Bypass Switch ON |

5. If $\mathrm{V}_{\mathrm{DD}}$ pin is used to turn the LNAs ON and OFF, the logic pins need to stay at Logic Low during $\mathrm{V}_{\mathrm{DD}}$ ramp up and ramp down.

## Absolute Maximum Ratings ${ }^{6,7,8}$

| Parameter | Absolute Maximum |
| :---: | :---: |
| RF Input Power <br> RF $_{\text {IN }}-R X$ <br> LNA $_{1 N}-\mathrm{RF}_{\text {out }}$ <br> RF $_{\text {IN }}-$ LOAD | $49 \mathrm{dBm} @ 85^{\circ} \mathrm{C}$ <br> 19 dBm |
| Switch Reverse Voltage (RF \& DC) | See Power Derating Curves |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $T_{J} \leq+150^{\circ} \mathrm{C}(\mathrm{LNA})$ and $\mathrm{T}_{J} \leq+175^{\circ} \mathrm{C}$ (Switch) will ensure MTTF $\gg 1 \times 10^{6}$ hours.
9. LNA Junction Temperature $\left(T_{J}\right)=T_{C}+\theta_{J C} *\left(P_{D I S S}\right)$ where $P_{D I S S}$ is the total DC \& RF dissipated power.

- LNA: Typical thermal resistance $\left(\Theta_{\mathrm{JC}}\right)=33.4^{\circ} \mathrm{C} / \mathrm{W}$.


## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged

| Parameter | Rating | Standard |
| :---: | :---: | :---: |
| Human Body <br> Model (HBM) | Class 1B | ESDA/JEDEC <br> JS-001 |
| Charged Device <br> Model (CDM) | Class C3 | ESDA/JEDEC <br> JS-002 | by static electricity.

## Typical Performance Curves

$\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$ (unless otherwise indicated)

ANT to LOAD Input Power Derating Curve @ 2.7GHz


ANT to LOAD Input Power Derating Curve over Frequency @ $105^{\circ} \mathrm{C}$ Case Temp


ANT to LOAD Input Power Derating Curve over Frequency @ $85^{\circ} \mathrm{C}$ Case Temp


ANT to LOAD Input Power Derating Curve over Frequency @ $120^{\circ} \mathrm{C}$ Case Temp


ANT to LOAD Input Power Derating Curve over Reverse Bias Voltage @ 2.7GHz


## PCB Layout



Parts List

| Part | Value | Case Style (Min Rating) |
| :---: | :---: | :---: |
| $\mathrm{C} 1, \mathrm{C} 2$ | 6.8 pF | $0603(\geq 250 \mathrm{~V})$ |
| C 3 | 10 pF | $0402(\geq 100 \mathrm{~V})$ |
| C5 | 15 pF | 0603 |
| C4,C14 | $0.1 \mu \mathrm{~F}$ | 0402 |
| $\mathrm{C} 6, \mathrm{C} 7, \mathrm{C} 8, \mathrm{C} 9$ | 15 pF | $0402(\geq 100 \mathrm{~V})$ |
| C10 | 4.7 pF | 0402 |
| C12,C13,C15,C16 | DNP | 0402 |
| C21 | 0.4 pF | 0402 |
| L1,L2,L3,L5 | 33 nH | 0402 |
| L4 | Jumper | 0402 |
| R1 | $40.2 \Omega$ | $2512(\geq 1 \mathrm{~W})$ |
| R2 | $0 \Omega$ | 1206 |
| R3 | $4.7 \mathrm{k} \Omega$ | $2512(\geq 1 \mathrm{~W})$ |
| R4 | $0 \Omega$ | 0402 |
| R5 | $100 \Omega$ | 0402 |

Application Schematic


## Typical Performance Curves

$\mathrm{P}_{\text {IN }}=-35 \mathrm{dBm}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$ (unless otherwise indicated)

LNA Gain over swept Frequency (\& Temp.) in High Gain Mode


RFin Port Return Loss over swept Frequency (\& Temp.) in High Gain Mode


RFout Port Return Loss over swept Frequency (\& Temp.) in High Gain Mode


LNA Gain over swept Frequency (\& Temp.) in Low Gain Mode


RFIN ${ }_{\text {IN }}$ Port Return Loss over swept Frequency (\& Temp.) in Low Gain Mode


RFout Port Return Loss over swept Frequency (\& Temp.) in Low Gain Mode


## Typical Performance Curves

$P_{\text {IN }}=-35 \mathrm{dBm}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$ (unless otherwise indicated)

LNA Noise Figure over swept Frequency (\& Temp.) in High Gain Mode


LNA1 ${ }_{\text {IN }}$ to RFout Isolation over swept Frequency (\& Temp.) in High Gain Mode

$R F_{I N}$ to LNA1 ${ }_{\text {IN }}$ Isolation over swept Frequency (\& Temp.)


LNA Noise Figure over swept Frequency (\& Temp.) in Low Gain Mode


LNA1 ${ }_{\text {IN }}$ to $R F_{\text {out }}$ Isolation over swept Frequency (\& Temp.) in Low Gain Mode


## Typical Performance Curves

$\mathrm{P}_{\text {IN }}=-35 \mathrm{dBm}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$ (unless otherwise indicated)

LNA Gain over swept Output Power (\& Temp.) at 3.5 GHz in High Gain Mode


OIP3 over swept Frequency (\& Temp.) with PiN $/$ Tone $=-35 \mathrm{dBm} \& 10 \mathrm{MHz}$ tone spacing in HGM.


OIP3 over swept Frequency (\& Temp.) with $\mathrm{P}_{\text {out }} /$ Tone $=10 \mathrm{dBm} \& 11 \mathrm{MHz}$ tone spacing in HGM.


LNA Gain over swept Output Power (\& Temp.) at 3.5 GHz in Low Gain Mode


OIP3 over swept Frequency (\& Temp.) with PiN $/$ Tone $=-25 \mathrm{dBm} \& 10 \mathrm{MHz}$ tone spacing in LGM.


OIP3 over swept Frequency (\& Temp.) with $\mathrm{P}_{\mathrm{out}} /$ Tone $=3 \mathrm{dBm} \& 11 \mathrm{MHz}$ tone spacing in LGM.


## Typical Performance Curves

$P_{\text {IN }}=-10 \mathrm{dBm}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$ (unless otherwise indicated)

Switch Insertion Loss over swept Frequency (\&
Temp.)


RF ${ }_{\text {IN }}$ Port Return Loss over swept Frequency (\& Temp.)

$R F_{I N}$ to $R F_{\text {out }}$ Isolation over swept Frequency (\& Temp.)


LOAD Port Return Loss over swept Frequency (\& Temp.)


Rev. V1

## Lead-Free 5 mm 32-Lead HQFN ${ }^{\dagger}$



ALL DIMENSIONS SHOWN AS in[mm]
$\dagger^{\dagger}$ Reference Application Note M538 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg.

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[^0]:    1. Reference Application Note M513 for reel size information.
    2. All sample boards include 3 loose parts.
[^1]:    * Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

