

MAGB-103438-020S0P



GaN Amplifier 50 V, 4 W AVG
3.4 - 3.8 GHz

Rev. V2

Features

- Optimized for Cellular Base Station Applications
- Designed for Digital Predistortion Error Correction Systems
- Suitable for Quadrature Combined & Symmetrical Doherty Driver Amplifier Applications
- High Terminal Impedances for Broadband Performance
- 50 V Operation
- 100% RF Tested
- RoHS* Compliant

Description

The MAGB-103438-020S0P is a GaN HEMT D-mode amplifier pair designed for use as a quadrature combined or symmetrical Doherty driver amplifier in base station applications in the frequency range of 3.4 - 3.8 GHz with modulated signal operation. This device supports pulsed and linear operation with peak output power levels to 25 W (44.1 dBm) in a plastic package.

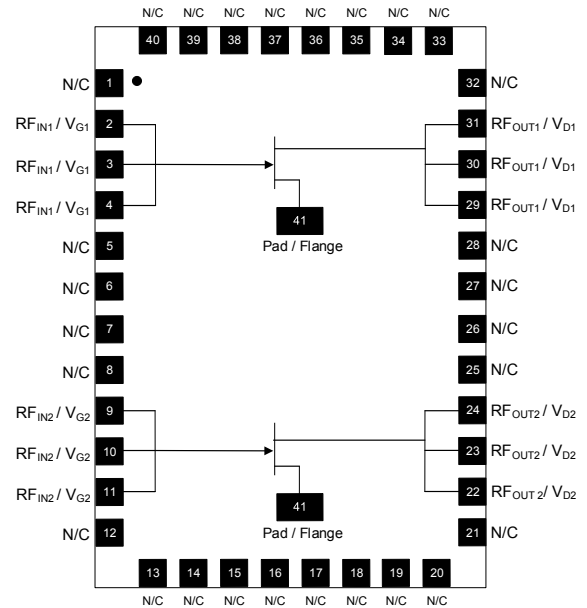
Typical Quadrature Combined Performance:

- WCDMA 3GPP TM1 64 DPCH 9.9 dB PAR @ 0.01% CCDF. $V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 45\text{ mA}$, $P_{OUT} = 36\text{ dBm}$

Frequency (MHz)	G_P (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
3400	17.2	29	8.0	-37	-25
3500	17.3	28	8.2	-37	-26
3600	16.9	26	8.3	-37	-29



Functional Schematic



Pin Configuration

Pin #	Pin Name	Function
1, 5-8, 12-21, 25-28, 32-40	N/C	No Connection
2-4	RF _{IN1} / V _{G1}	RF Input / Gate
9-11	RF _{IN2} / V _{G2}	RF Input / Gate
22-24	RF _{OUT2} / V _{D2}	RF Output / Drain
29-31	RF _{OUT1} / V _{D1}	RF Output / Drain
41	Pad ¹	Ground / Source

1. The exposed pad centered on the package bottom must be connected to RF and DC ground. This path must also provide a low thermal resistance heat path.

Ordering Information

Part Number	Package
MAGB-103438-020S0P	Bulk Quantity
MAGB-1B3438-020S0P	Dual Path Class-AB Sample Board
MAGB-103438-020STP	1000 Piece Reel

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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RF Electrical Characteristics: $T_C = 25^\circ\text{C}$, $V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 45\text{ mA}$
Note: Performance in MACOM Quadrature Combined Circuit, 50 Ω system

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Small Signal Gain	Pulsed ² , 3500 MHz	G_{SS}	-	18	-	dB
Saturated Output Power	Pulsed ² , 3500 MHz	P_{SAT}	-	44.3	-	dBm
Drain Efficiency at Saturation	Pulsed ² , 3500 MHz	η_{SAT}	-	54	-	%
AM/PM	Pulsed ² , 3500 MHz	Φ	-	-5	-	°
Modulated Peak Power	WCDMA ³ , 3500 MHz	P_{3dB}^4	-	44.5	-	dBm
VBW Resonance Point	IMD 3rd Order Inflection Point	VBW_{RES}	-	200	-	MHz
Gain Flatness in 60 MHz	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	G_F	-	0.2	-	dB
Gain Variation (-25°C to +105°C)	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	ΔG	-	± 0.02	-	dB/°C
Power Variation (-25°C to +105°C)	Pulsed ² , 3500 MHz	ΔP_{1dB}	-	± 0.01	-	dB/°C
Ruggedness: Output Mismatch	All phase angles	Ψ	VSWR = 10:1, No Device Damage			

RF Electrical Specifications: $T_A = 25^\circ\text{C}$, $V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 40\text{ mA}$
Note: Performance in MACOM Quadrature Combined Production Test Fixture, 50 Ω system

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Power Gain	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	G_P	14	17.5	-	dB
Drain Efficiency	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	η	18	25	-	%
Output PAR @ 0.01% CCDF	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	PAR	6.4	8	-	dB
Adjacent Channel Power Ratio	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	ACPR	-	-35	-25	dBc
Input Return Loss	WCDMA ³ , 3500 MHz, $P_{OUT} = 36\text{ dBm}$	IRL	-	-16	-9	dB

2. Pulse details: 100 μs pulse width, 1 ms period, 10% Duty Cycle

3. Modulated Signal: 3.84 MHz, WCDMA 3GPP TM1 64 DPCH, 9.9dB PAR @ 0.01% CCDF.

4. $P_{3dB} = P_{OUT} + 7\text{ dB}$ where P_{OUT} is the average output power measured using a modulated signal³ where the output PAR is compressed to 7 dB @ 0.01% probability CCDF.

DC Electrical Characteristics: $T_A = 25^\circ\text{C}$ (per side of symmetrical device)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Drain-Source Leakage Current	$V_{GS} = -8\text{ V}$, $V_{DS} = 130\text{ V}$	I_{DLK}	-	-	2.04	mA
Gate-Source Leakage Current	$V_{GS} = -8\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GLK}	-	-	1.02	mA
Gate Threshold Voltage	$V_{DS} = 50\text{ V}$, $I_D = 2.04\text{ mA}$	V_T	-2.6	-2.1	-1.6	V
Gate Quiescent Voltage	$V_{DS} = 50\text{ V}$, $I_D = 40\text{ mA}$	V_{GSQ}	-2.4	-1.9	-1.4	V
On Resistance	$V_{DS} = 2\text{ V}$, $I_D = 15\text{ mA}$	R_{ON}	-	2.4	-	Ω
Maximum Drain Current	$V_{DS} = 7\text{ V}$ pulsed, pulse width 300 μs	$I_{D,MAX}$	-	1.1	-	A

Absolute Maximum Ratings^{5,6,7,8,9} (Quadrature Combined Configuration)

Parameter	Absolute Maximum
Drain Source Voltage, V_{DS}	130 V
Gate Source Voltage, V_{GS}	-10 to 3 V
Gate Current, I_G	4.04 mA
Storage Temperature Range	-65°C to +150°C
Case Operating Temperature Range	-40°C to +120°C
Channel Operating Temperature Range, T_{CH}	-40°C to +225°C
Absolute Maximum Channel Temperature	+225°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation above maximum operating conditions.
7. Operating at drain source voltage $V_{DS} < 55$ V will ensure $MTTF > 1 \times 10^7$ hours.
8. Operating at nominal conditions with $T_{CH} \leq 225^\circ\text{C}$ will ensure $MTTF > 1 \times 10^7$ hours.
9. $MTTF$ may be estimated by the expression $MTTF$ (hours) = $A e^{[B + C/(T+273)]}$, where T is the channel temperature in degrees Celsius., $A = 3.686$, $B = -35.00$, and $C = 25,416$.

Thermal Characteristics¹⁰

Parameter	Test Conditions	Symbol	Typical	Units
Thermal Resistance using Finite Element Analysis	$V_{DS} = 50$ V, $T_C = 120^\circ\text{C}$, $T_{CH} = 225^\circ\text{C}$	R_{θ} (FEA)	8.8	°C/W
Thermal Resistance using Infrared Measurement of Die Surface Temperature	$V_{DS} = 50$ V, $T_C = 120^\circ\text{C}$, $T_{CH} = 225^\circ\text{C}$	R_{θ} (IR)	7.4	°C/W

10. Case temperature measured using thermocouple embedded in heat-sink. Contact local applications support team for more details on this measurement.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Nitride Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 0B and CDM class C2A devices.

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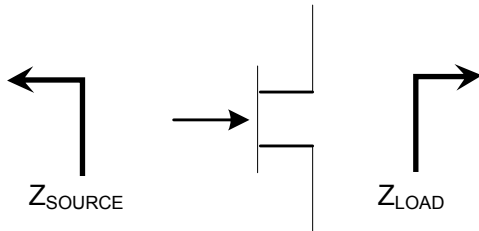
Pulsed¹¹ Load-Pull Performance - for one side only (device is symmetrical)

Reference Plane at Device Leads

Frequency (GHz)	Z_{SOURCE} (Ω)	Single Channel: Maximum Output Power					
		$V_{D1} = 50\text{ V}, I_{DQ1} = 40\text{ mA}, T_C = 25^\circ\text{C}, P_{2.5\text{dB}}$					
		Z_{LOAD}^{12} (Ω)	Gain (dB)	P_{OUT} (dBm)	P_{OUT} (W)	η_D (%)	AM/PM ($^\circ$)
3.4	26.8 - j35.5	15.3 + j16.7	16.6	42.1	16	52	-0.2
3.6	71.7 - j21.2	14.7 + j16.2	16.3	42.2	17	53	0.8
3.8	48.6 + j36.5	14.4 + j16.0	15.9	42.2	17	54	0.7

Frequency (GHz)	Z_{SOURCE} (Ω)	Single Channel: Maximum Drain Efficiency					
		$V_{D1} = 50\text{ V}, I_{DQ1} = 40\text{ mA}, T_C = 25^\circ\text{C}, P_{2.5\text{dB}}$					
		Z_{LOAD}^{13} (Ω)	Gain (dB)	P_{OUT} (dBm)	P_{OUT} (W)	η_D (%)	AM/PM ($^\circ$)
3.4	33.3 - j45.2	8.9 + j20.6	18.4	41.1	13	60	-5
3.6	94.3 - j0.3	7.2 + j21.3	18.3	40.2	10	62	-4
3.8	34.8 + j42.1	8.9 + j19.9	17.4	41.4	14	63	-3

Impedance Reference



Z_{SOURCE} = Measured impedance presented to the input of the device at package reference plane.

Z_{LOAD} = Measured impedance presented to the output of the device at package reference plane.

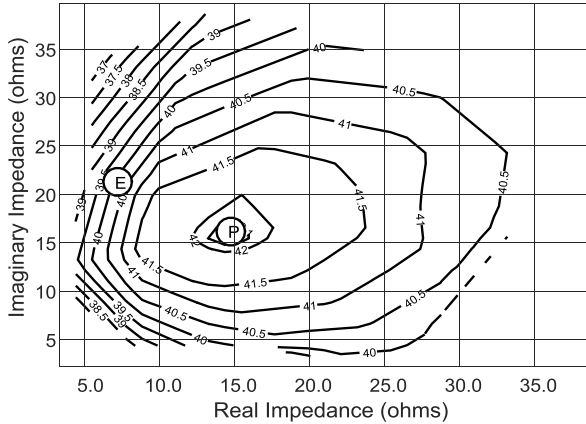
11. Pulse details: 100 μs pulse width, 1 ms period, 10% Duty Cycle.
12. Load Impedance for optimum output power.
13. Load Impedance for optimum efficiency.

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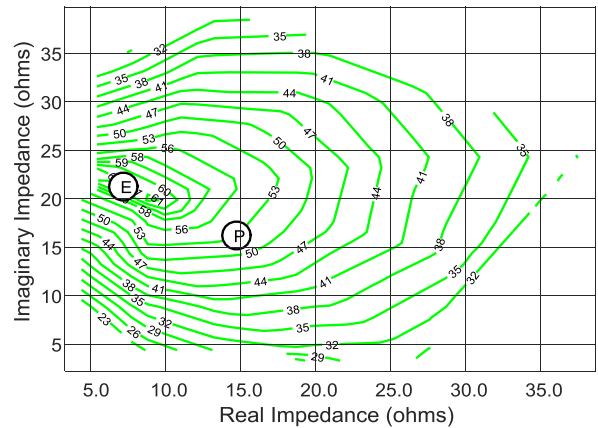
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Pulsed¹¹ Load-Pull Performance - for one side only (device is symmetrical)
3.6 GHz

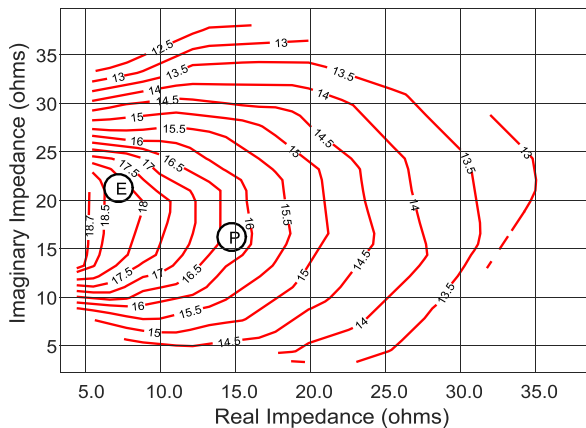
P2.5dB Loadpull Output Power Contours (dBm)



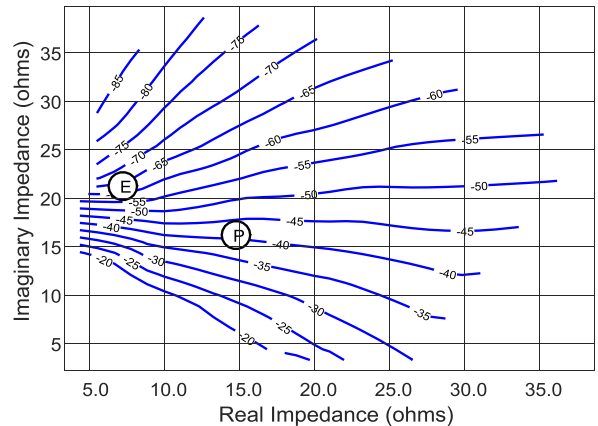
P2.5dB Loadpull Drain Efficiency Contours (%)



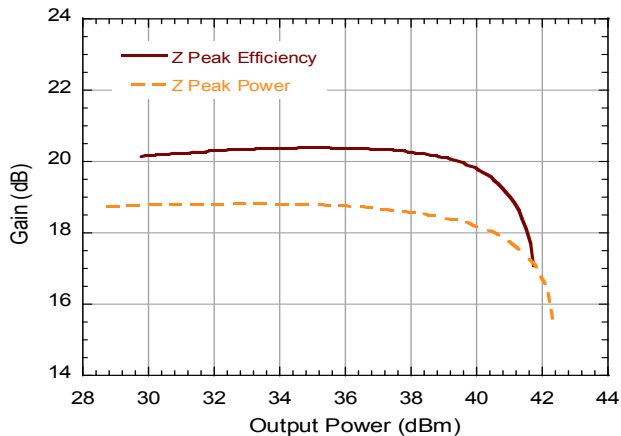
P2.5dB Loadpull Gain Contours (dB)



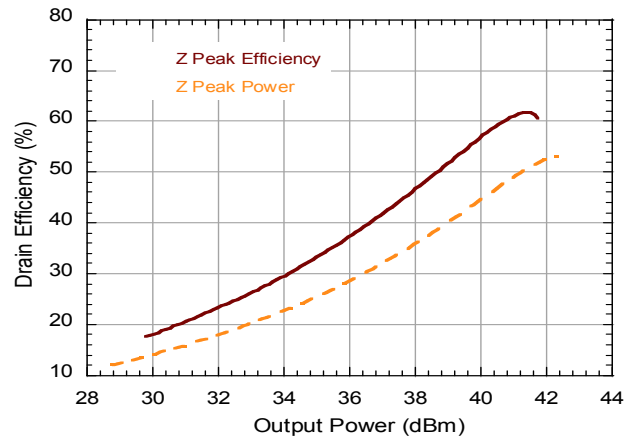
P2.5dB Loadpull AM/PM Contours (°)



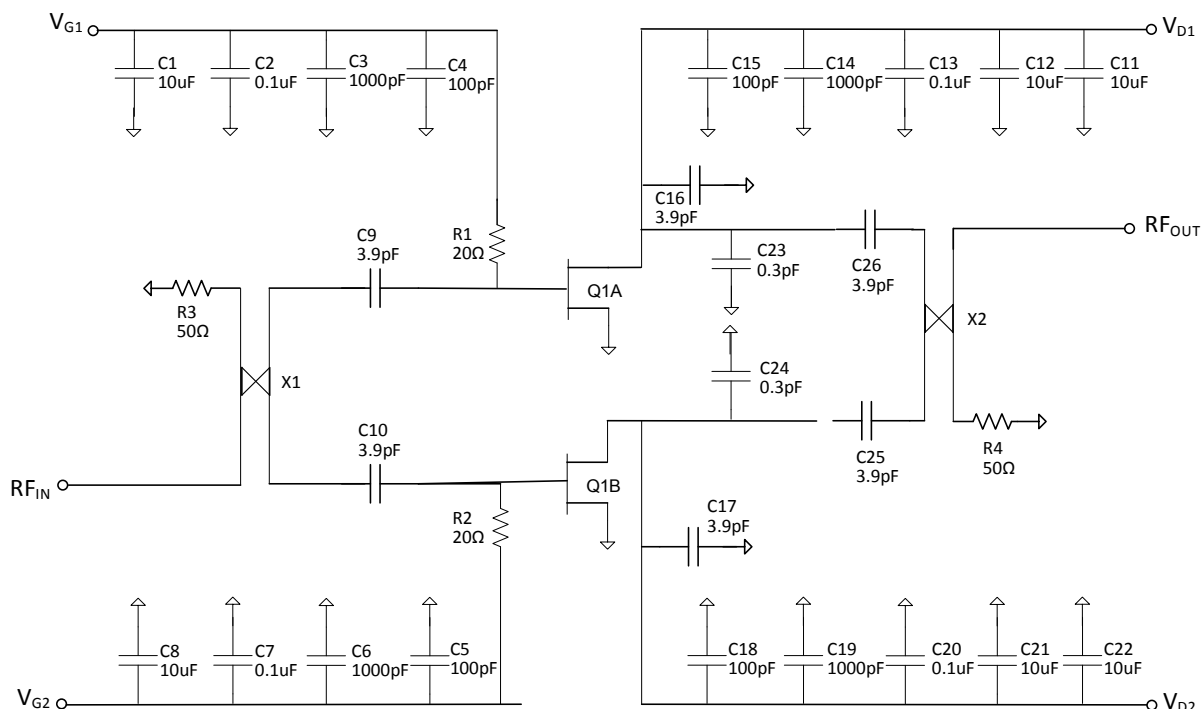
Gain vs. Output Power



Drain Efficiency vs. Output Power



Evaluation Board and Recommended Tuning Solution 3.4 - 3.6 GHz



Description

Parts measured on evaluation board (20-mil thick RO4350). Matching is provided using a combination of lumped elements and transmission lines as shown in the simplified schematic above. Recommended tuning solution component placement, transmission lines, and details are shown on the next page.

Bias Sequencing

Turning the device ON

1. Set V_{G1} and V_{G2} to the pinch-off Voltage (V_P), typically -3 V.
2. Turn on V_{D1} and V_{D2} to nominal Voltage (50 V).
3. Increase V_{G1} until I_{D1} current is reached.
4. Increase V_{G2} until I_{D2} current is reached.
5. Apply RF power to desired level.

Turning the device OFF

1. Turn the RF power off.
2. Decrease both V_{G1} and V_{G2} down to V_P .
3. Decrease V_{D1} and V_{D2} down to 0 V.
4. Turn off V_{G1} and V_{G2} .

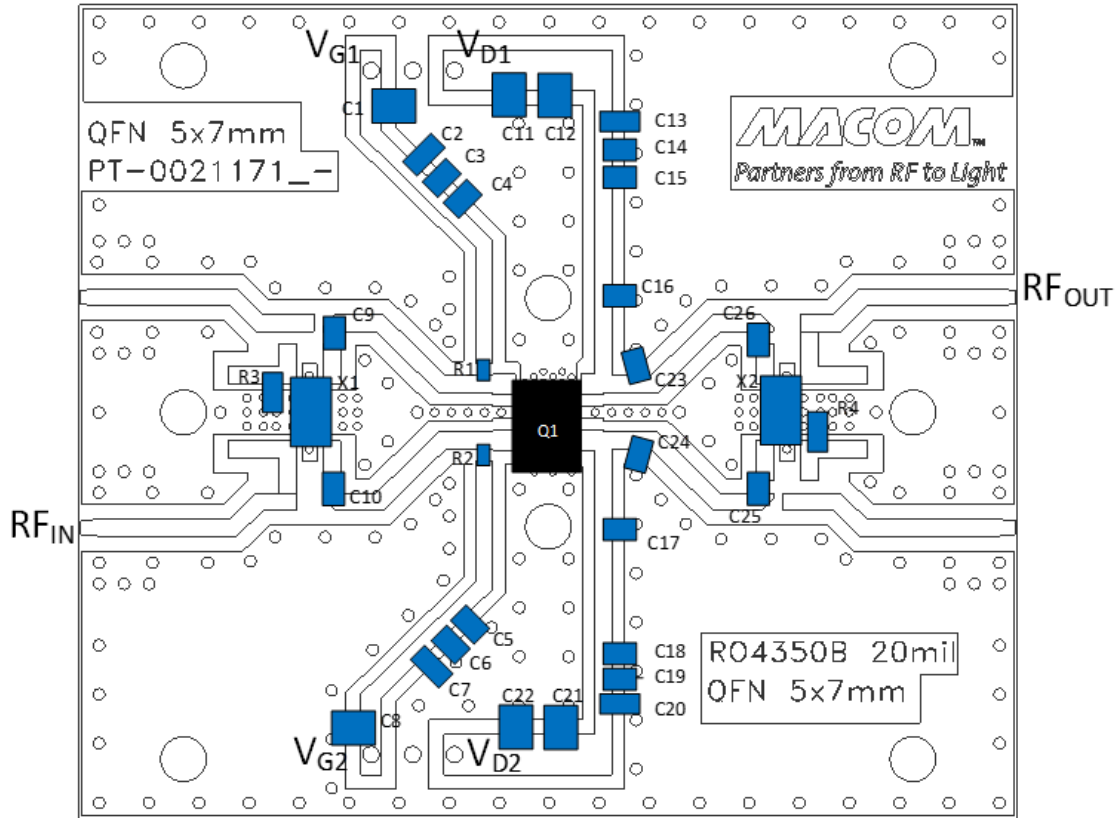
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Evaluation Board and Recommended Tuning Solution 3.4 - 3.6 GHz



Reference Designator	Value	Tolerance	Manufacturer	Part Number
C1, C8, C11, C12, C21, C22	10 μ F	+/- 10%	Murata	GRM21BZ71C106KE15L
C2, C7, C13, C20	0.1 μ F	+/- 10%	DigiKey	C1206C104K1RACTU
C3, C6, C14, C19	1000 pF	+/- 10%	DigiKey	C0805C102K2RACTU
C4, C5, C15, C18	100 pF	+/- 5%	Murata	GQM2195C2E101JB12D
C9, C10, C16, C17, C25, C26	3.9 pF	+/- 0.1 pF	Murata	GQM2195C2E3R9BB12D
C23, C24	0.3 pF	+/- 0.1 pF	Murata	GQM2195C2ER30BB12D
R1, R2	20 Ω	+/- 1%	DigiKey	RT0805DRE0720RL
R3, R4	50 Ω	+/- 1%	RN2 Technologies	S1206N
X1, X2	3dB Coupler		Anaren	X3C35F1-03S
PCB	RO4350, 20 mil, 1 oz. Cu, Au Finish			

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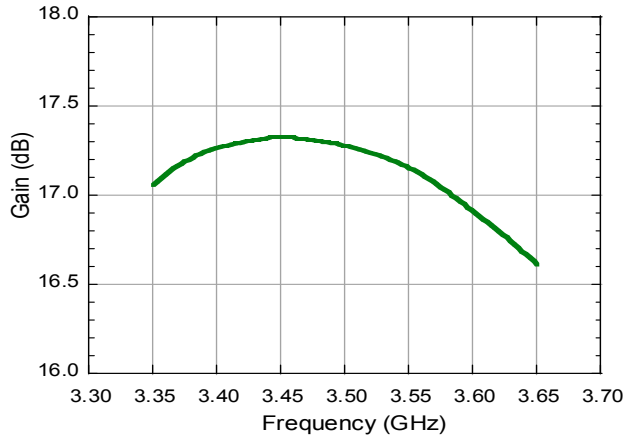
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Typical Performance as Measured in the 3.4 - 3.6 GHz Evaluation Board:

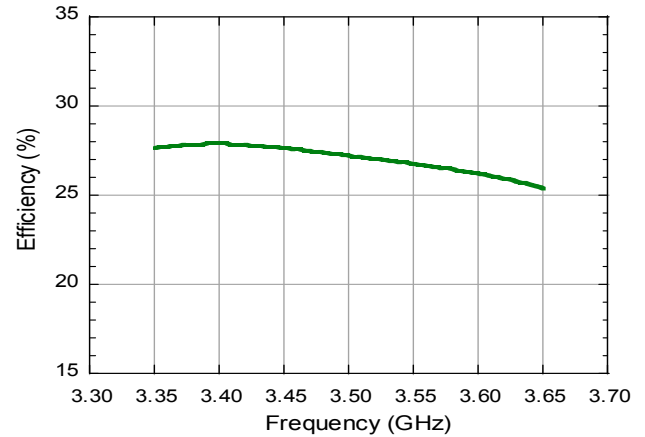
WCMDA 3GPP TM1 64 DPCH 9.9 dB PAR @ 0.01% CCDF

$V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 45\text{ mA}$, $T_C = 25^\circ\text{C}$

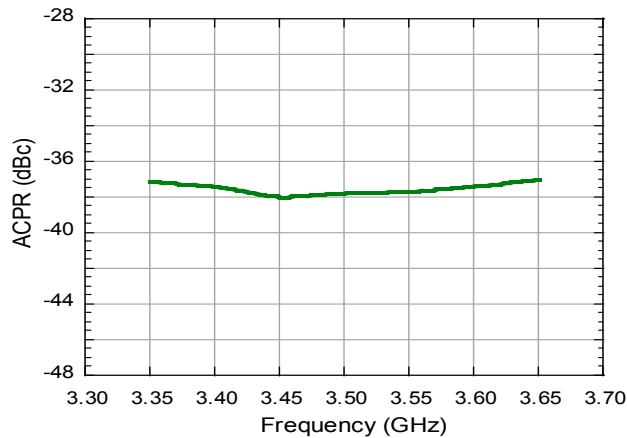
Gain vs. Frequency at $P_{OUT} = 36\text{ dBm}$



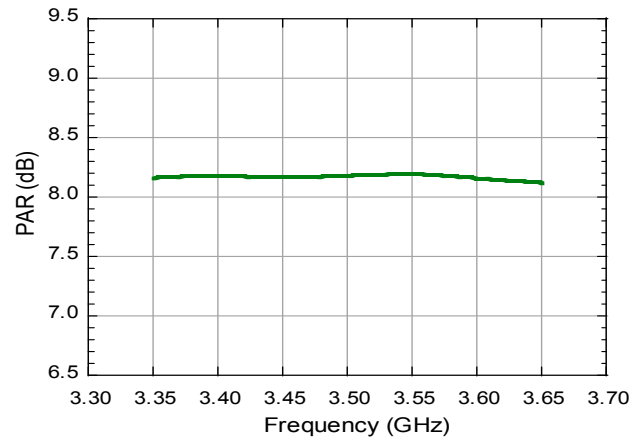
Efficiency vs. Frequency at $P_{OUT} = 36\text{ dBm}$



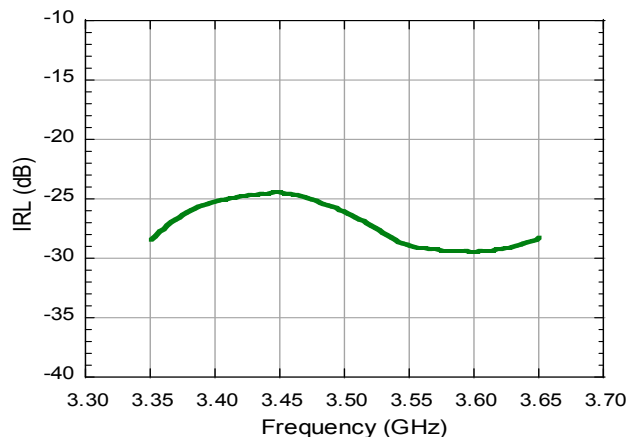
ACPR (Max $\pm 5\text{ MHz}$) vs. Frequency at $P_{OUT} = 36\text{ dBm}$



PAR (CCDF @ 0.01%) vs. Frequency at $P_{OUT} = 36\text{ dBm}$



Input Return Loss vs. Frequency at $P_{OUT} = 36\text{ dBm}$

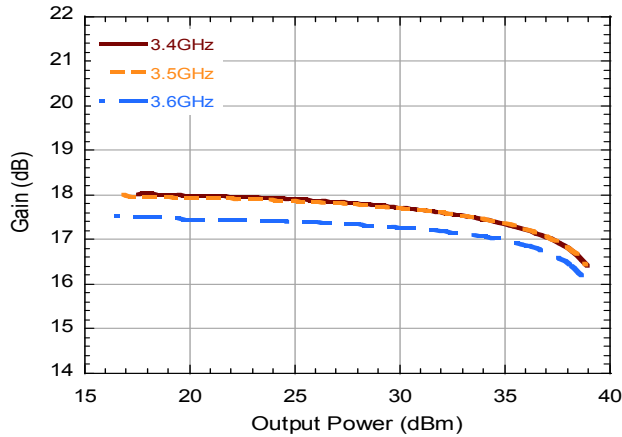


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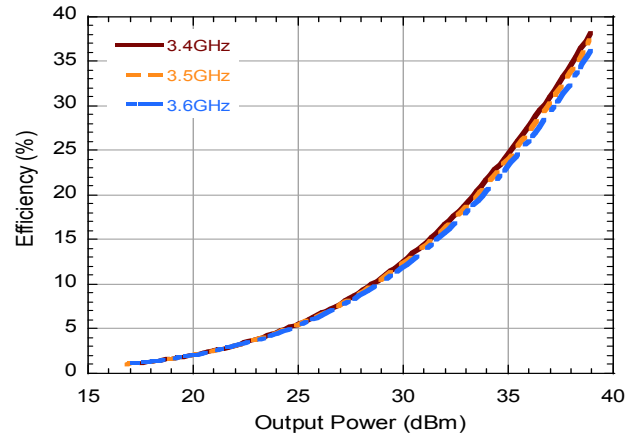
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Typical Performance as Measured in the 3.4 - 3.6 GHz Evaluation Board:
WCMDA 3GPP TM1 64 DPCH 9.9 dB PAR @ 0.01% CCDF
 $V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 45\text{ mA}$, $T_C = 25^\circ\text{C}$

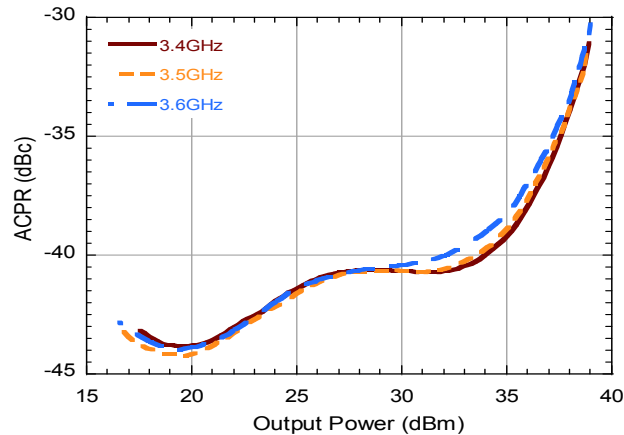
Gain vs. Output Power



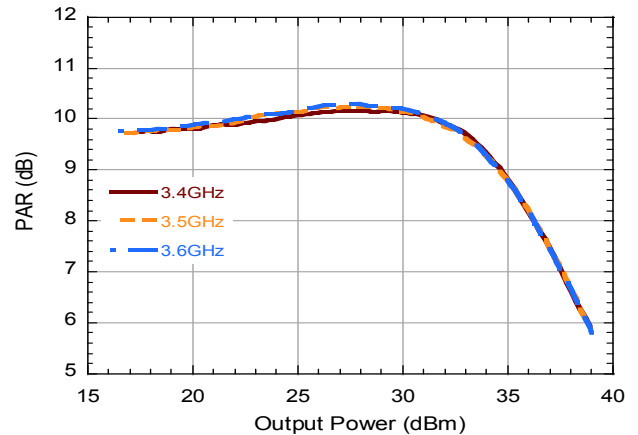
Efficiency vs. Output Power



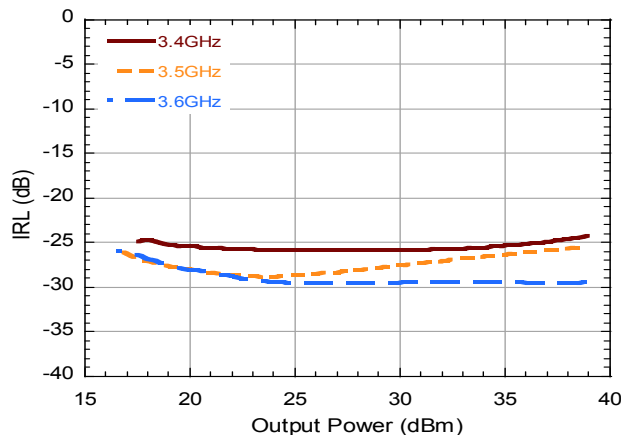
ACPR (Max ±5 MHz) vs. Output Power



PAR (CCDF @ 0.01%) vs. Output Power



Input Return Loss vs. Output Power

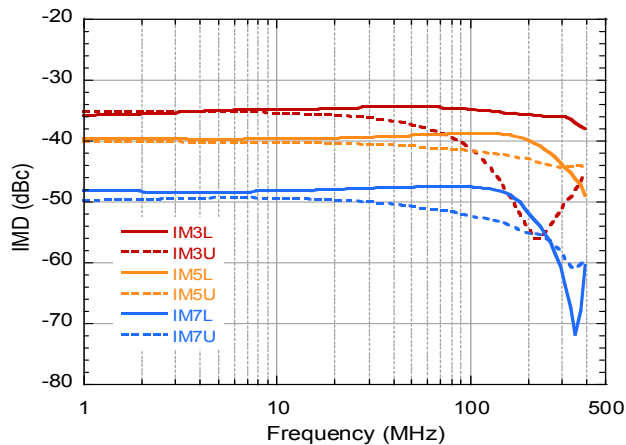


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Typical Performance as Measured in the 3.4 - 3.6 GHz Applications Circuit:
2-Tone Video Bandwidth Performance
 $V_{D1,2} = 50\text{ V}$, $I_{DQ1,2} = 45\text{ mA}$, $P_{OUT} = 36\text{ dBm Avg.}$

IMD vs. Tone Spacing (MHz) at 3.5 GHz



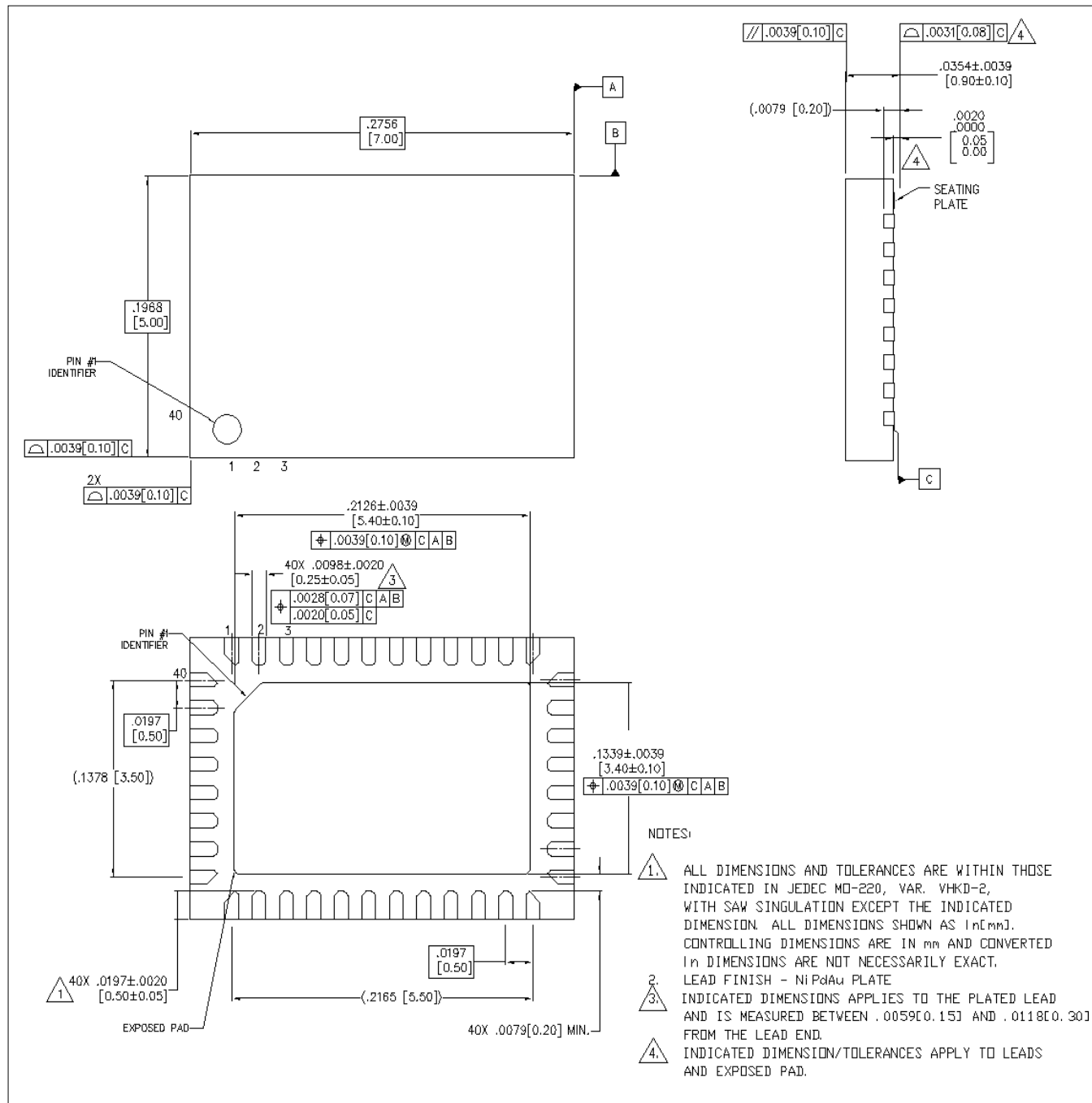
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5 x 7 mm QFN Plastic Package[†]



[†] Meets JEDEC moisture sensitivity level 3 requirements.

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