MADR-010269-DIE

CMOS Serial/Parallel Hex Driver for Digital Attenuators and Phase Shifters

Rev. V1

Features

- 6-bit Serial / Parallel Control Interface
- 3.3 V or 5 V CMOS Input Logic Level
- Complementary 0 V / -5 V Outputs
- Propagation Delay <30 ns Driving 1.5 pF Capacitive Load
- Quiescent Currents <10 µA
- RoHS* Compliant

Description

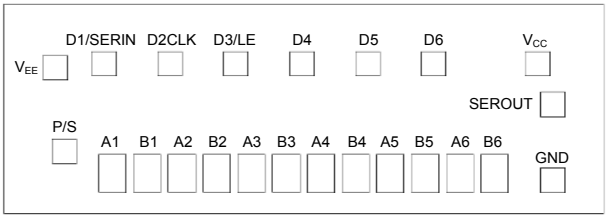
The MADR-010269-DIE is a CMOS driver designed to work with MACOM's digital attenuators and phase shifters. It translates 3.3 V or 5.0 V CMOS inputs to negative gate control voltages.

This driver offers 6-bit serial and parallel control interface. The serial control interface is compatible with the SPI protocol. SEROUT is the SERIN delayed by 6 clock cycles which can be used in daisy-chain operation. Complementary 0 V / -5 V outputs provide up to 1 mA bias current.

Ordering Information

Part Number	Package
MADR-010269-DIE	50 piece Gel Pak

Die Pad Layout



Pin Configuration[1,2]

Pin #	Function	Description of Function
1	P/S	Mode Selection Control
2	A1	Output
3	B1	Output
4	A2	Output
5	B2	Output
6	A3	Output
7	B3	Output
8	A4	Output
9	B4	Output
10	A5	Output
11	B5	Output
12	A6	Output
13	B6	Output
14	GND	Ground
15	SEROUT[3]	SERIN Delayed by 6 Clock Cycles
16	V_{CC}	Positive Bias
17	D6	Parallel Control Input
18	D5	Parallel Control Input
19	D4	Parallel Control Input
20	D3/LE	Shared Control Input
21	D2/CLK	Shared Control Input
22	D1/SERIN	Shared Control Input
23	V_{EE}	Negative Bias

1. Backside of die is connected to VEE, and must be mounted using non-conductive epoxy.
2. Unused control inputs must be tied to VCC or ground.
3. SEROUT shall be left floating when not used.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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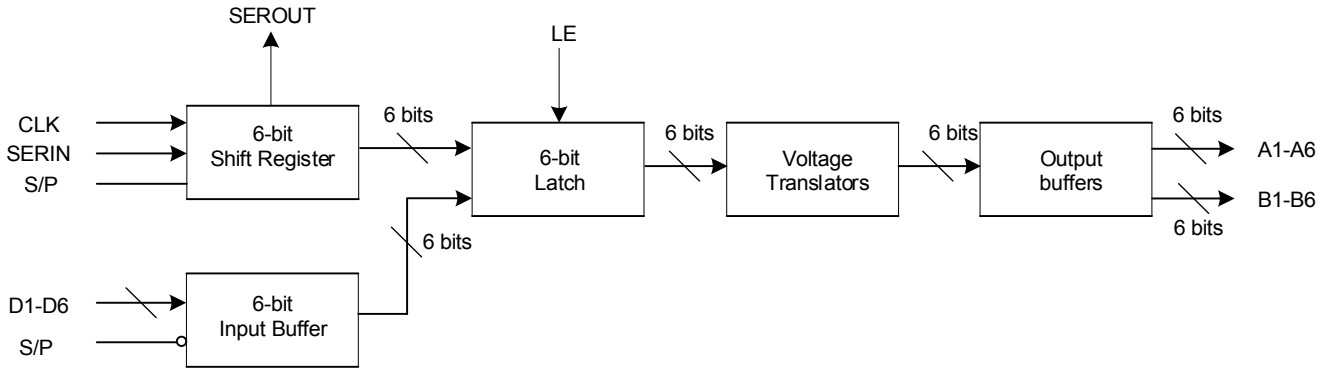
Functional Diagram



6-bit Serial/Parallel Driver

The 6-bit serial/parallel driver consists of shared control inputs D1 - D6, mode selection control P/S, complementary outputs A1 - A6 and B1 - B6, and shifter register output SEROUT.

The serial control interface (SERIN, CLK, LE and SEROUT) is compatible with SPI protocol. It is activated when P/S is set to high. The 6-bit serial word must be loaded with MSB first. When LE is high, 6-bit data in the serial input register will be transferred to 6 pairs of complementary outputs. CLK will be masked to prevent data transition during output loading. SEROUT is the SERIN delayed by 6 clock cycles, and should leave floating if not used.

The parallel mode is enabled when P/S is set to low. In the parallel mode, the outputs are controlled by the parallel control inputs (D1 - D6) directly.

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1C devices.

Serial/Parallel Mode Truth Table

P/S	Mode
1	Serial
0	Parallel

Logic Truth Table

Inputs D1 - D6	Outputs	
	A1 - A6	B1 - B6
0	V_{EE}	GND
1	GND	V_{EE}

Recommended Operating Conditions

Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{CC}	—	V	3.0	—	5.5
V_{EE}	—	V	-5.5	—	-3.0
Junction Temperature	—	°C	-40	+25	+105

DC Electrical Specifications: T_A = 25°C, V_{CC} = +3.3 V, V_{EE} = -5.0 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{CC} Quiescent Current	Control = V_{CC} or GND, No Output Load	µA	—	0.1	0.2
V_{EE} Quiescent Current	Control = V_{CC} or GND, No Output Load	µA	-0.2	0.1	—
Control Input Leakage Current	Control = V_{CC} or GND	µA	—	0.1	—
Input Logic High V_{IH}	—	V	0.7xV_{CC}	V_{CC}	V_{CC}
Input Logic Low V_{IL}	—	V	GND	GND	0.3xV_{CC}
Output High Voltage V_{OH} for An and Bn[4]	I_{OH} = -250 µA	V	-0.1	—	0
Output Low Voltage V_{OL} for An and Bn[4]	I_{OL} = 250 µA	V	V_{EE}	—	V_{EE} + 0.1
Output High Voltage V_{OHS} for SEROUT	I_{OHS} = -100 µA	V	V_{CC} - 0.2	—	V_{CC}
Output Low Voltage V_{OLS} for SEROUT	I_{OLS} = 100 µA	V	0	—	0.2

4. An refers to outputs A1 - A6. Bn refers to outputs B1 - B6.

Typical AC Electrical Specifications: V_{CC} = +3.3 V, V_{EE} = -5.0 V, C_L = 1.5 pF [5,6,7]

Parameter	Description	Units	-40°C	+25°C	+125°C
T_{PLH}	Propagation Delay[6]	ns	20	23	26
T_{PHL}	Propagation Delay[6]	ns	22	24	28
T_{TLH}	Output Rising Transition Time	ns	6	8	8
T_{THL}	Output Falling Transition Time	ns	4	4.5	5.5
T_{SKEW}	Delay Skew, Output A to Output B	ns	1.2	1.2	1.0
t_{CKH}	Min. Serial Clock HIGH Period	ns	50	50	50
t_{CKL}	Min. Serial Clock LOW Time	ns	50	50	50
t_{CS}	Min. Control Set-up Time	ns	20	20	20
t_{CH}	Min. Control Hold Time	ns	20	20	20
t_{LS}	Min. LE Set-up Time	ns	10	10	10
t_{LEW}	Min. LE Pulse Width	ns	10	10	10
T_{LH}	Min. LE Hold Time	ns	10	10	10

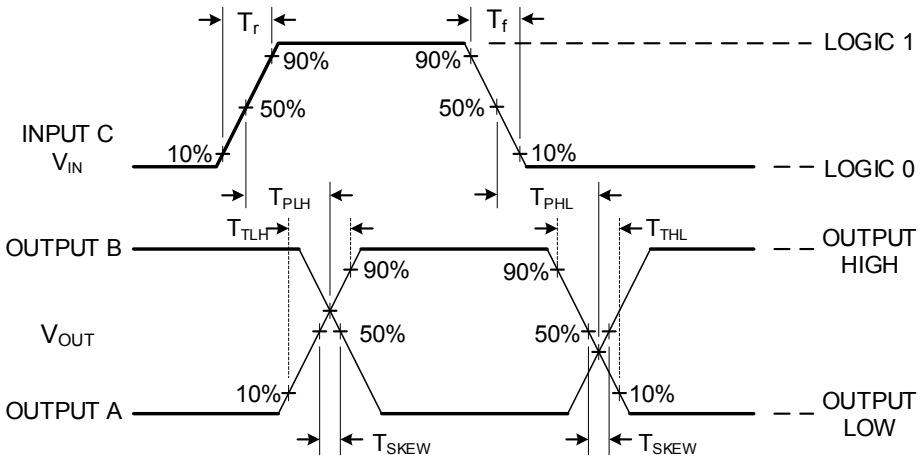
5. The switching speed was measured with 0 V / 3 V inputs with 6 ns rise and fall times.
6. See SWITCHING WAVEFORMS for the definition of the switching terms.
7. In the parallel mode, the INPUT V_{IN} in the SWITCHING WAVEFORMS diagram is the parallel input (D1 - D6). In the serial mode, INPUT VIN in the SWITCHING WAVEFORMS diagram is LE.

Absolute Maximum Ratings[8,9]

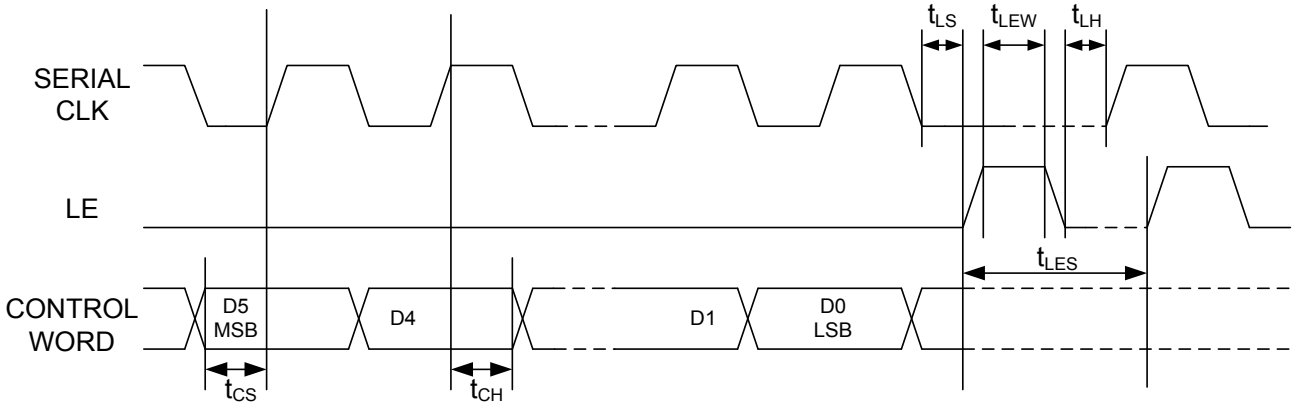
Parameter	Absolute Maximum
V_{CC}	-0.5 V ≤ V_{CC} ≤ +7 V
V_{EE}	-7 V ≤ V_{EE} ≤ +0.5 V
D1 - D6, P/S	-0.5 V ≤ V_{IN} ≤ V_{CC}+0.5 V
DC output Current per Output	10 mA
Junction Temperature	-40°C to +125°C
Storage Temperature	-55°C to +150°C

8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.

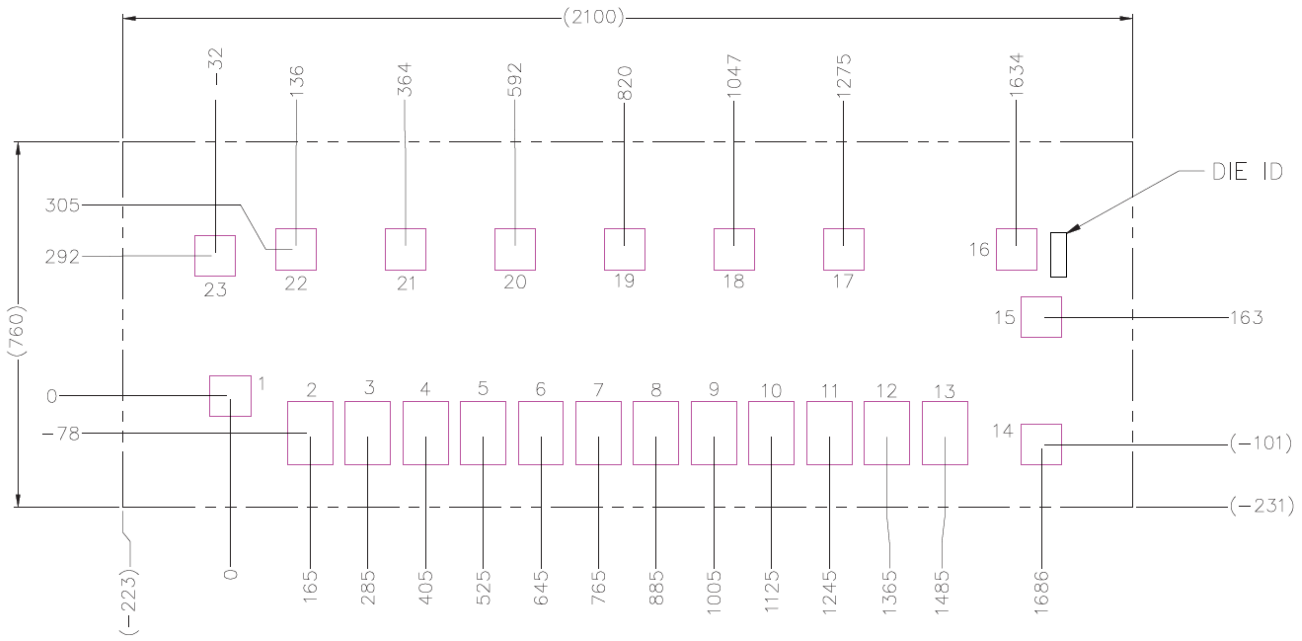
Switching Waveforms: Parallel Mode



Switching Waveforms: Serial Input Interface Timing Diagram



Die Outline[10,11,12,13]



10. All units in µm, unless otherwise noted, with a tolerance of ±5 µm.
11. Die thickness is 203 ±30 µm.
12. Bond pad metallization: Al.
13. Die size reflects uncut dimensions. Saw or laser kerf reduces die size by ~30 um each dimension.

Bond Pad Detail

Pad	X (µm)	Y (µm)
1, 14 - 23	85	85
2 - 13	94	132