MADD-00802
Rev. V1

Features and Functionalities

- Eight(8) Input Parallel Interface (INx)
- Eight (8) Push-Pull Output Drivers
- Driver Output (Vneg) can be set from -54V to 0V
- Driver Output (Vpwr) Rated up to 60V/±80mA
- Internal Level Shifters To Bias Push-Pull Drivers to -54V & 60V.
- Input Logic Range of 2.7V to 5.25V
- 3-Wire Serial Interface (SDI, SCLK, CS*) plus Output Enable (OE)
- Outputs Can Be Paralleled

Applications

- Wireless Base Station/Wireless Infrastructure
- RADAR
- WLAN
- VSAT
- CATV and Broadband

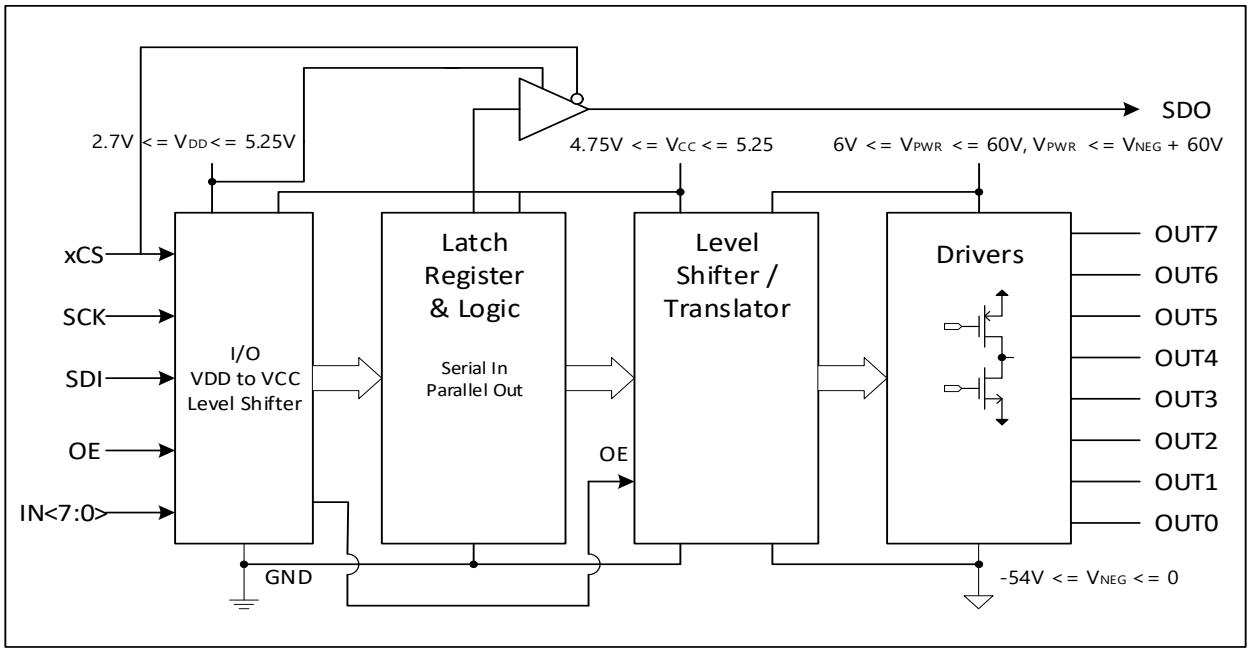
Markets

- Commercial
- Military
- Aerospace
- Industrial

Description

The MADD-00802 is an 8-bit serial to parallel data translator with interfaces to a microprocessor using a standard 3 wire serial interface: serial clock (SCK), serial data input (SDI), and chip select low (xCS). The MADD-00802 can control the 8 switches using an 8-bit parallel input. The output switches can be enabled or tri-stated using pin OE. The MADD-00802 operating range is between 6V ≤ V_{PWR} ≤ 60V and -54V ≤ V_{NEG} ≤ 0V. The maximum power supply difference V_{PWR} – V_{NEG} is 60V. Output total current is up to 400mA. The push pull driver configuration can drive up to 60V. The device also supports a daisy chain configuration mode in which the serial output data (SDO) interfaces to the serial input data (SDI) input of next device. See Functional Description. The MADD-00802 is designed to operate over -40°C to +105°C case temperature range and available in a 32 pin QFN package.

Block Diagram



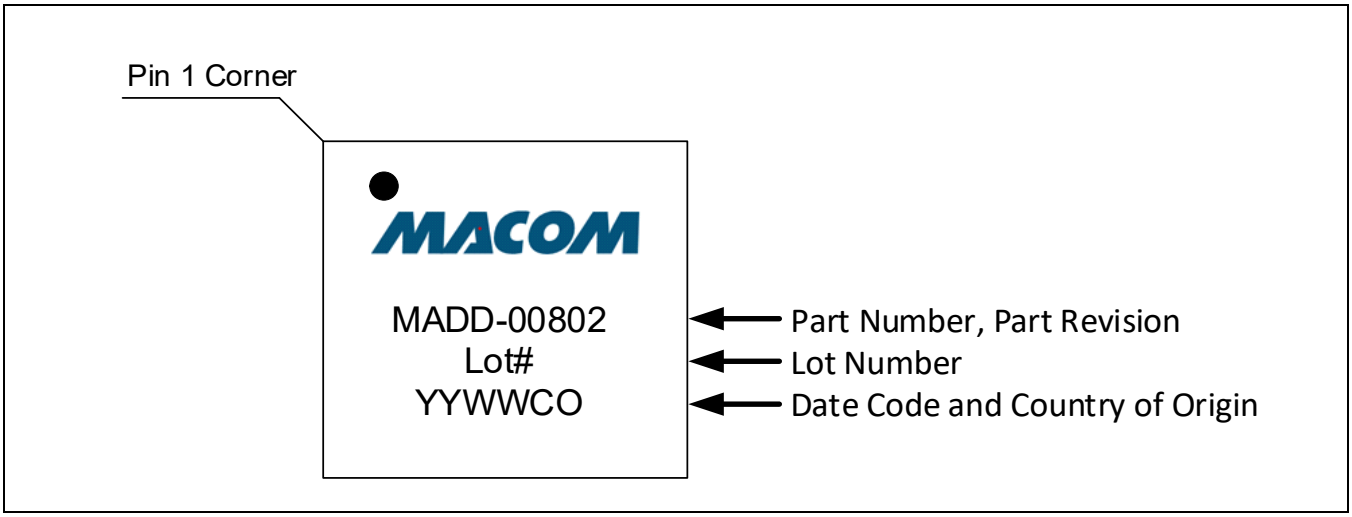
Ordering Information

Part Number	Package	Operating Temperature
MADD-00802	5 x 5 mm QFN32	-40°C to +105°C

Revision History

Revision	Level	Date	Description
V1	Release	Oct 2023	Updated Electrical Characteristics
V2P	Preliminary	Oct 2022	Updated Electrical Characteristics; Added Chapter 3.0 Function Description
V1P	Preliminary	March 2021	Initial release

Figure 1-1. MADD-00802 Marking Diagram



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Min.	Max.	Units
VPWR	VPWR Supply Voltage	1	-0.5	60+Vneg	V
VNEG	VNEG (VPWR reference)	1	-54	0	V
VDD	VDD Supply Voltage (Input Logic Supply for SCK, SDI, OE, xCS, IN<7:0>)	1	-0.5	5.75	V
VCC	VCC Supply Voltage (Level Shifter Supply)	1	-0.5	5.75	V
IOUTx	Continuous Output Current (OUT0-OUT7)	1		±100	mA
TJUNC	Operating Junction Temperature	1	-40	150	°C
TSTORE	Storage Temperature	1	-65	150	°C
VESD,HBM	Electrostatic discharge (HBM)	1,2	-1500	1500	V
VESD,CDM	Electrostatic discharge (CDM)	1,2	-500	500	V

NOTE:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 1(JESD22-A114-B).

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD	VDD Supply Voltage (Input Logic Supply)		2.7		5.25	V
VCC	VCC Supply Voltage (Level Shifter Supply)		4.75	5.0	5.25	V
VNEG	VNEG Voltage		-54	-2.75	0	V
VPWR	VPWR Voltage		+6		VNEG+60	V
TC	Case Temperature	1	-40		105	°C
Theta-JC	Thermal resistance between junction and case	1		26.9(top) 2.2(bot)		°C/Watt

NOTE:

1.) Junction Temperature (TJ) = TC + Theta-JC * (V * I)

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
	Power Consumption Specifications					
IDD	VDD Logic Supply Current (fSCK = 50MHz)			250		uA
IDD	VDD Logic Supply Current (fSCK = 0)				3	uA
IQPWR	Quiescent VPWR Current - VPWR=42, No Load			0.2		mA
Ipwr	Vpwr Current - Total of all Outputs				400	mA
Ineg	Vneg Current - Total of all Outputs				400	mA
ICC	VCC Level Shifter Supply Current			0.3		mA
	DC Electrical Characteristics					
ILeak	Input Leakage Current (SCK, SDI, CS*, OE)				1	uA
Isdo-leak	SDO Tri-State Leakage Current				1	uA
IOUTx	OUT0-OUT7 Current	1			±80	mA
ROUTn	OUT0-OUT7 NMOS Resistance	2		9		Ω
ROUTn	OUT0-OUT7 PMOS Resistance	3		9		Ω
IOUTx	OUT0-7 Tri-State Leakage Current	4			1	uA
NOTE: 1. Any One Output, Sink or Source 2. VNEG = -2.75V, OUT = Low 3. VPWR=42V, OUT = High 4. OE=Logic Low, VPWR=42V, VNEG=0V, VOUT=42V or 0V, TA=25˚C						
	SPI Specifications					
VIH	Input High Voltage (SCK, SDI, CS*, OE)		VDD*0.75			V
VIL	Input Low Voltage (SCK, SDI, CS*, OE)				VDD*0.25	V
tSCK	SCK Period		20			ns
tSCKwh	SCK High Time		8			ns
tSCKwl	SCK Low Time		8			ns
tCSwh	CS* High Time		10			ns
tCSs	CS* Falling to SCK Rising		10			ns
tCSwl	CS* Low Time	2	10			ns
tINs	INx to CS Falling (Setup Time)		5			ns
tINh	INx to CS Rising (Hold Time)		10			ns
tSDIs	SDI to SCK Rising (Setup Time)		4			ns
tSDIh	SDI to SCK Rising (Hold Time)		4			ns
tSDO	SCK Falling to SDO Data Valid	7		4		ns

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
tSDOz	CS* Rising to SDO High Z			4		ns
tdOUTr	CS* Rising to OUTx Rising	1,3		300		ns
tdOUTf	CS* Rising to OUTx Falling	1,3		300		ns
tOUTr	OUTx Rise Time	1,4		100		ns
tOUTf	OUTx Fall Time	1,5		75		ns
tdEOUTr	OE Rising to OUTx Rising	1,4		100		ns
tdEOUTf	OE Rising to OUTx Falling	1,5		100		ns
tdHIZh	OE Falling to OUTx High Z - to 10%, OUTx High	6		50		ns
tdHIZf	OE Falling to OUTx High Z - to 10%, OUTx Low	6		50		ns

NOTE:

1. C(outx)=1000pF and 1K to VMID
2. SCK Low(Parallel Input Mode)
3. OE or CS*50% rising to 10% of OUTx final value
4. From 10% to 90% of final value
5. From 90% to 10% of final value
6. 1KΩ load resistor connected to VMID = (VPWR+VNEG)/2 + VNEG,; no C(OUTx) capacitor
7. Maximum SDO Cload = 100pF

2.0 Package Outline Drawing, Pinout Diagram, and Pin Descriptions

2.1 MADD-00802 Pinout

Figure 2-1. MADD-00802 Pinout

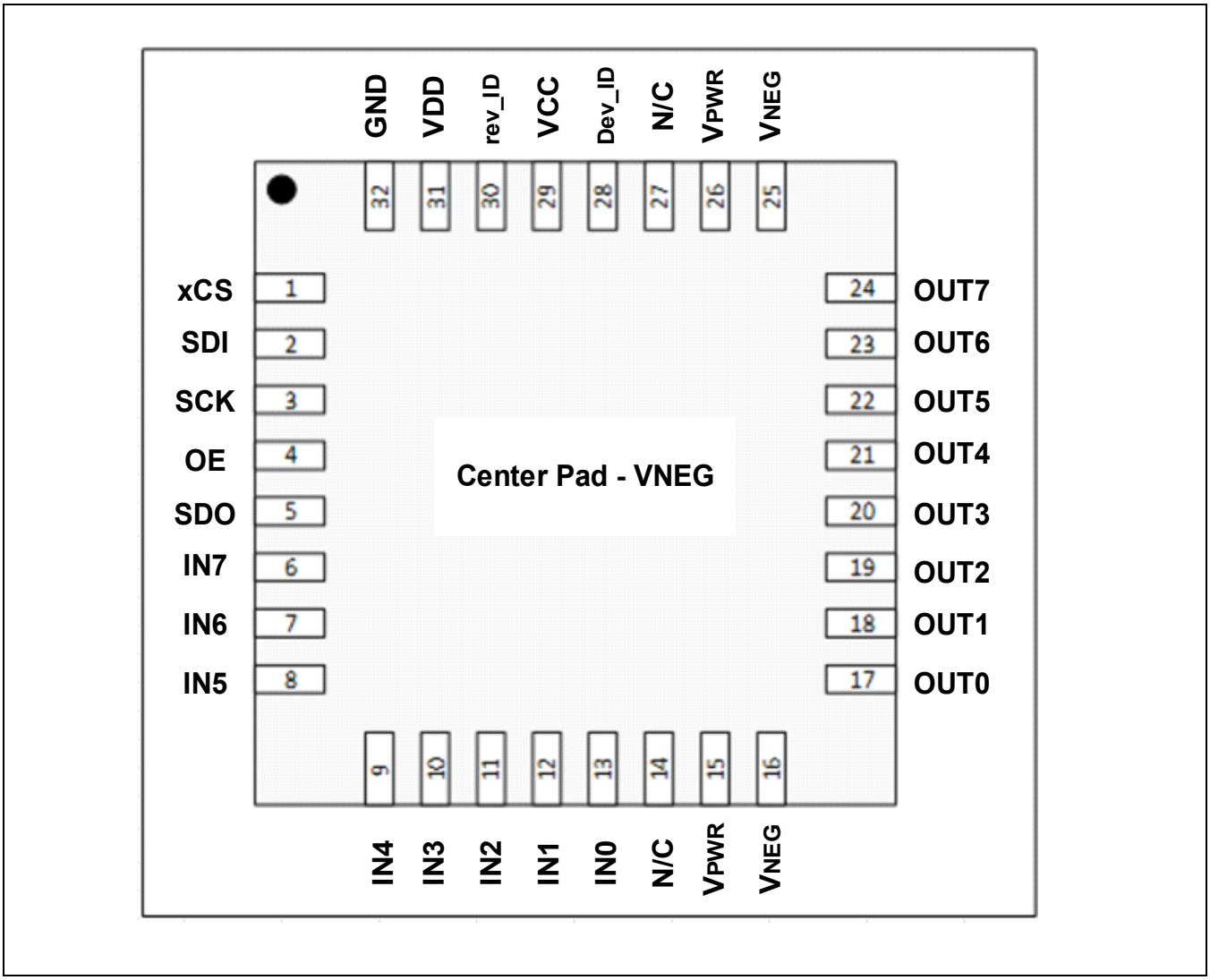
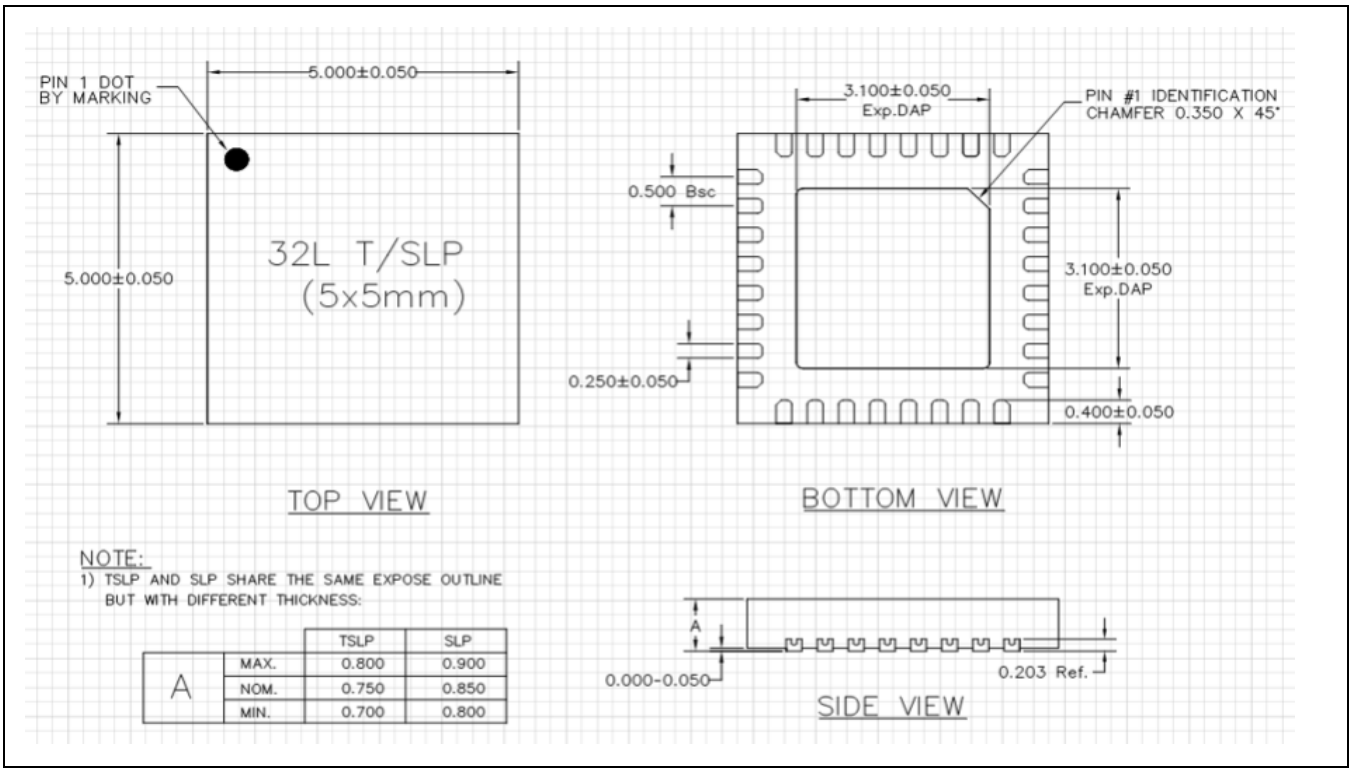


Table 2-1. Pin Configuration

Pin Name	Pin Number	Type	Description
VPWR	15, 26	Power	High Voltage Positive supply: 6V – 60V
VCC	29	Power	Level Shifter Supply (5V)
VDD	31	Power	Input Logic Supply (2.7V to 5.25V)
VNEG	16, 25	Power	Low Voltage Negative supply: -54V – 0V
GND	32	Power	Ground(0V)
IN<7:0>	6, 7, 8, 9, 10, 11, 12, 13	Digital Input	Parallel Input
xCS	1	Digital Input	Chip Select (Active Low)
SDI	2	Digital Input	Serial Data In
SCK	3	Digital Input	Serial Clock
OE	4	Digital Input	Output Enable
SDO	5	Digital Output	Serial Data Out
OUT<7:0>	24, 23, 22, 21, 20, 19, 18, 17	Digital Output	Switch output: -54V – 60V
dev_ID	28	Analog Output	Device ID output (32-pin = 2.5V)
rev_ID	30	Analog Output	Revision ID Output(Rev1 = 0.5V)
NC	14, 27	No connect	
Center Pad	VNEG	Power	Negative supply: -54V – 0V

2.2 Package Outline Drawing

Figure 2-2. MADD-00802 32 Pin Package Dimension



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

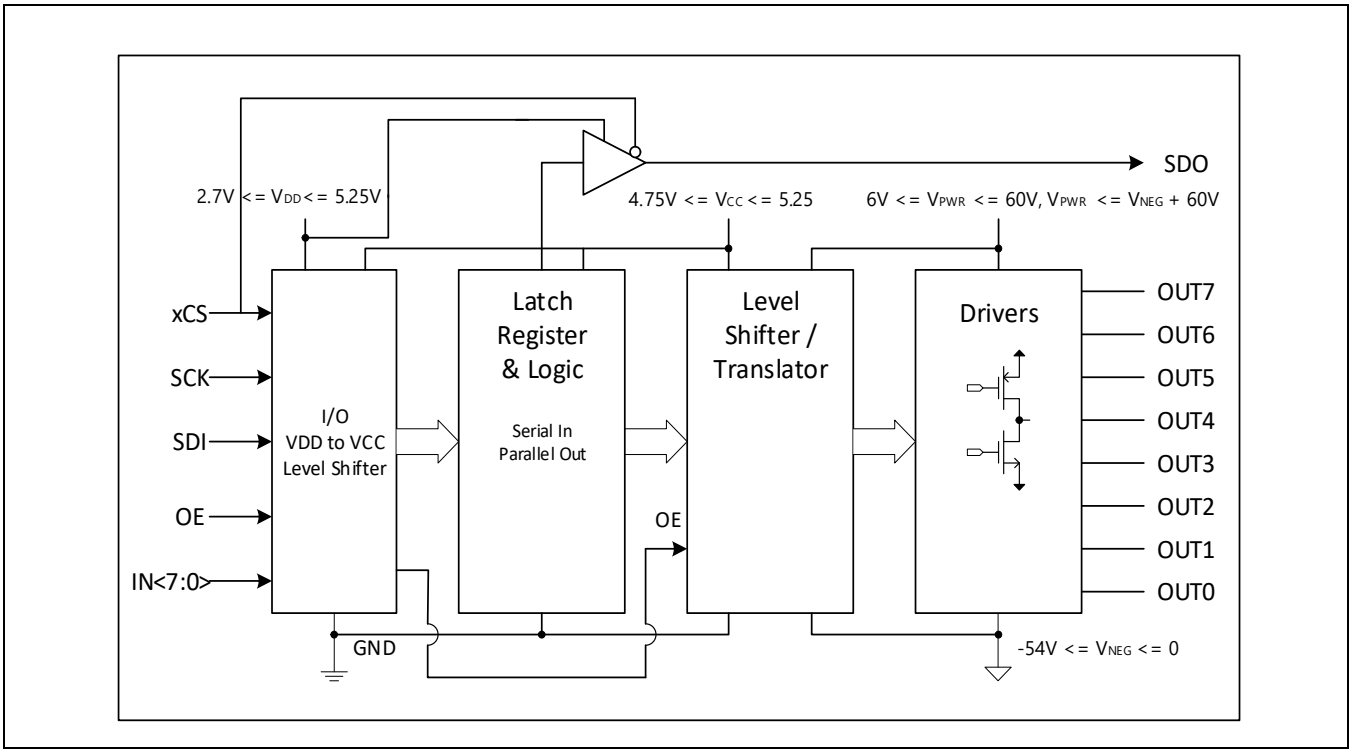
3.0 Functional Description

The MADD-00802 is an 8-bit serial to parallel data translator. The MADD-00802 interfaces to a microprocessor via a standard 3 wire serial interface and a Chip Select (active low).

The serial data with voltage reference to VDD (2.7V to 5.25V) is converted to parallel data and outputted using pins OUT [7:0]. These output pins toggle between V_{PWR} (+6V to 60V) and V_{NEG} (-54V to 0V). The maximum difference between V_{PWR} and V_{NEG} is 60V.

Figure 3-1 Shows a simplified MADD-00802 block diagram. The device functions include VDD to VCC digital input level shifters for xCS, OE, SCK,SDI and IN<7:0>. The xCS pin latches the parallel data IN<7:0> and sends the latched data to the high voltage output switches. There is a VCC to VDD digital output level shifter and tristate buffer for SDO, a serial shift register and 8-bit latch, a bias generator, switch non-overlap circuit, high voltage level shifters VCC to VPWR and VCC to VNEG, and high voltage switches on the output stage. The integrated level shifter eliminate the need to external level shifters, and therefore, decrease the PCB complexity, device count, and increase clock and data rate.

Figure 3-1. MADD-00802 Detailed Block Diagram



3.1 Operation Modes

3.1.1 Serial Input to Parallel Output Mode

The MADD-00802 interfaces to a microprocessor through a serial to parallel data interface: serial data input (SDI), serial clock (SCK), and an active-low chip select (xCS). Refer to Figure 3-2.

When xCS is low (call out 1), serial input data can be transferred to the shift register through the SDI pin. The serial input data is shifted into the register on the positive edge of SCK (call out 2). Eight SCK cycles are required to transfer the SDI data to the 8-bit shift register. If CS* remains low, the serial data from the previous 8-bits shift out of the register through the SDO pin on the negative edge of SCK (call out 3). On the positive edge of xCS (call out 4), serial input data is latched and sent to the high voltage drivers, OUT0 through OUT7. Also, SDI and SCK are ignored and SDO is tristated. When the output enable pin OE is HIGH (call out 5) , the high voltage switch outputs OUT0 through OUT7 are enabled. If OE is low, the switches are tristated.

Figure 3-2. Serial Mode Timing Diagram 1

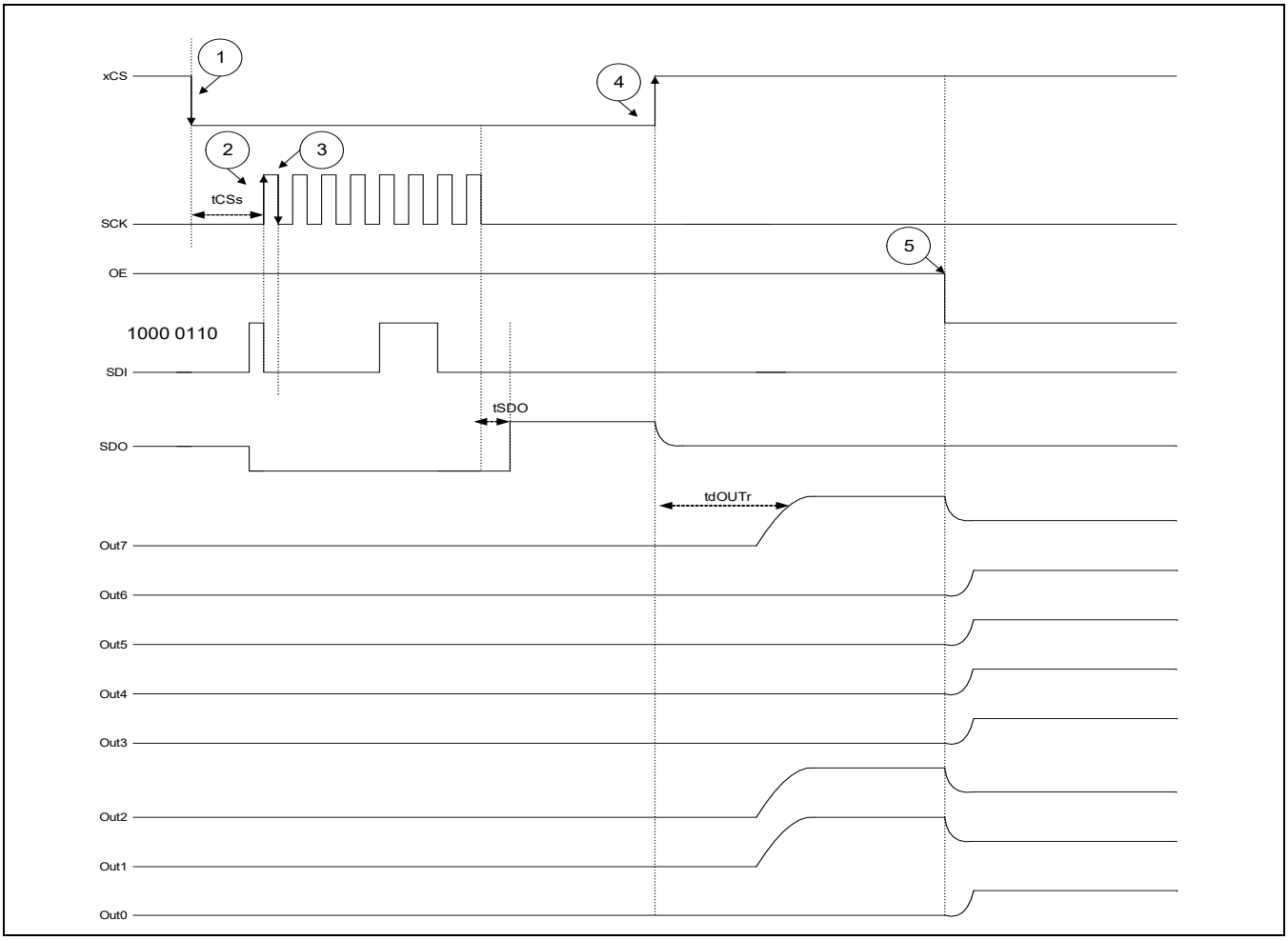
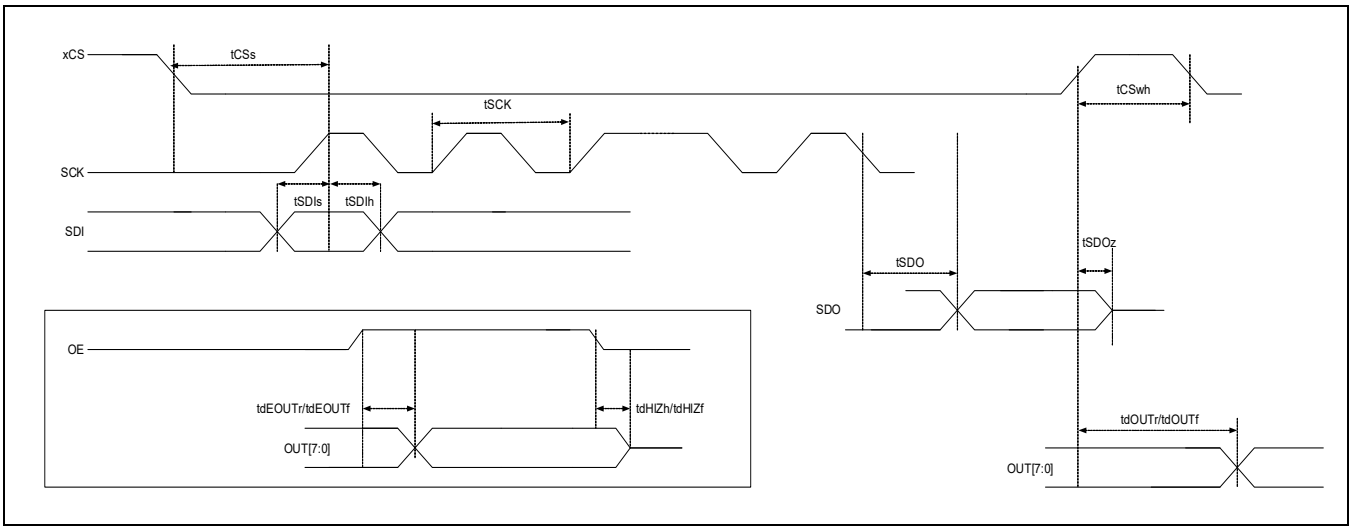


Figure 3-3. Serial Mode Timing Diagram 2



3.1.2 Serial Daisy Chain Mode

The MADD-00802 devices may be serially cascaded by connecting SDO to SDI of the next device. See Figure 3-4. Pins SCK and xCS are common to all cascaded devices. For n-cascaded devices, there should be multiple 8 SCK cycles (8N) and the xCS pin should remain LOW.

When the xCS pin goes LOW, the initial 8-bits of the shift register will be 00000000b. See Figure 3-5. The first 8 SCK cycles will shift the SDI data into the register on the SCK RISING edge (call out 1). On the SCK FALLING edge (call out 2), the initial 8-bits, 00000000b, are shifted out of SDO.

If SCK exceeds 8 cycles and xCS remains LOW, the SDI data that propagated through the shift register will be appear at the SDO pin (call out 3). After N 8-bit SCK cycles and on the rising edge of xCS, the switch outputs will correspond to the last 8-bits clocked into the shift register (call out 4) and the SDO output will be tri-stated.

Figure 3-4. Daisy Chain Configuration

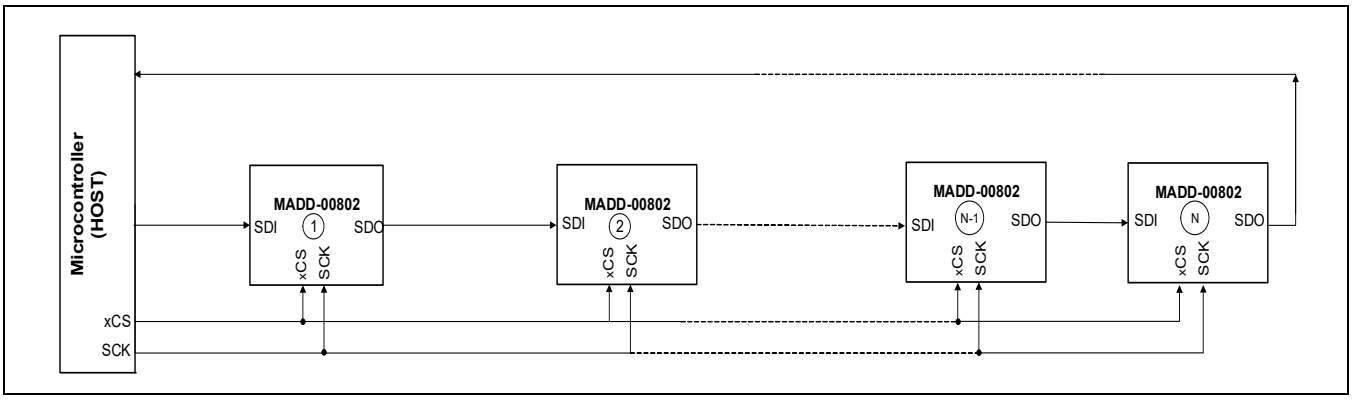


Figure 3-5. Daisy Chain Timing Diagram 1

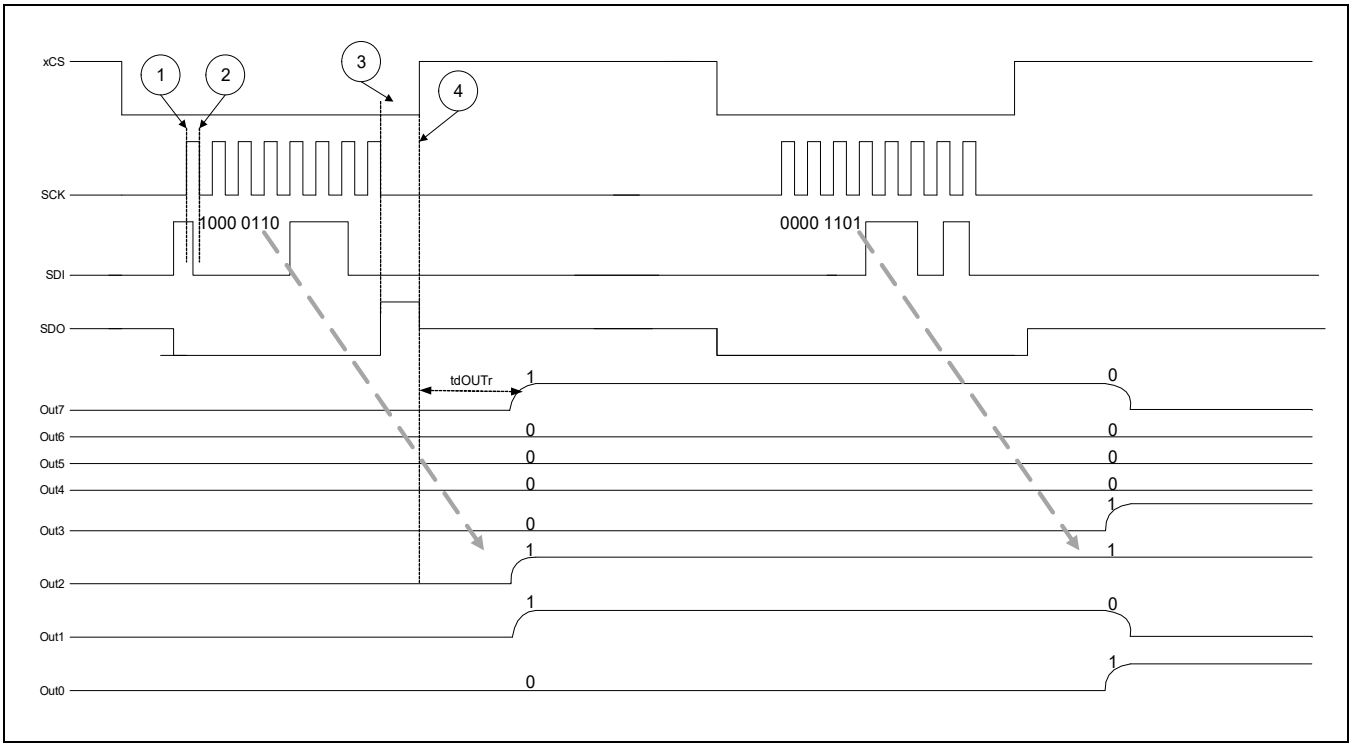
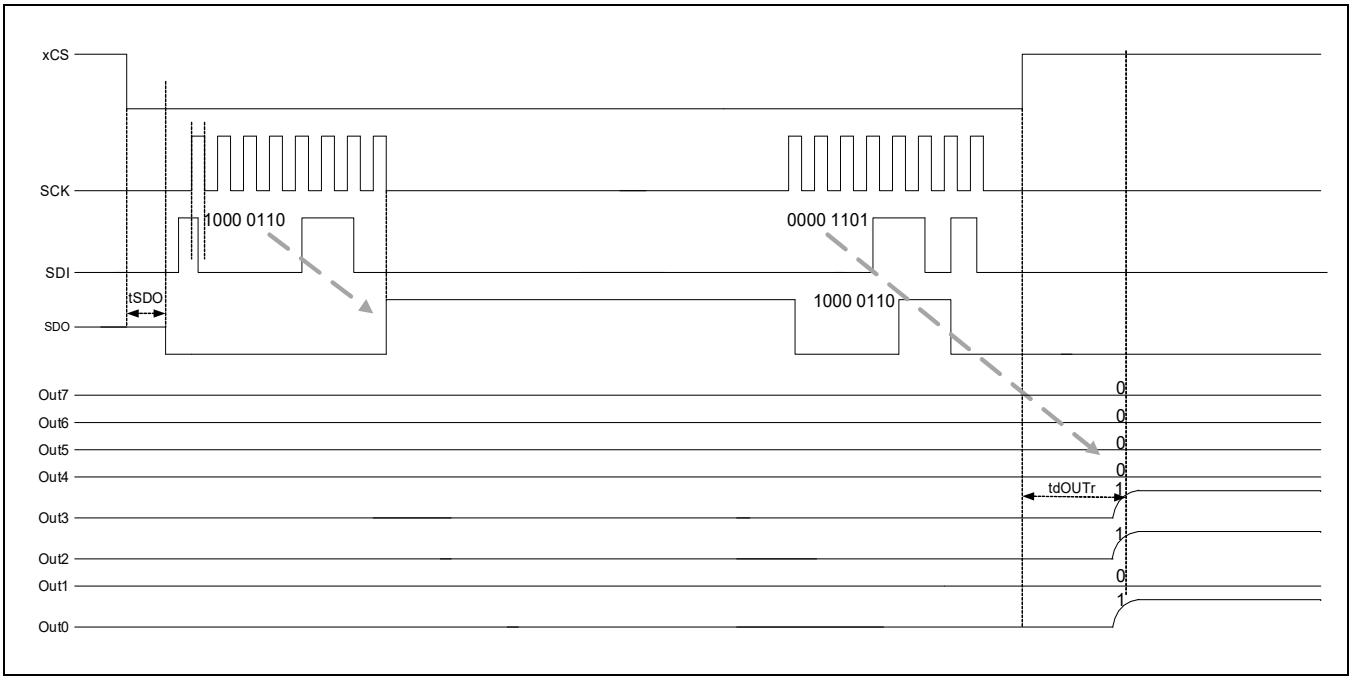


Figure 3-6. Daisy Chain Timing Diagram 2



3.1.3 Parallel Input to Parallel Output Mode

The MADD_00802 supports parallel input mode where the logic at the low voltage inputs IN<7:0> are latched to the high voltage outputs Out<7:0>.

pin. **SDI** and pin.**SCK** should both be LOW as they have no effect on this mode, only pin.**xCS**. When the xCS pin goes LOW, the parallel bits are latched into an internal MADD-00802 register after tINxh time. When the xCS goes HIGH, the outputs OUT<7:0> correspond the IN<7:0> inputs after tdOUTr time.

Figure 3-7. Parallel Input Diagram