Features

- E-Band Downconverter
- Direct Down-Conversion with I/Q BW up to 4 GHz
- WR12 Interface for the RF Input
- LO×8 with Buffer
- 12 dB Conversion Gain
- 5 dB Noise Figure
- 2 dBm Input IP3
- RoHS* Compliant Surface Mount Package
- Size: 8.0 × 8.0 × 2.235 mm

Applications

- Point-to-Point

Description

The MADC-011021 is a surface mount E-band receiver. The module operates from 71 - 86 GHz and is designed to be used in direct conversion or heterodyne applications. The RF input is a WR12 interface.

The module provides 12 dB of conversion gain and a noise figure of 5 dB. The linear mixer topology allows for strong IIP3 performance (2 dBm) to be maintained up to the radio input levels recommended in the standards. The baseband is a quadrature balanced four line interface (I, I*, Q, Q*).

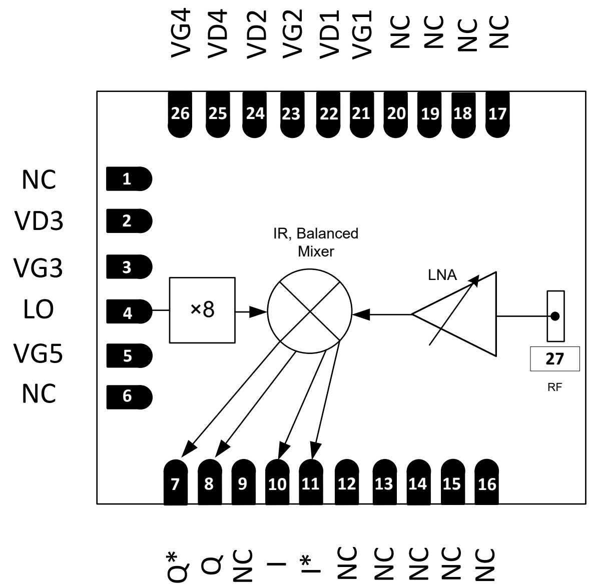
Other features include a local oscillator ×8 multiplier and buffer.

Each device is 100% RF tested to ensure performance compliance.

Ordering Information

Part Number	Package
MADC-011021	Parts shipped in tray
MADC-011021-TR0200	200 part reel
MADC-011021-TR0500	500 part reel
MADC-011021-001SMB	Evaluation Board

Functional Schematic



Pin Configuration[1,2]

Pin #	Pin Name	Function
1,6,9,12-20	N/C	No Connection
2	VD3	Drain Voltage 3
3	VG3	Gate Voltage 3
4	LO	LO Port
5	VG5	Gate Voltage 5
7	Q*	Q*, IF Port
8	Q	Q, IF Port
10	I	I, IF Port
11	I*	I*, IF Port
21	VG1	Gate Voltage 1
22	VD1	Drain Voltage 1
23	VG2	Gate Voltage 2
24	VD2	Drain Voltage 2
25	VD4	Drain Voltage 4
26	VG4	Gate Voltage 4
27	RF	RF Port

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
VD = 3 V, ID1,2,3,4 = 50, 160, 125, 100 mA, VG5 = -2.25 V, PLO = -5 dBm, Backside Temperature (T_B) = +25°C

Parameter	Test Conditions[2]	Units	Min.	Typ.	Max.
RF Frequency	—	GHz	71	—	86
IF Bandwidth	—	GHz	DC	—	4
LO Frequency	—	GHz	8.625	—	11
LO Multiplication Factor	—			8	
LO Input Power	—	dBm	—	-5	—
Conversion Gain	IF = 700 MHz	dB	9	12	—
Image Rejection	IF = 21.4 MHz	dBc	—	-20	—
Noise Figure	IF = 700 MHz	dB	—	5	8
LO×7, LO×9 at RF Port Leakage	No IF Applied	dBm	—	-50	—
LO×8 at RF Port Leakage	No IF Applied	dBm	—	-40	—
Input IP3	IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone	dBm	—	2	—
C/I2 Two Tones	IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone	dBc	—	55	—
C/I2 (IF/2)	IF = 21.4 MHz, Pin = -30 dBm	dBc	—	55	—
Input P1dB	IF = 21.4 MHz	dBm	—	-5	—
Return Loss	RF LO IF	dB	—	8 15 8	—

2. Graphs in datasheet use test conditions as shown above unless otherwise specified.

Biasing over Temperature

It is recommended to have a current controlled biasing method.
Temperature data presented here is at the following bias levels unless otherwise specified.
For graphs labelled ID12, stages 1 and 2 are combined to create ID1 + ID2; similarly for ID34.

Pad Label	Current @ -40°C (mA)	Gate Voltage @ -40°C (V)	Current @ +25°C (mA)	Gate Voltage @ +25°C (V)	Current @ +85°C (mA)	Gate Voltage @ +85°C (V)
VD1	37.5	-0.55	50	-0.45	62.5	-0.35
VD2	112.5	-0.55	150	-0.45	187.5	-0.35
VD3	120	-0.38	120	-0.35	120	-0.32
VD4	100	-0.38	100	-0.35	100	-0.32
VG5	-3	-2.25	-3	-2.25	-3	-2.25

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Drain Voltage	4.3 V
Gate Bias Voltage (VG1,2,3,4)	-1.5 V < VG < 0.3 V
Gate Bias Voltage (VG5)	-5 V < VG < 0.3 V
RF Input Power	0 dBm
LO Input Power	+10 dBm
Junction Temperature[5,6]	+150°C
Storage Temperature	-55 to 150°C
Operating Temperature	-40 to 85°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \le 150°C$ will ensure MTTF > 1×10^6 hours.
6. Junction Temperature (T_J) = $T_B + \Theta_{jc} \times (V \times I)$, where T_B is backside temperature of package and Θ_{jc} is thermal resistance of the device.
   See table below for Junction Temperature for each stage of the module. Each stage must remain below 150°C.

Handling Procedures

Please observe the following precautions to avoid damage:

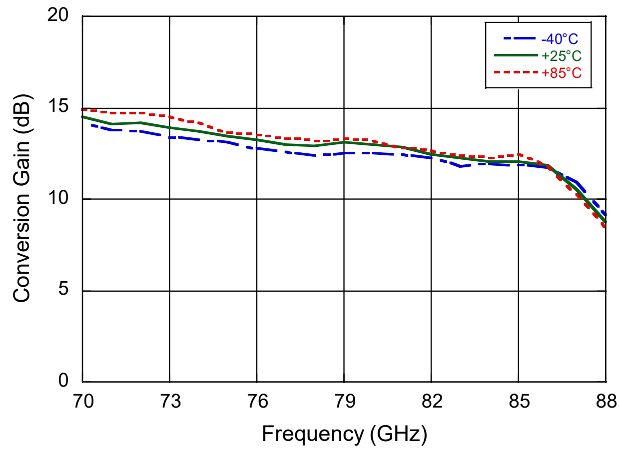
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B static sensitive devices.

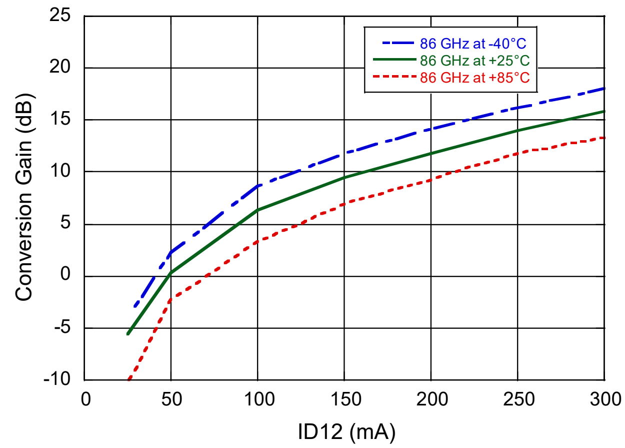
Pin Label	Thermal Resistance (°C/W)	Current @ +85°C (mA)	T_J for T_B = +85°C (°C)	Maximum Drain Current Rating (mA)
VD1	139	63	111	130
VD2	54	187	115	220
VD3	75	120	112	300
VD4	115	100	120	190

Typical Performance Curves over Temperature

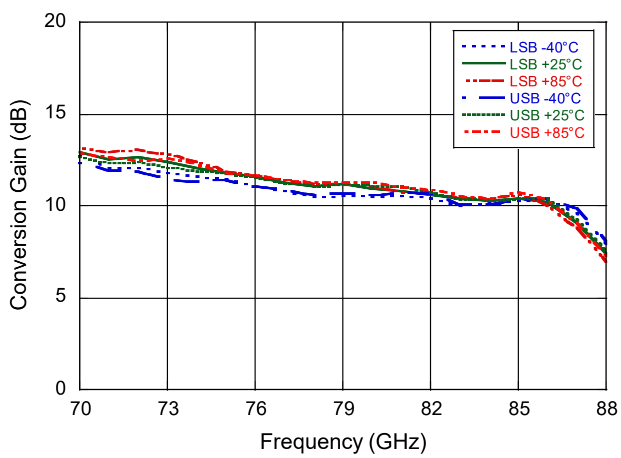
Conversion Gain at Nominal Bias at IF = 21.4 MHz



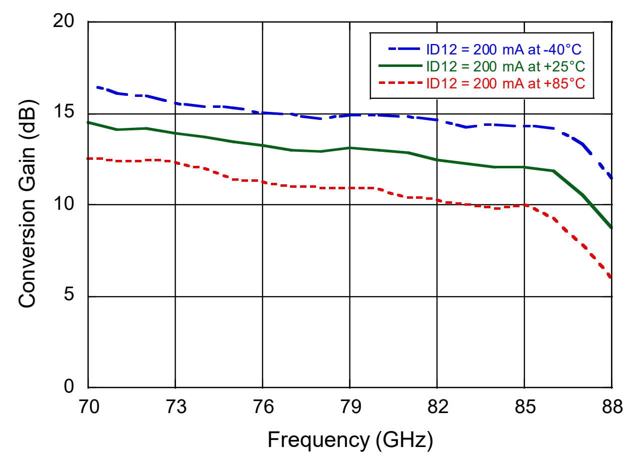
Conversion Gain vs. LNA Bias at IF = 21.4 MHz



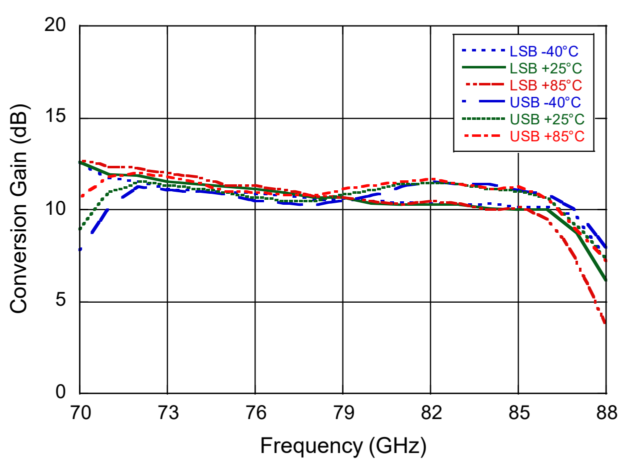
Conversion Gain at Nominal Bias at IF = 700 MHz



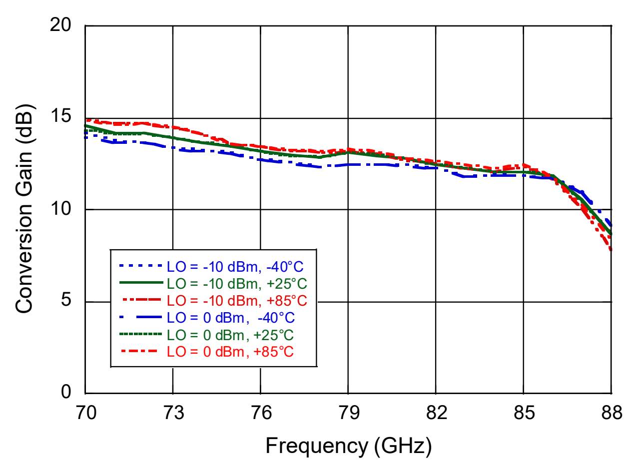
Conversion Gain at Fixed Current at IF = 21.4 MHz



Conversion Gain at Nominal Bias at IF = 4 GHz

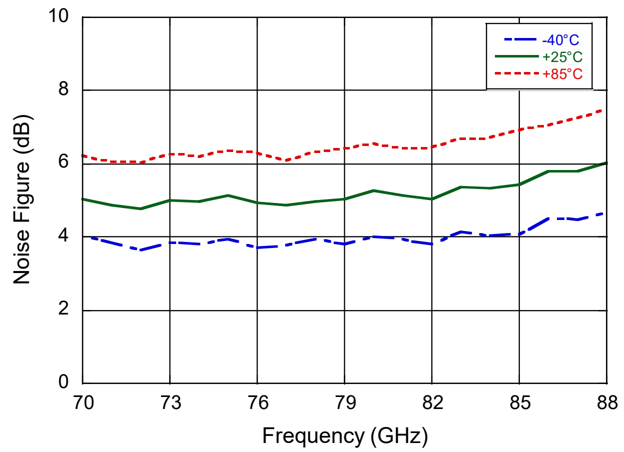


Conversion Gain vs. LO Power at IF = 21.4 MHz

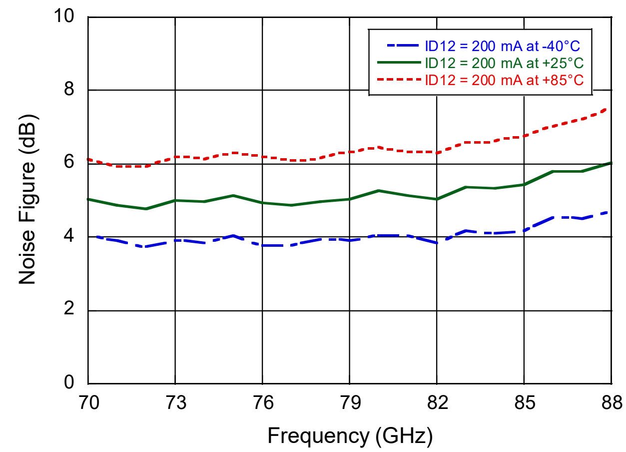


Typical Performance Curves over Temperature

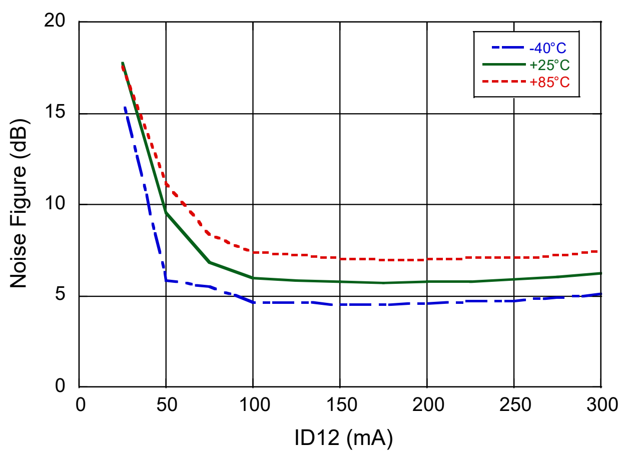
Noise Figure at Nominal Bias at IF = 700 MHz



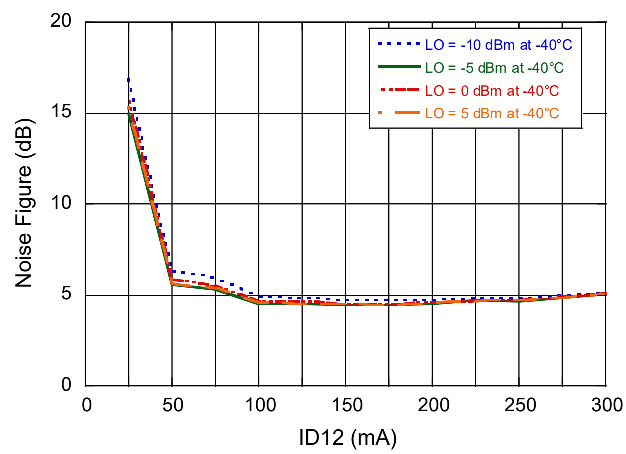
Noise Figure at Fixed Bias at IF = 700 MHz



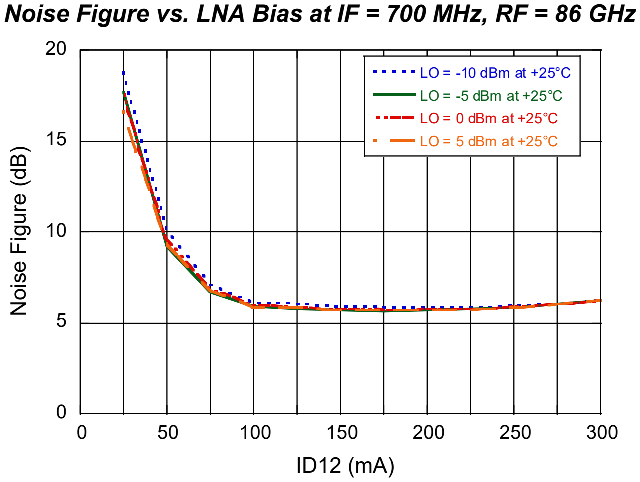
Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz



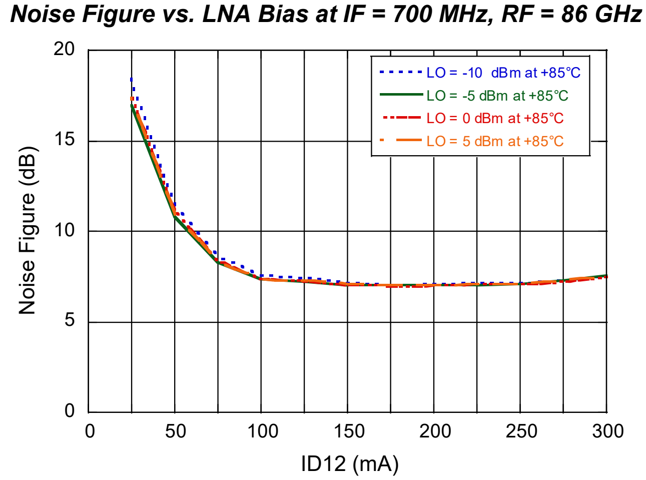
Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz



Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz

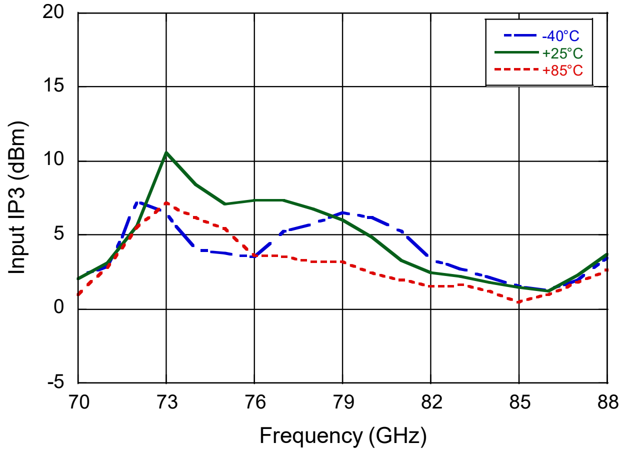


Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz

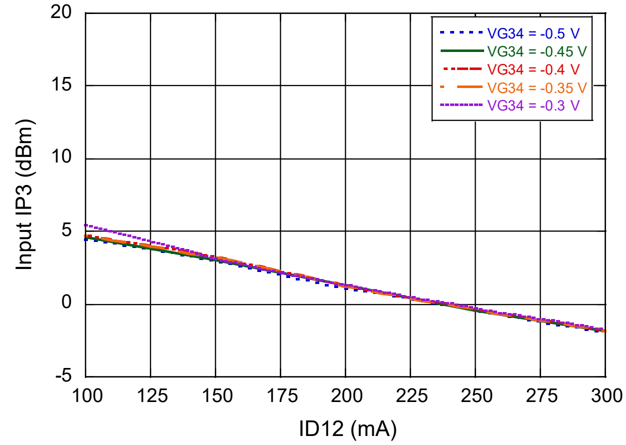


Typical Performance Curves over Temperature

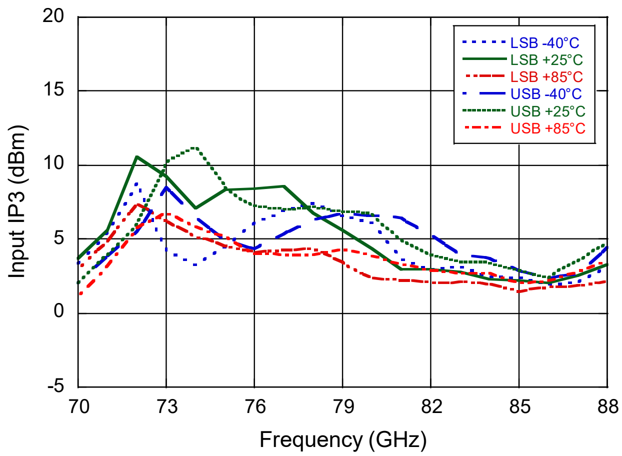
Input Referred IP3 at Nominal Bias at IF = 21.4 MHz



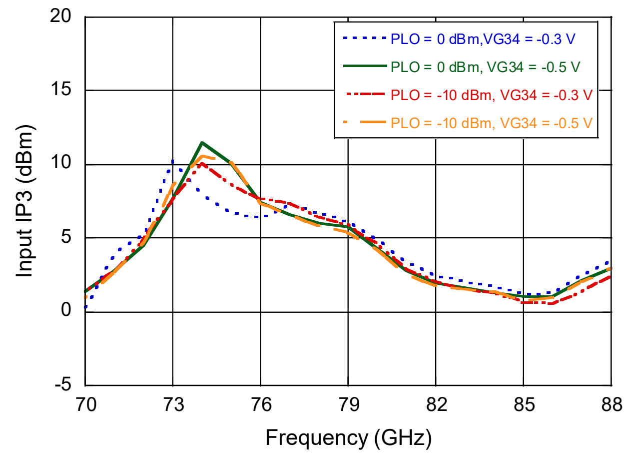
Input Referred IP3 vs. LNA Bias at IF = 21.4 MHz, RF = 86 GHz



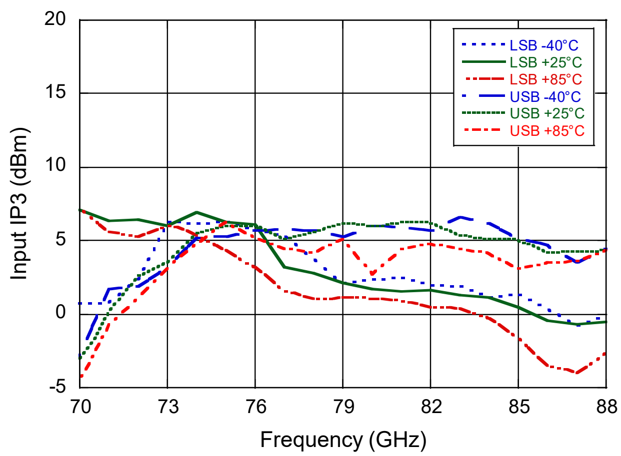
Input Referred IP3 at Nominal Bias at IF = 700 MHz[7]



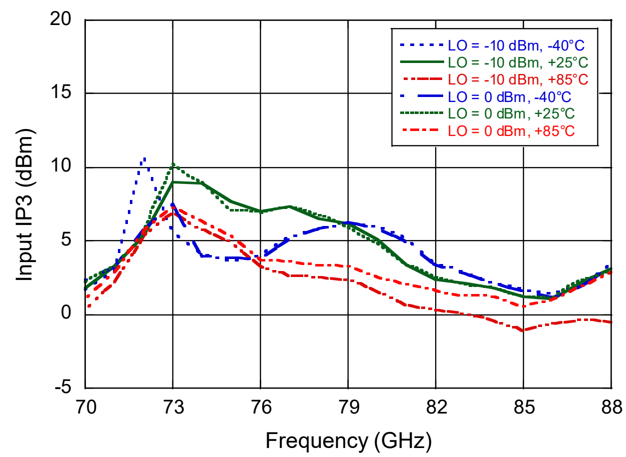
Input Referred IP3 vs. LO Bias at IF = 21.4 MHz



Input Referred IP3 at Nominal Bias at IF = 4 GHz[7]



Input Referred IP3 vs. LO Power at IF = 21.4 MHz



7. ΔIF is 11 MHz

Typical Performance Curves over Temperature

Conversion Gain to each IF vs. IF, RF = 71 GHz

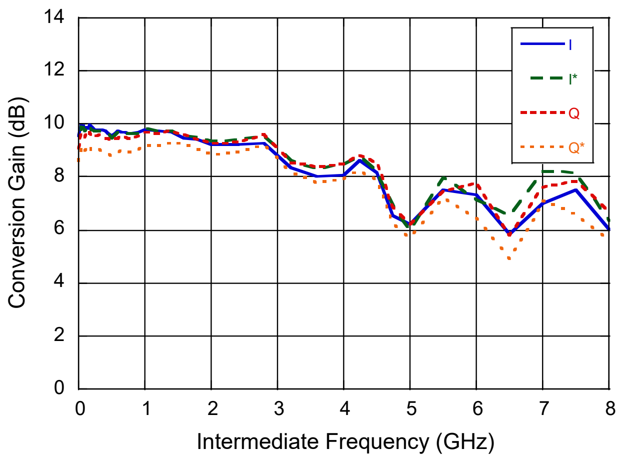
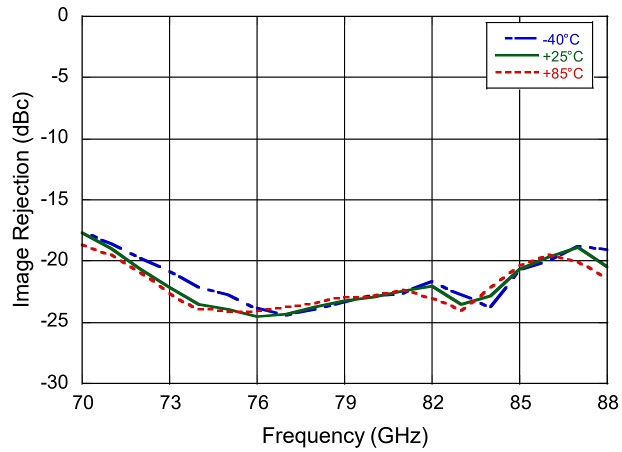


Image Rejection at IF = 21.4 MHz



Conversion Gain to each IF vs. IF, RF = 86 GHz

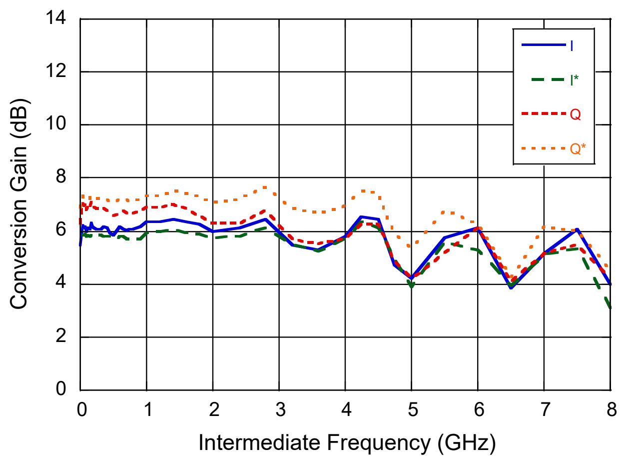


Image Rejection at IF = 700 MHz

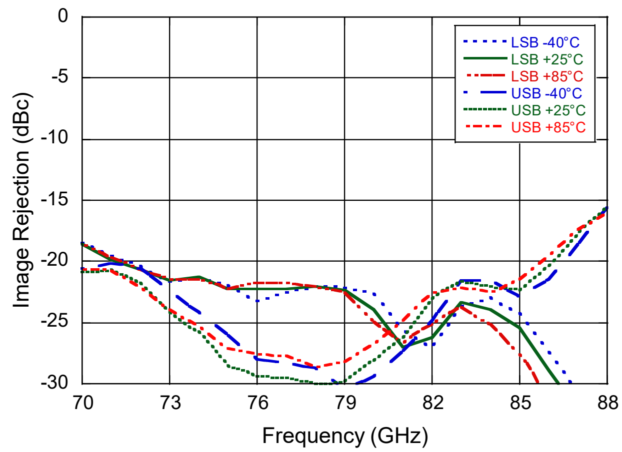
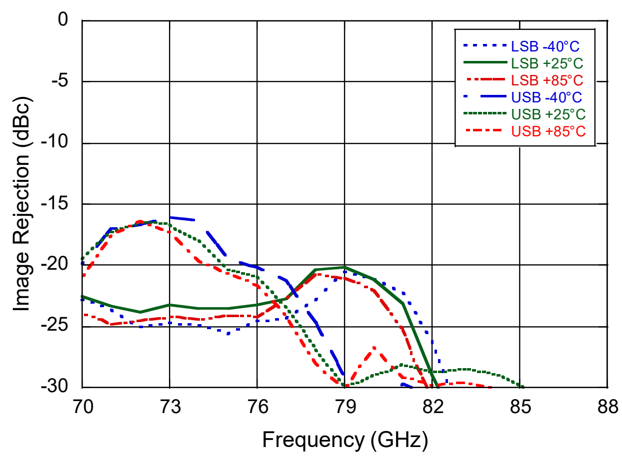
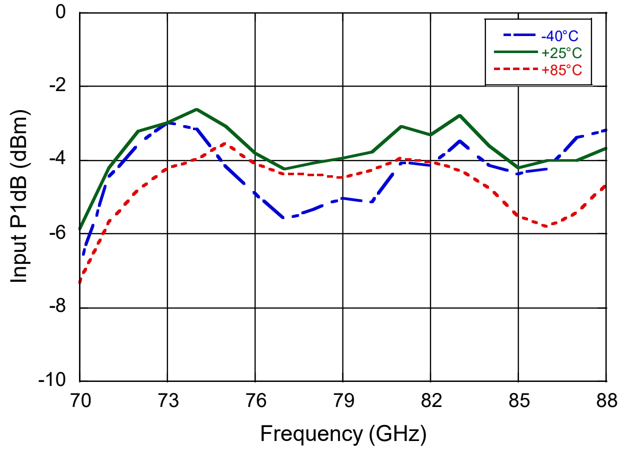


Image Rejection at IF = 4 GHz

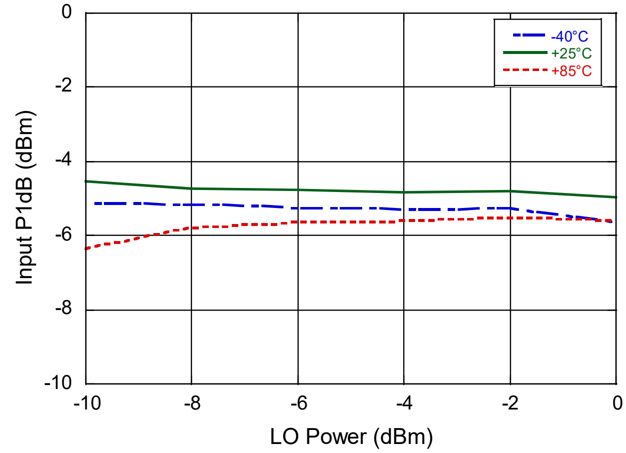


Typical Performance Curves over Temperature

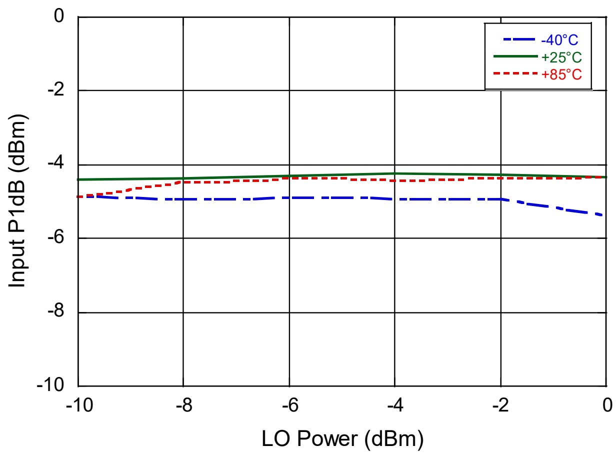
P1dB at Nominal Bias at IF = 21.4 MHz



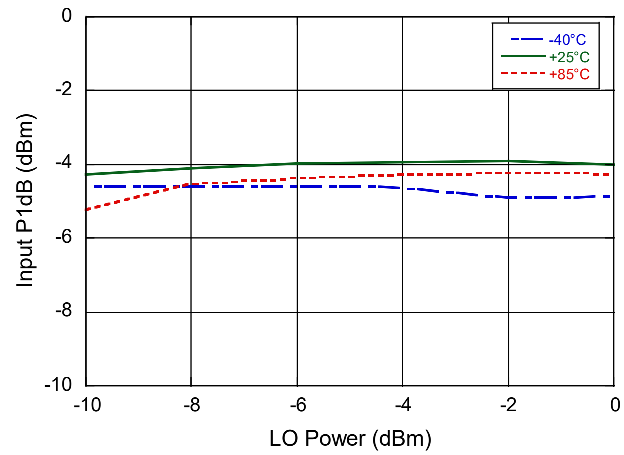
P1dB vs. LO Power at IF = 21.4 MHz, RF = 71 GHz



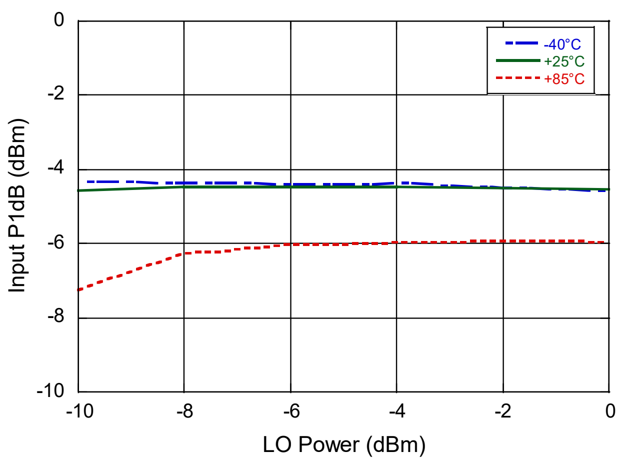
P1dB vs. LO Power at IF = 21.4 MHz, RF = 76 GHz



P1dB vs. LO Power at IF = 21.4 MHz, RF = 81 GHz

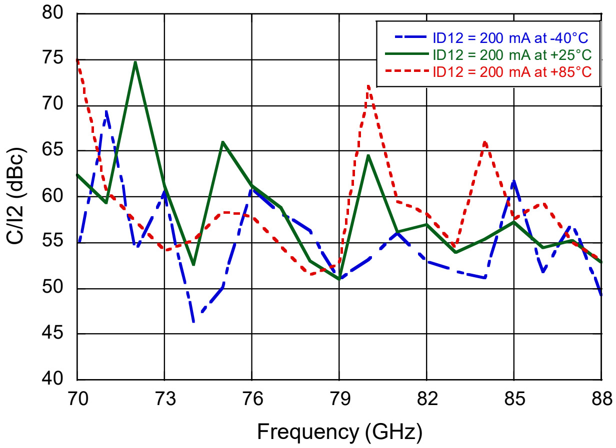


P1dB vs. LO Power at IF = 21.4 MHz, RF = 86 GHz

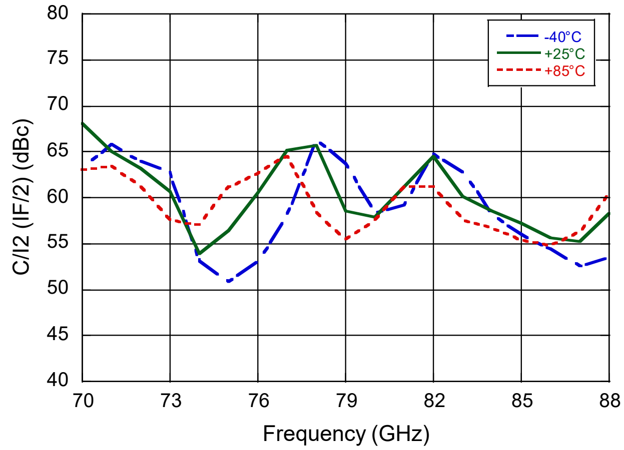


Typical Performance Curves over Temperature

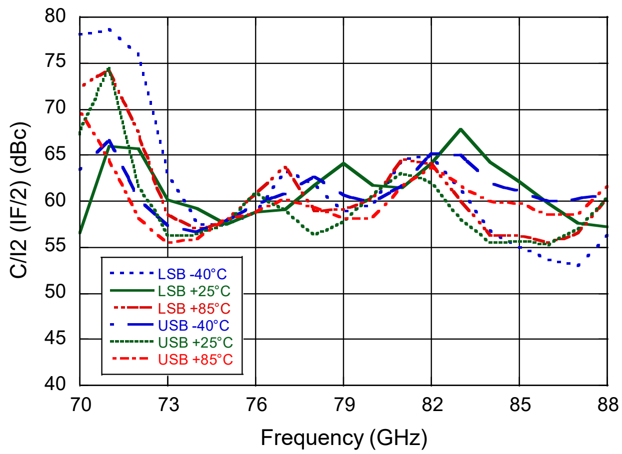
Two-Tone C/I2 at Pin = -27 dBm total at IF = 21.4 MHz



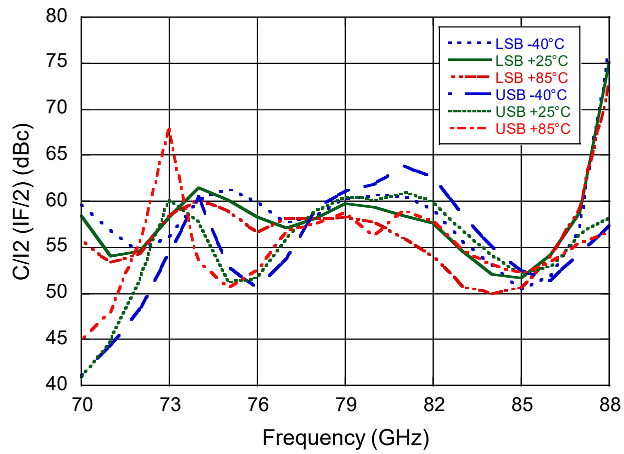
Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 21.4 MHz



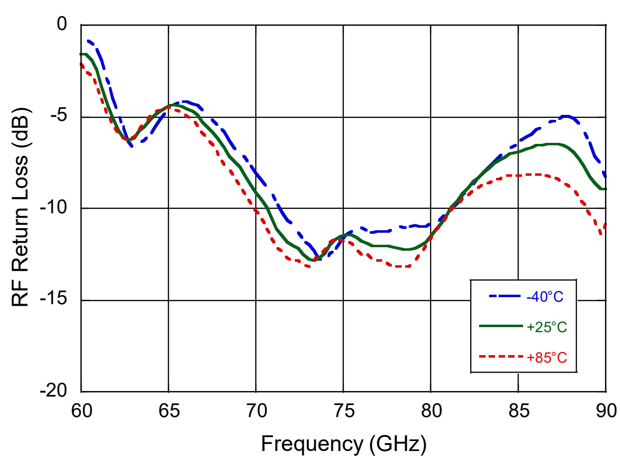
Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 700 MHz



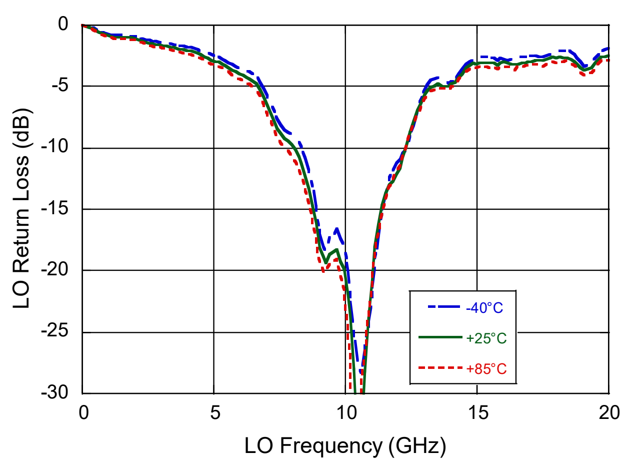
Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 4 GHz



RF Return Loss

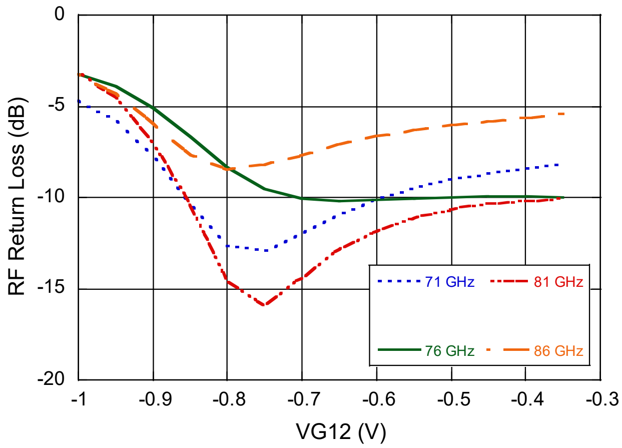


LO Return Loss

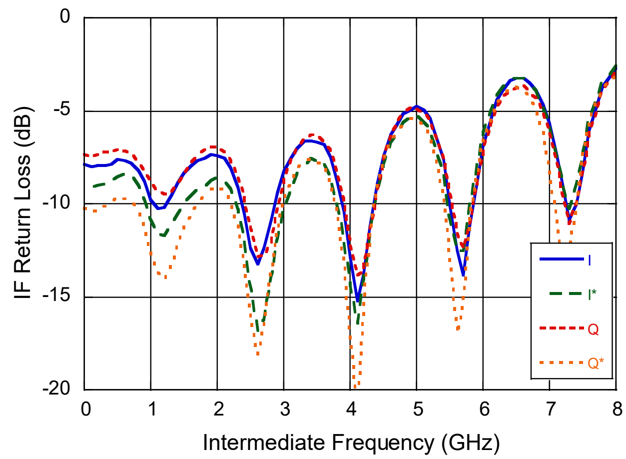


Typical Performance Curves over Temperature

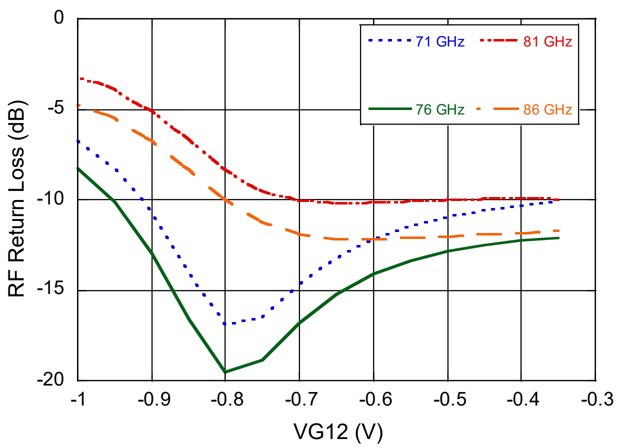
RF Return Loss vs. VG12 Sweep, Temp = -40°C



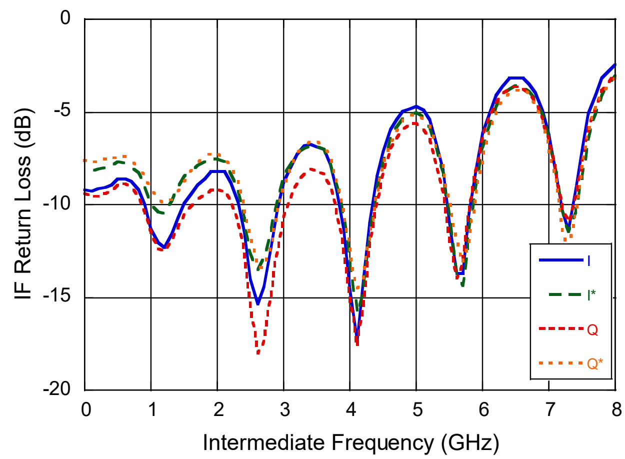
IF Return Loss, ID12 = 150 mA, Temp = -40°C



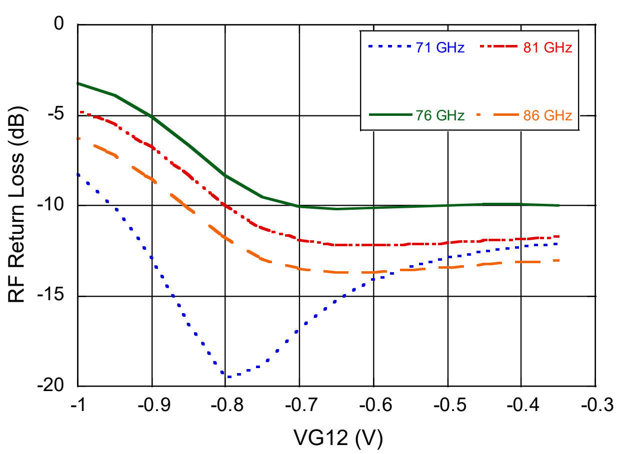
RF Return Loss vs. VG12 Sweep, Temp = +25°C



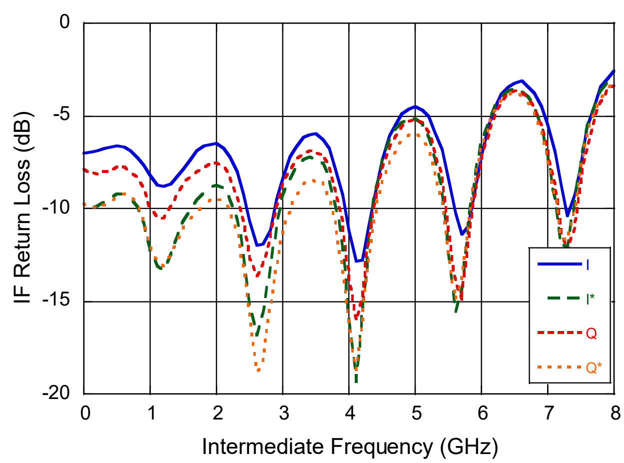
IF Return Loss, ID12 = 200 mA, Temp = +25°C



RF Return Loss, VG12 Sweep, Temp = +85°C

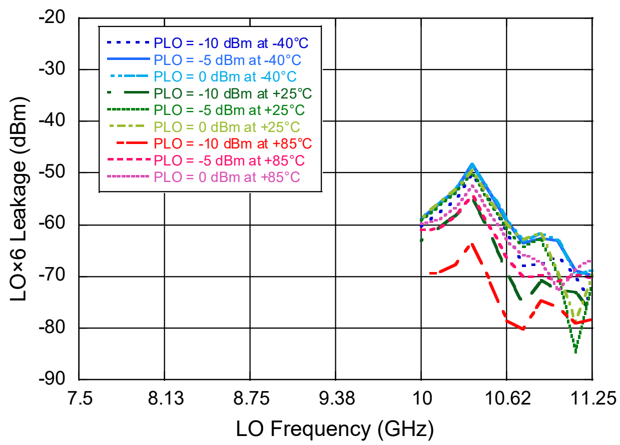


IF Return Loss, ID12 = 250 mA, Temp = +85°C

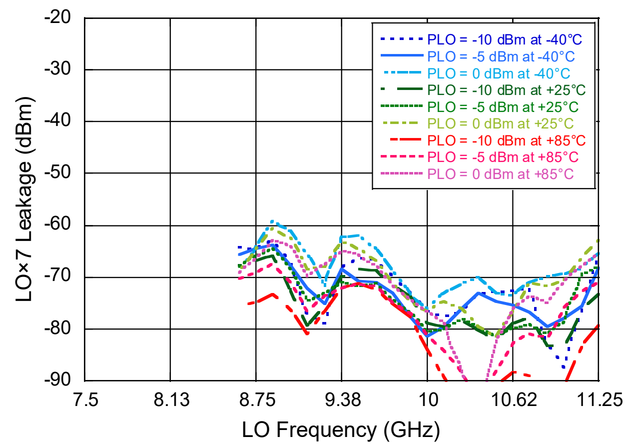


Typical Performance Curves over Temperature

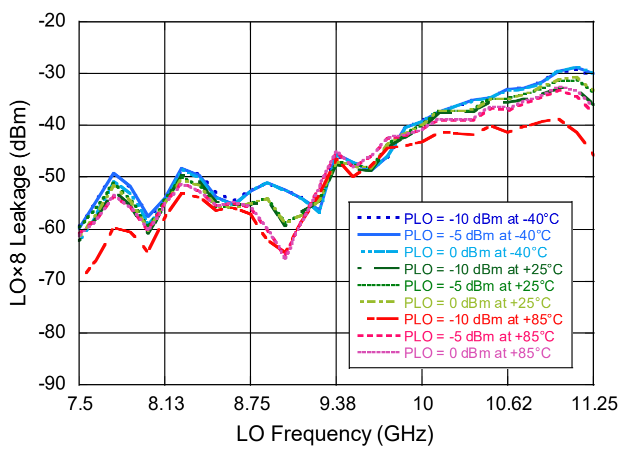
LO×6 Leakage at RF port with No IF



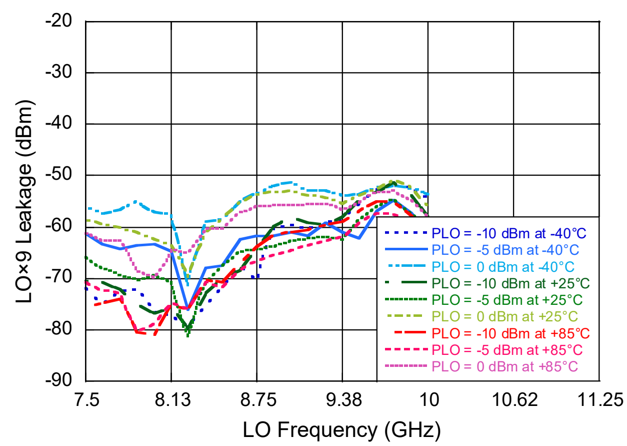
LO×7 Leakage at RF port with No IF



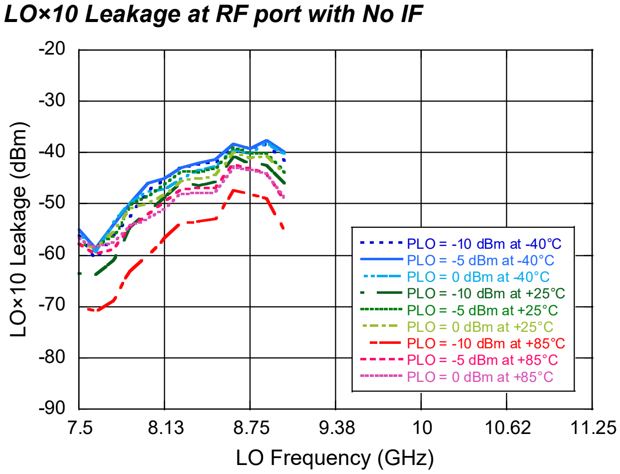
LO×8 Leakage at RF port with No IF



LO×9 Leakage at RF port with No IF



LO×10 Leakage at RF port with No IF



Biasing Methods

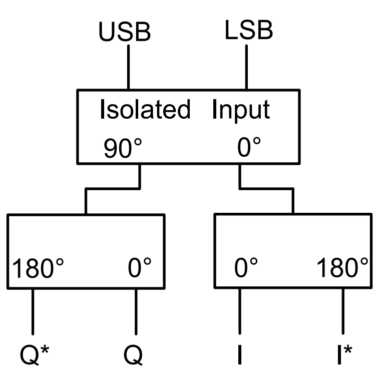
The datasheet presents two different methods for biasing. The first one is to actively biased with a fixed current. This provides a method that consistently groups packages between different manufacturing lots, however it will show variation in gain versus temperature.

The second method is also an active bias, however it is tuned over temperature to maintain constant gain level. This current compensation is a more complex method of biasing but enables consistent performances over both temperature and manufacturing lots.

Bias Sequencing

All gates should be pinched off (VG < -2 V) before the drain voltage (VD = 3 V) is applied. This requirement includes VG5 even though there is no external drain voltage. The gate voltages should then be adjusted as per bias table on Page 2. The current will change when LO is applied to stages three and four.

LSB/USB Operation



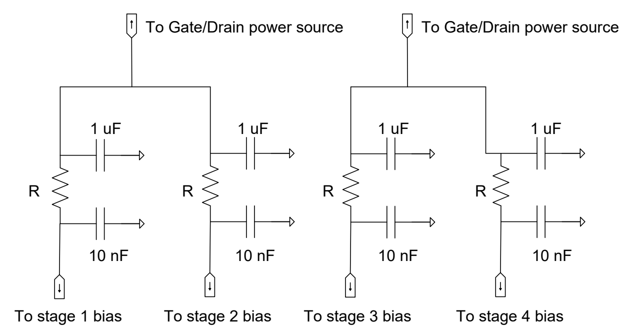
DC Bypassing

Each pin is required to have bypass capacitors. The recommendation is to have 10 nF capacitors close to the package as possible and 1 μF capacitors where space permits. It is not recommended to use 100 pF capacitors due to parallel capacitor resonances with internally mounted capacitors.

When gate stages are tied together, it is recommended to have a small series resistance in the order of 10 Ω. Stages that have a similar function can be combined, that is stage one and two (amplification) and stages three and four (LO multiplication).

Due to the current used on drains, series resistance isn't recommended due to the resulting current drop across the resistor. Ferrite beads can be an alternate source used to isolate drain stages. These ferrite beads generally have an impedance of 100 Ω at 100 MHz. The requirement for these beads is dependent on the board layout and how much coupling arises from parallel traces.

If there are multiple capacitors in parallel to ground it is recommended that one of the capacitors has a small series resistor to dequeue the network to avoid parallel capacitor resonances.



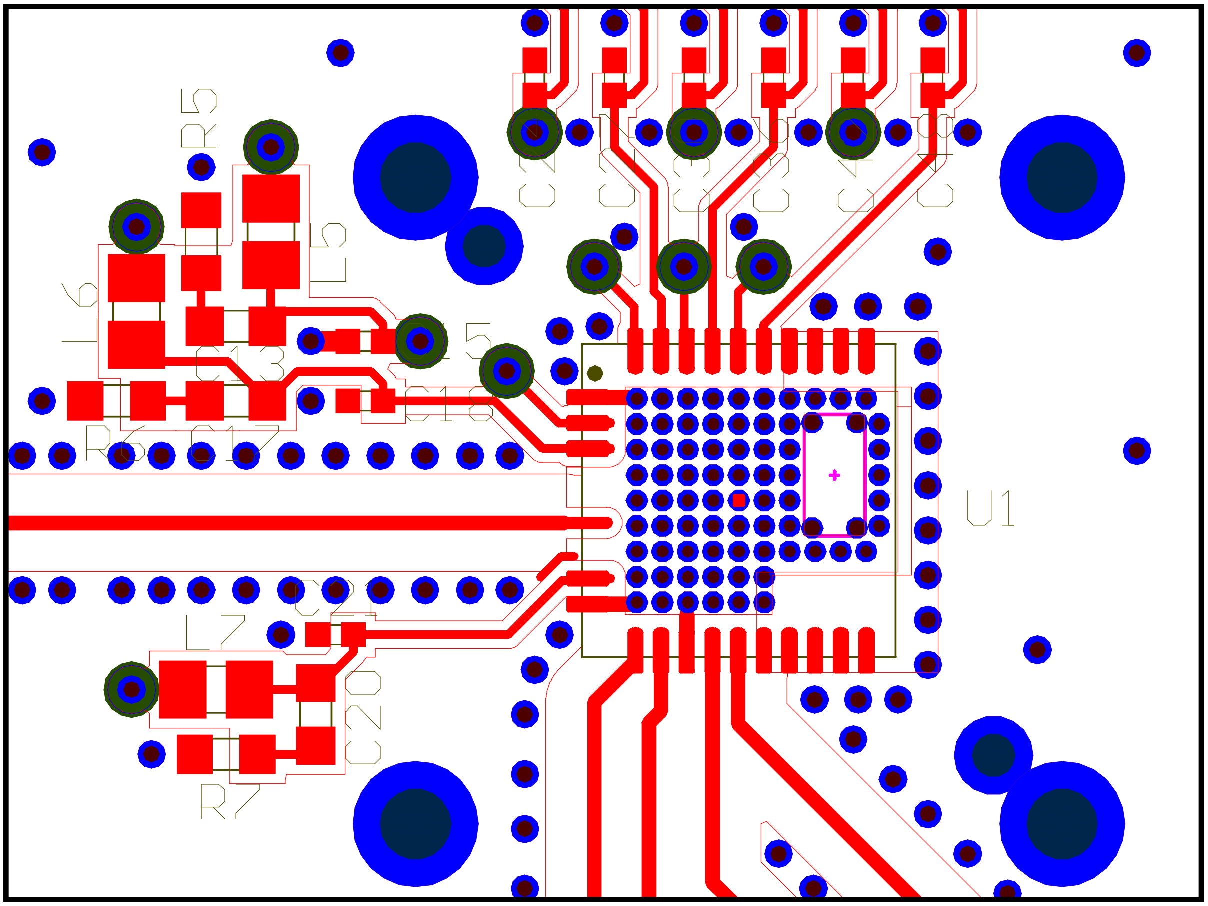
Package Alignment

The SMD package is ideal for pick and place assembly. The package should self align. It is recommended that a solder stencil is used complying with Application Note S2083. To minimize solder flowing into waveguide area, stencil can be inset an additional 25 μm.

Reflow Profile

This package is capable of lead free reflow. The recommended reflow profile depends on the solder used however Application Note S2083 has guidelines that can be applied to this product.

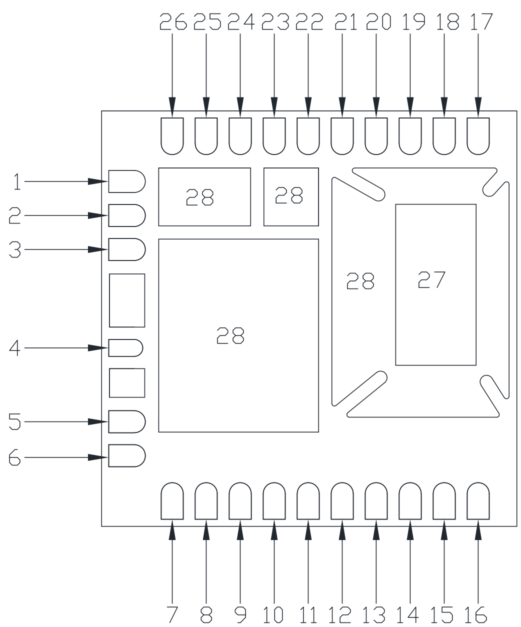
Layout for Evaluation Board



PCB Layout Recommendations

The gerbers, DXF and Altium files for the evaluation board are available on request. It is recommended that VD2 and VD4 DC traces are separated as soon as possible to minimise on board coupling. A simple way to separate the two traces is to have them running on different PCB layers on the board. The image above is a capture of the evaluation board. It can be noted that each adjacent DC trace is alternating on different layers.

Pin Diagram



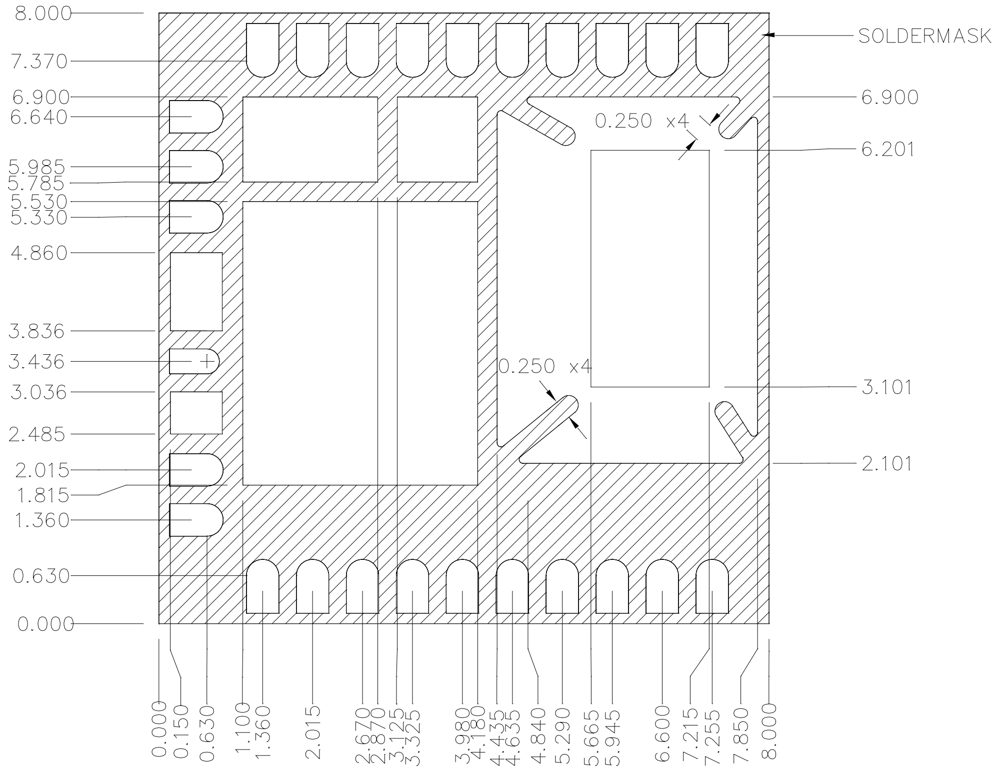
Bottom Layer Viewed From The Top

Pin Table

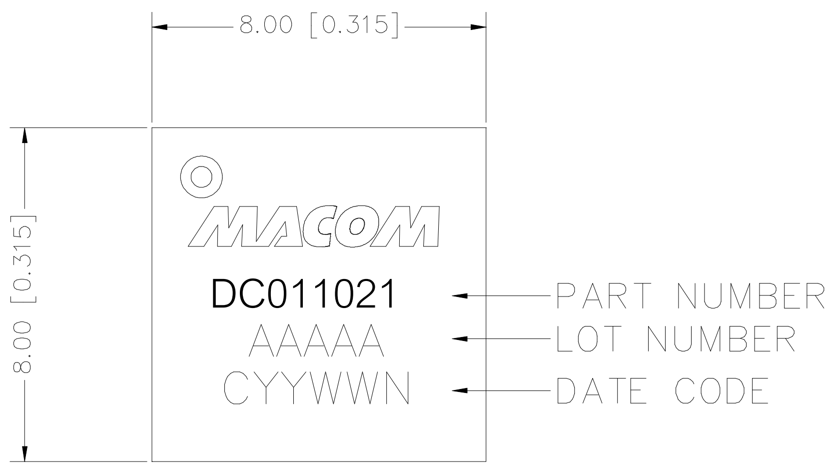
Pin #	Pin Name	Function
1	NC[8]	Not Connected
2	VD3	LO Multiplier Stage
3	VG3	LO Multiplier Stage
4	LO	Local Oscillator Input
5	VG5	Mixer Bias
6	NC[8]	Not Connected
7	Q*	IF Port
8	Q	IF Port
9	NC[8]	Not Connected
10	I	IF Port
11	I*	IF Port
12 - 20	NC[8]	Not Connected
21	VG1	LNA Stage 1
22	VD1	LNA Stage 1
23	VG2	LNA Stage 2
24	VD2	LNA Stage 2
25	VD4	LO Multiplier Post Amplifier
26	VG4	LO Multiplier Post Amplifier
27	RF	WR12 Port
28	Paddle[9]	Ground

8. For optimum RF performance, all NCs should be terminated to ground.
9. The exposed paddle centered on the package bottom must be connected to RF, DC and thermal ground.

Layout Dimensions



Bottom Layer Viewed From The Top



Top View

Major dimensions provided are in millimeters [inches]
DXF of footprint can be provided on request
Reference Application Note M538/S2083 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level (MSL) 3 requirements.