Quad PIN Diode π Attenuator
10 - 4000 MHz

AEC-Q101

MAAV-011019-Q1225T
Rev V1

Features

- AEC-Q101 Qualified
- 4 PIN diodes in a SOT-25 Plastic Package
- Externally Selectable Bias & RF Matching Network
- 10 - 4,000 MHz Useable Frequency Band
- 43 dBm IP3 @ 1000 MHz (50 Ω)
- 1 dB Loss @ 1000 MHz (50 Ω)
- 30 dB Attenuation @ 1000 MHz (50 Ω)
- Lead-Free SOT-25 Package
- 100% Matte Tin Plating over Copper
- RoHS* Compliant

Applications

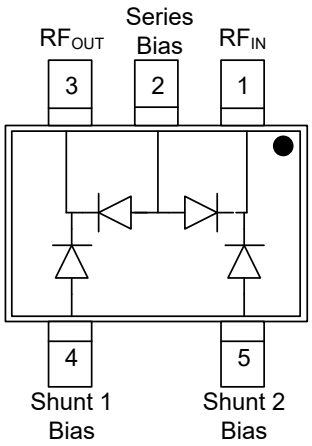
- Automotive Smart Antenna Systems
- TCU and Compensator Blocks

Description

The MAAV-011019-Q1225T is a wideband, lower insertion loss, high IP3, quad PIN diode attenuator in a lead free surface mount SOT-25 package. Four PIN diodes in one package reduce design parasitics and improve circuit density.

These PIN diode attenuators perform well where RF signal amplitude control is required in 50 Ω systems. Exceptional insertion loss, attenuation range, and IP3 at <10 mA suitable for better power level control in RF amplifiers.

Functional Schematic



Pin Configuration

Pin #	Function
1	RF_{IN}
2	Series Bias
3	RF_{OUT}
4	Shunt 1 Bias
5	Shunt 2 Bias

Ordering Information[1]

Part #	Package
MAAV-011019-Q1225T	Tape and Reel

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Typical 50 Ω Performance[2] @ +25°C using Wideband RF Circuit Design

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	1000 MHz 3.0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dB	—	-2 -1	—
Return Loss	1000 MHz 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dB	—	-10	—
Attenuation	1000 MHz 0 mA - Series Diode Bias / 0.75 V - Shunt 1 and 2 Bias	dB	—	-29	—
Input IP3	F1 = 1000 MHz, F2 = 1100 MHz 0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias F1 = 100 MHz, F2 = 110 MHz 0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dBm	—	43 43 43 33	—
Settling Time	1000 MHz Within 1 dB of Final Attenuation Value	us	—	3	—
RF C.W. Incident Power	0 - 20 V Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dBm	—	20	—

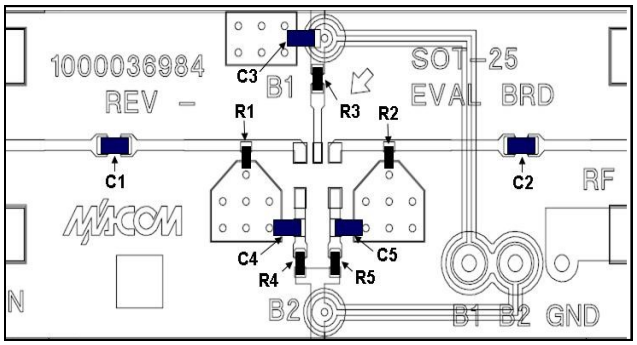
2. Values shown include through loss calibrated out of RF test circuit.

Absolute Maximum Ratings[4,5]

Parameter	Absolute Maximum
DC Voltage @ Temperature Extremes	-100 V
DC Current	75 mA
Operating Temperature	-65°C to +125°C
Storage Temperature (no Dissipated Power)	-65°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.

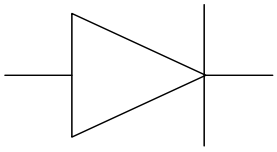
Recommended PCB Layout



Parts List

Part	Value	Case Style	Manufacturer
C1, C2, C3, C4, C5	100 pF	0603	Murata
R1, R2, R3, R4, R5	1000 Ω	0402	Panasonic

MAAV-011019-Q1225T Spice Model

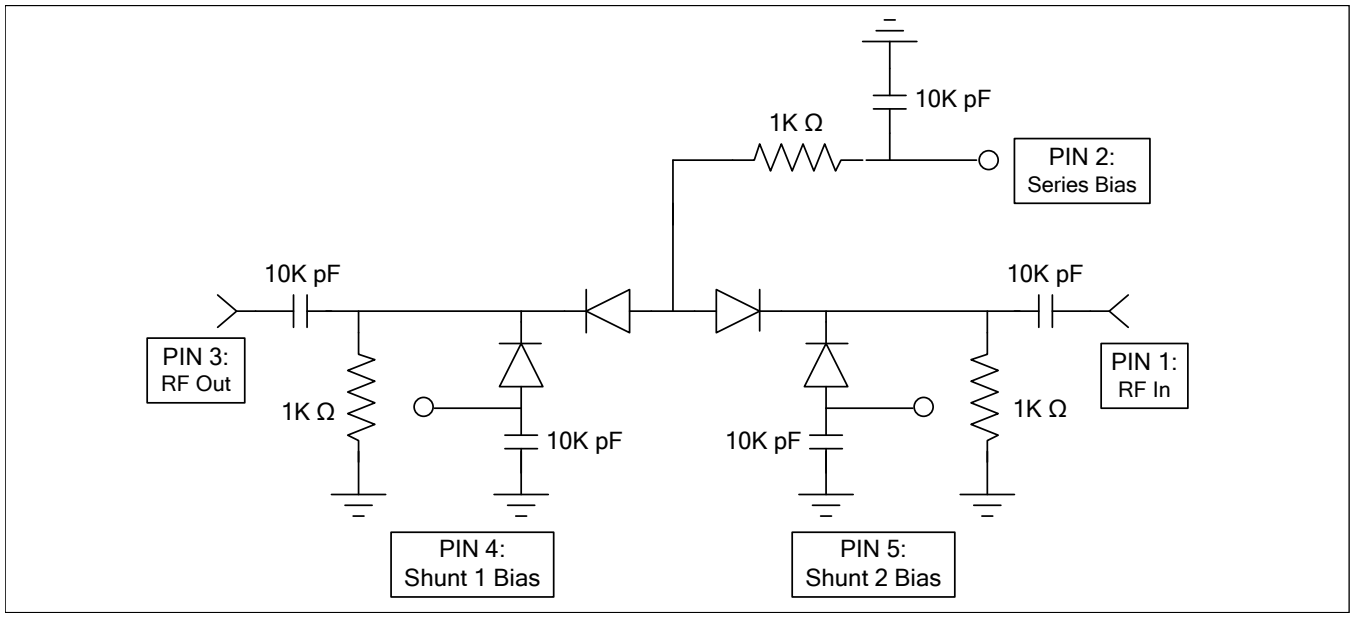


Pin Diode Model
NLPINM2
Is = 1E-14 A
Vi = 0 V
Un = 900 cm^2/V-sec
Wi = 60 um
Rr = 1.25 Ohm
Cmin = 0.20 pF
Tau = 1.0 usec
Rs = 0.1 Ohm
Cjo = 0.27 pF
Vj = 0.7 V
M = 0.5
Fc = 0.5
Imax = 2.5E+6 A/m^2
Kf = 0
Af = 1
Ffe = 1
wBV = 150 V

Series & Shunt Diode Bias Currents as a Function of Vseries & Vshunt Voltage (Values shown are PER DIODE)

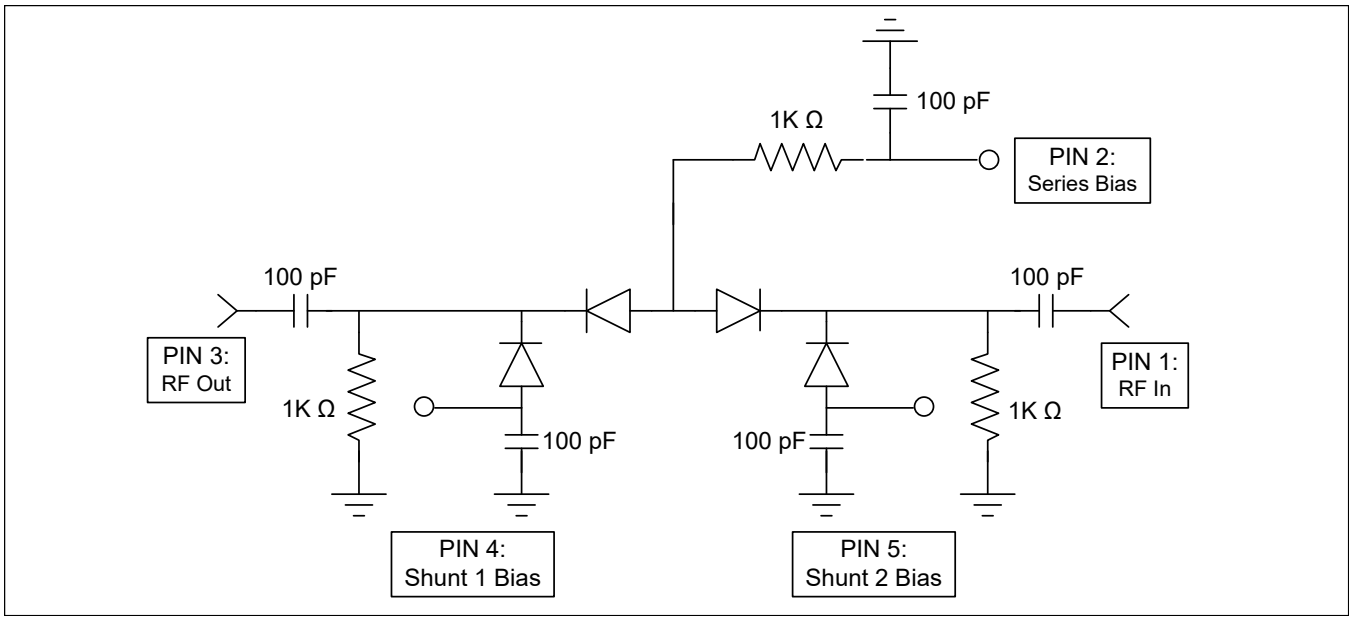
Vshunt Bias (V)	Vseries Bias (V)	Iseries Diode (mA)	Ishunt Diode (mA)
0.75	0	0.000	0.192
0.75	1	0.106	0.120
0.75	2	0.443	0.048
0.75	3	0/773	0
0.75	4	1.099	0
0.75	5	1.426	0
0.75	6	1.750	0
0.75	7	2.092	0
0.75	8	2.424	0
0.75	9	2.756	0
0.75	10	3.088	0
0.75	11	3.421	0
0.75	12	3.754	0
0.75	13	4.087	0
0.75	14	4.410	0
0.75	15	4.743	0
0.75	16	5.081	0
0.75	17	5.406	0
0.75	18	5.750	0
0.75	19	6.079	0
0.75	20	6.413	0

Schematic 10 - 1000 MHz, 50 Ω, RF Circuit[9]



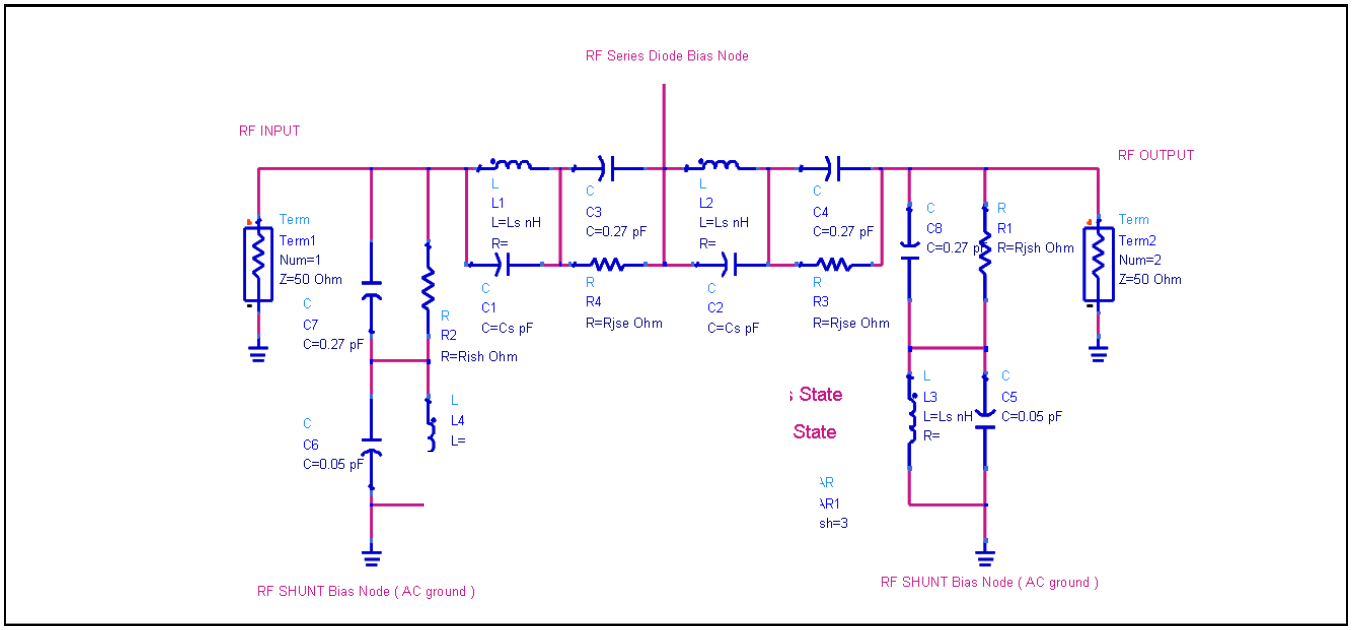
9. Keeping PIN 4 & PIN 5 as Separate Bias Points (Same V) reduces RF leakage (increases attenuation) through an otherwise connected Common Anode Bias Note.

Schematic 1 - 4 GHz, 50 Ω, RF Circuit[10]

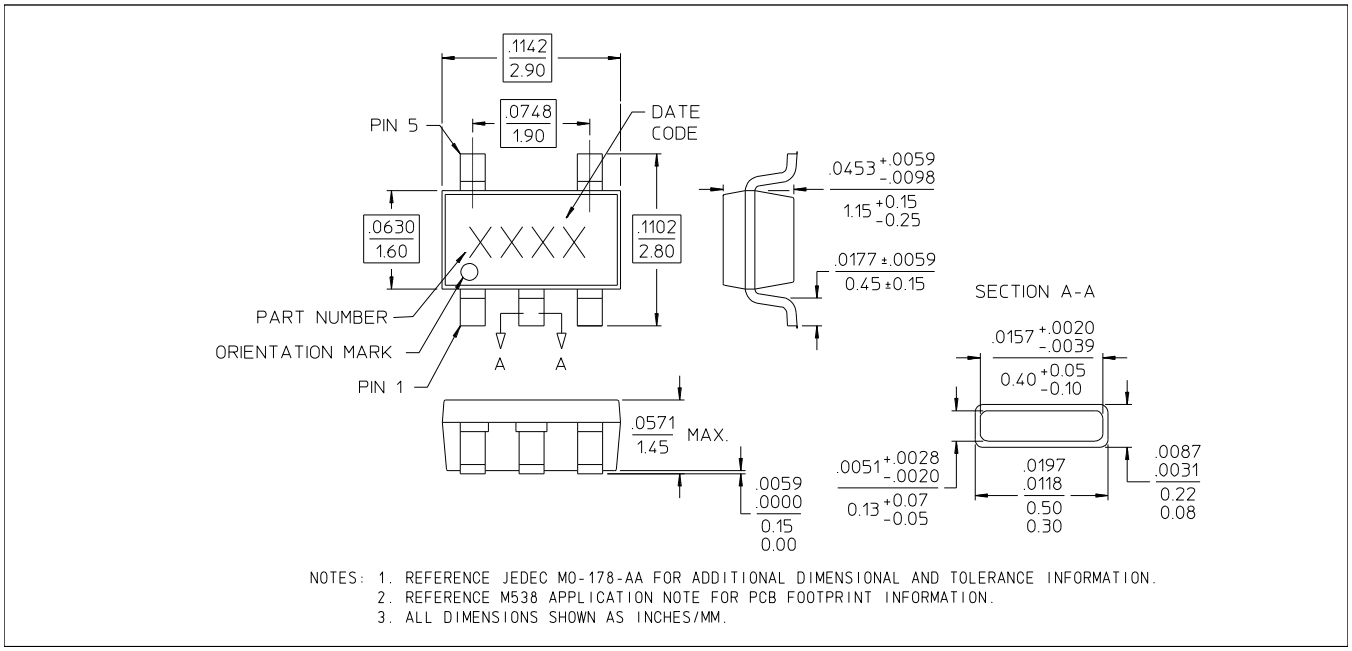


10. Keeping PIN 4 & PIN 5 as Separate Bias Points (Same V) reduces RF leakage through an otherwise connected Common Anode Bias Node.

Lumped Element Model for MAAV-01109-Q1225T PIN Diode π Attenuator in SOT-25



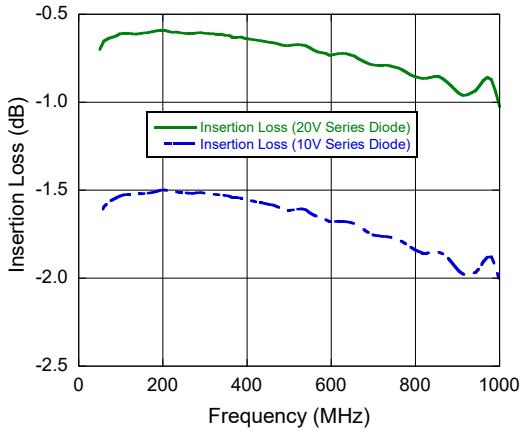
Lead Free SOT-25 †



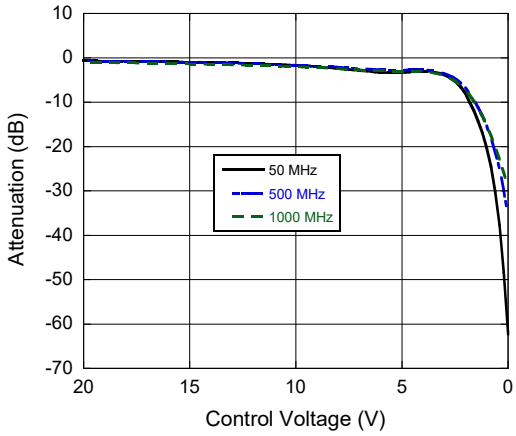
† Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.

Typical Performance Curves @ +25°C, 50 - 1000 MHz, Shunt Bias = 0.75 Volts

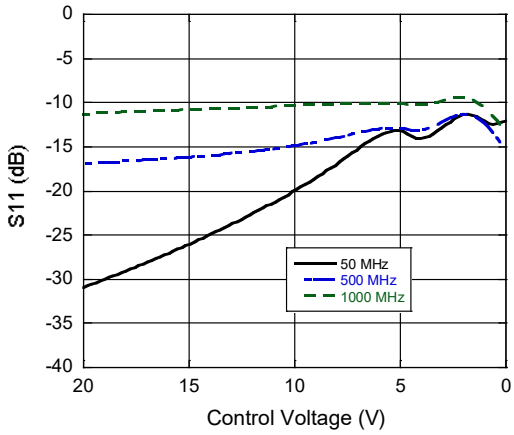
Insertion Loss vs. Frequency



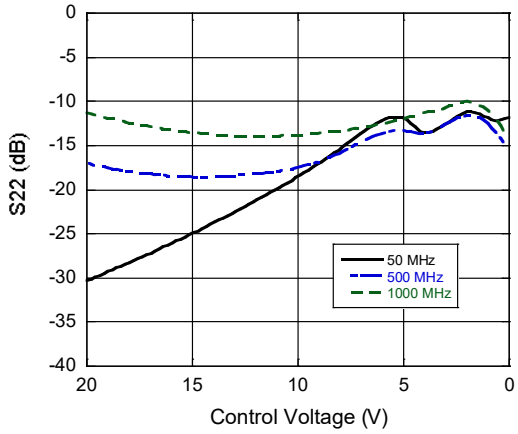
Attenuation vs. Control Voltage



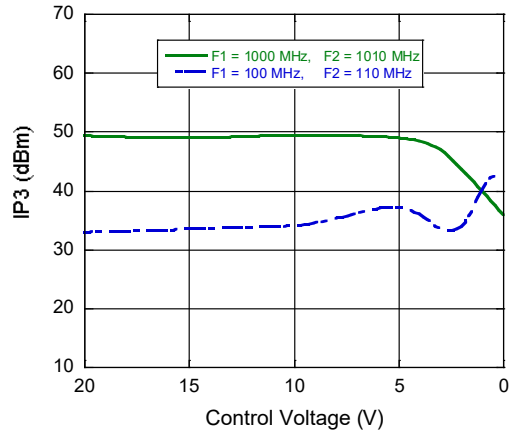
Input Return Loss vs. Control Voltage



Output Return Loss vs. Control Voltage

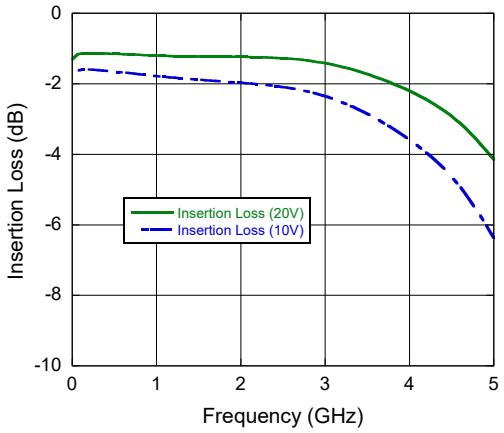


IP3 vs. Control Voltage

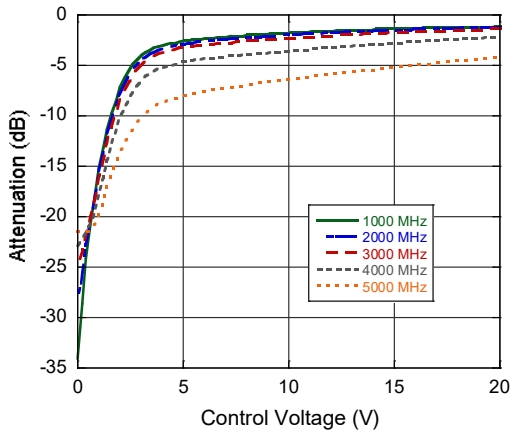


Typical Performance Curves @ +25°C, 1000 - 5000 MHz, Shunt Bias = 0.75 Volts

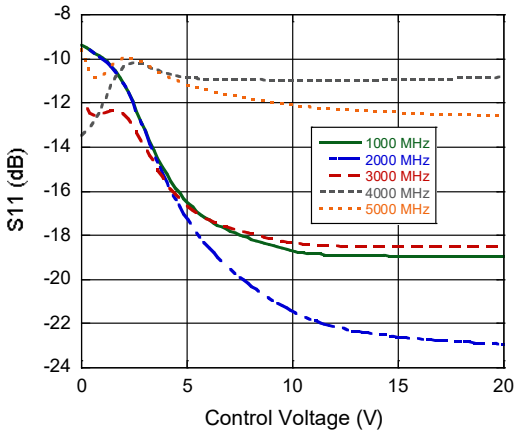
Insertion Loss vs. Frequency



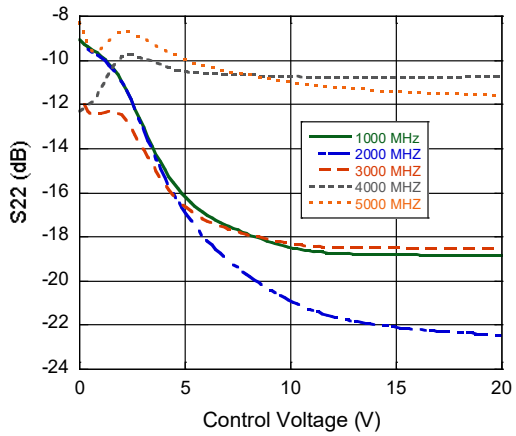
Attenuation vs. Control Voltage



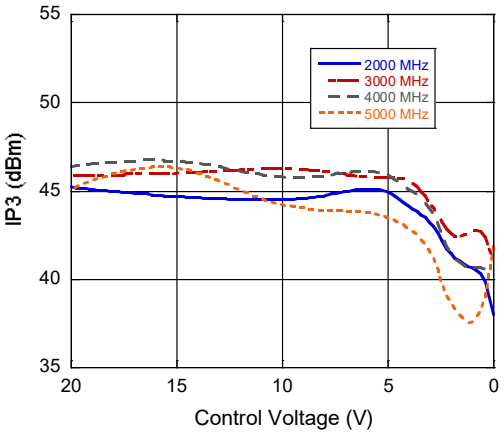
Input Return Loss vs. Control Voltage



Output Return Loss vs. Control Voltage



IP3 vs. Control Voltage (10 MHz Spacing)



P1dB vs. Control Voltage