Features

- High Gain: 28 dB
- P1dB: 29 dBm
- P3dB: 31 dBm
- Output IP3: 42 dBm
- Bias Voltage: V_{DD} = 4 V
- Bias Current: I_{DSQ} = 2850 mA
- 50 Ω Matched Input / Output
- Output Power Detector
- Die Size: 4.0 x 4.3 x 0.05 mm
- RoHS* Compliant

Applications

- Satellite Communications
- Point-to-Point Communications
- Radar Front Ends
- Test and Measurement
- Automotive Radar

Description

The MAAP-011388-DIE is a 1 W power amplifier. The power amplifier operates from 71 to 86 GHz and provides 28 dB of linear gain (at nominal bias conditions) and 31 dBm of output power at 6 dB compression. The device is fully matched across the band and includes an output power detector. The data contained within this datasheet is probed directly on the die.

The MAAP-011388-DIE can be used as a power amplifier stage or as a driver stage in higher power applications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

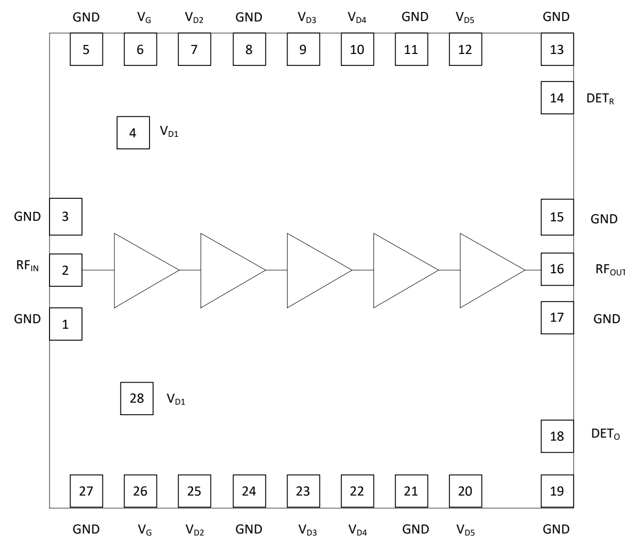
All data was measured on die using RF probes.

Ordering Information

Part Number	Package
MAAP-011388-DIE	Gel Pack[1]

1. Die quantity varies.

Functional Schematic



Pin Configuration[2]

Pin #	Pin Name	Description
1,3,15,17	RF GND	RF ground
2	RF_{IN}	RF Input
4, 28	V_{D1}	Drain voltage 1
5,8,11,13, 19,21,24,27	DC GND	DC ground
6,26	V_G	Gate voltage
7,25	V_{D2}	Drain voltage 2
9,23	V_{D3}	Drain voltage 3
10,22	V_{D4}	Drain voltage 4
12,20	V_{D5}	Drain voltage 5
14	DET_R	Detector Reference
16	RF_{OUT}	RF Out
18	DET_O	Detector Output
		Backside of die[2]

2. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
T_A = +25°C, V_{DD} = 4 V, I_{DSQ} = 2850 mA, Z_0 = 50 Ω Probed On-Wafer

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	71 GHz 76 GHz 81 GHz 86 GHz	dB	25.0 25.0 23.5 21.0	28.0 30.0 28.0 27.0	—
P_{OUT}	P_{IN} = +10 dBm 71 GHz 76 GHz 81 GHz 86 GHz	dBm	30.5 30.5 29.0 25.0	31.5 31.5 30.5 29.5	—
P1dB	71 - 76 GHz 81 - 86 GHz	dBm	—	29.5 28.0	—
OIP3	P_{OUT} = +20 dBm/tone (10 MHz Tone Spacing) 71 - 76 GHz 81 - 86 GHz	dBm	—	42 41	—
PAE	P_{IN} = +10 dBm 71 - 86 GHz	%	—	8	—
Input Return Loss	P_{IN} = -20 dBm	dB	—	10	—
Output Return Loss	P_{IN} = -20 dBm	dB	—	12	—

Maximum Operating Ratings

Parameter	Rating
Input Power	12 dBm
Junction Temperature[4,5]	+150°C
Operating Temperature	-40°C to +85°C

4. Operating at nominal conditions with junction temperature ≤ +150°C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θ_{JC}) = 4°C/W.
   a) For I_{DSQ} = 2850 mA, T_C = +85°C, defined as backside of die.
   T_J = 137°C @ 4 V, 3500 mA, P_{OUT} = 30 dBm, P_{IN} = 10 dBm

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power	15 dBm
Drain Voltage	+4.5 V
Gate Voltage	-2 V to +0.3 V
Junction Temperature[8]	+175°C
Storage Temperature	-65°C to +125°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

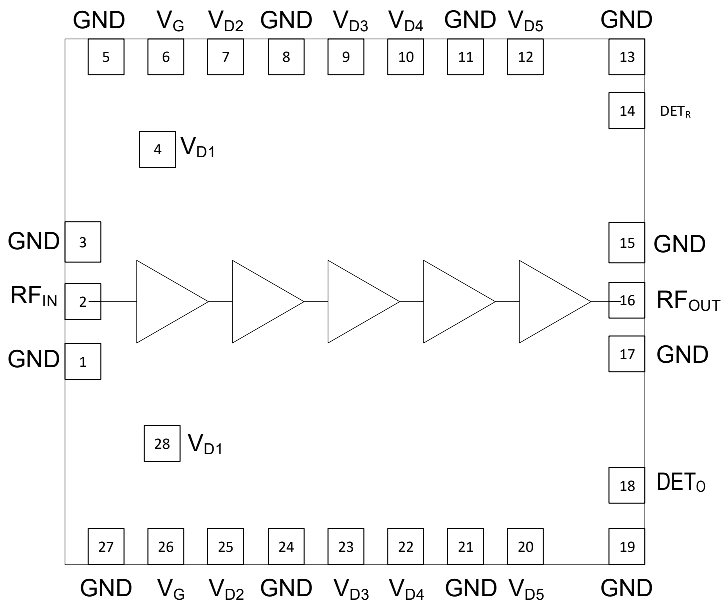
Recommended Operating Conditions

It is recommended to operate at a typical drain voltage of +4 V ±5%. The maximum recommended operating drain current is fundamentally defined by the combination of the maximum operating junction temperature and the power dissipated. This can be calculated as shown in note 5.

Electrostatic Sensitivity

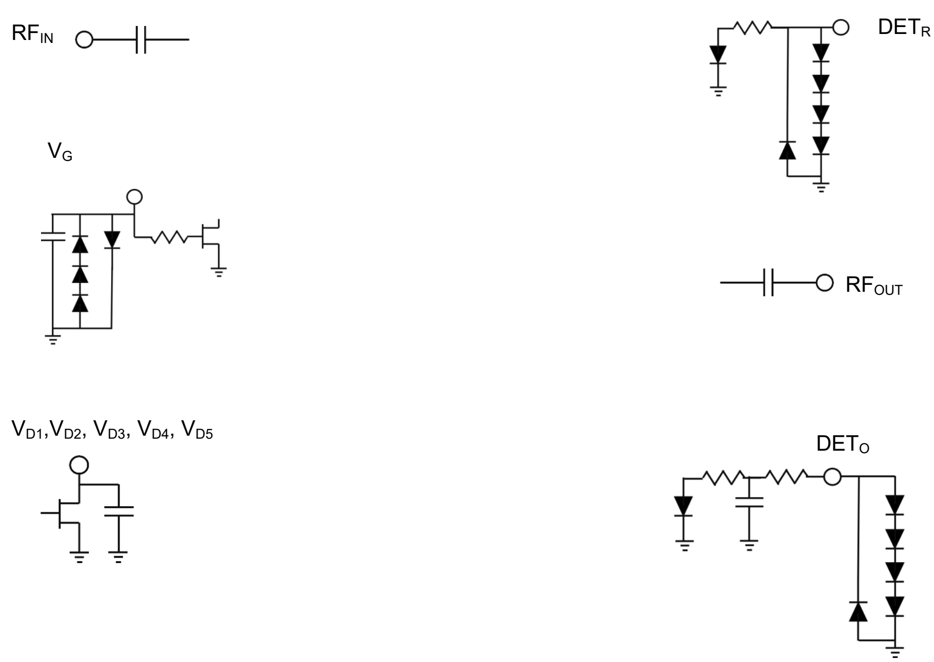
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 1A HBM devices.

Pin Configuration and Functional Descriptions

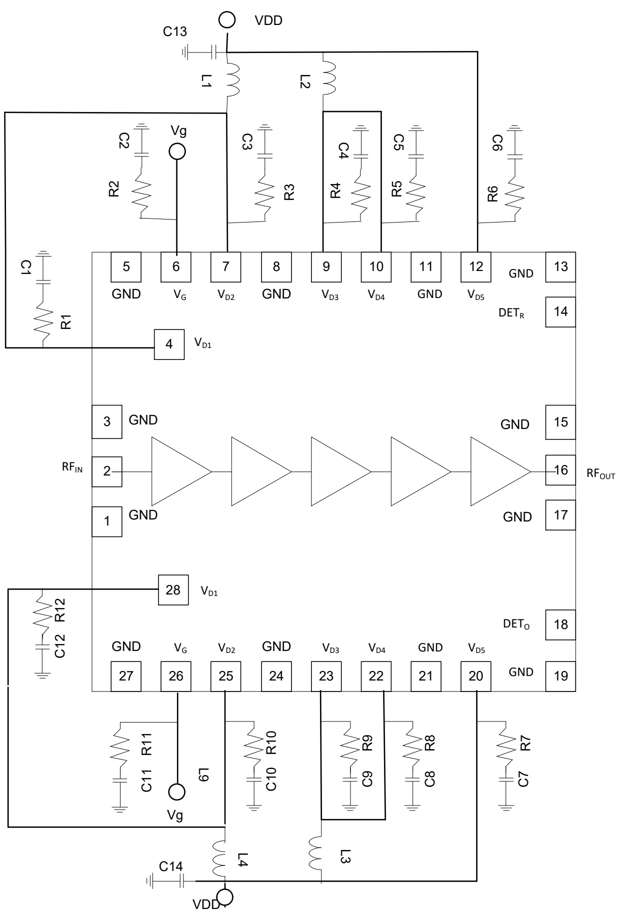


Pin #	Pin Name	Description
1,3,15,17	RF GND	These pads are grounded on the MMIC. They are intended to support both on-wafer G-S-G probing for production test and also the use of RF GND bonds if required in the application.
2	RF_{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
4, 28	V_{D1}	Drain biases for stage 1 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pads 4 and 28 and so both pins need to be externally connected to the same voltage.
5,26	V_G	Power amplifier gate controls. Adjust V_G from –1.5 V to 0 V to achieve the desired quiescent current. External bypass capacitors and de-Q resistors are required as described in the applications schematic. There is no internal connection between pads 5 and 26 and so both pins need to be externally connected to the same voltage.
7,25	V_{D2}	Drain biases for stage 2 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pads 7 and 25 and so both pins need to be externally connected to the same voltage.
9,23	V_{D3}	Drain biases for stage 3 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pads 9 and 23 and so both pins need to be externally connected to the same voltage.
10,22	V_{D4}	Drain biases for stage 4 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pads 10 and 22 and so both pins need to be externally connected to the same voltage.
12,20	V_{D5}	Drain biases for stage 5 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pads 12 and 20 and so both pins need to be externally connected to the same voltage.
14	DET_R	Detector Diode Reference voltage. This provides a reference voltage to compensate for temperature effects of the power detector output (DET_O). An external comparator circuit can be used as described in the applications section.
16	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled
18	DET_O	Detector Diode Output voltage. When biased using an external resistor as described in the applications section, this provides an output voltage proportional to the RF output power. Used in conjunction with DET_R, temperature effects can be compensated for. The voltage DET_R—DET_O is a temperature compensated DC voltage proportional to the RF output power of the PA.

Interface Schematics



Application Schematic



Bill of Materials

Part	Value	Size	Comment
C1-C12	0.01 µF	0402	bypass
C13-C14	10 µF	0603	bypass
R1-R12	10 Ω	0402	—
L1-L4	Ferrite Bead	—	RF choke

Application Circuit Notes

The MAAP-011388-DIE incorporates on-chip 100 pF bypass capacitors for all the drain connections. This eliminates the requirement to include 100pF chip capacitors as close as possible to the MMIC. However, these can be included if desired.

C1 to C12 are SMT components which can be mounted on the application PCB, with the appropriate traces being bonded directly to the MMIC. These should be placed as closely as practically possible to the MMIC.

The circuit is not sensitive to the positioning of C13 and C14, however these should be on the same PCB as the rest of the biasing components.

Biasing Conditions

Recommended biasing conditions are V_{DD} = 4 V, I_{DSQ} = 2850 mA

V_G must be applied to pinch off the device before V_{DD} is applied.

V_{DD} Bias must be applied from both north and south bonding pads. V_{DD} and V_G bias lines are not connected internally.

Operating the MAAP-011388-DIE

Turn-on

1. Apply V_G (-1.5 V).
2. Increase V_{DD} to 4 V.
3. Set I_{DSQ} by adjusting V_G more positive (typically -0.55 V for I_{DSQ} = 2850 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -1.5 V.
3. Decrease V_{DD} to 0 V.

Handling Procedures

Please observe the following precautions to avoid damage:

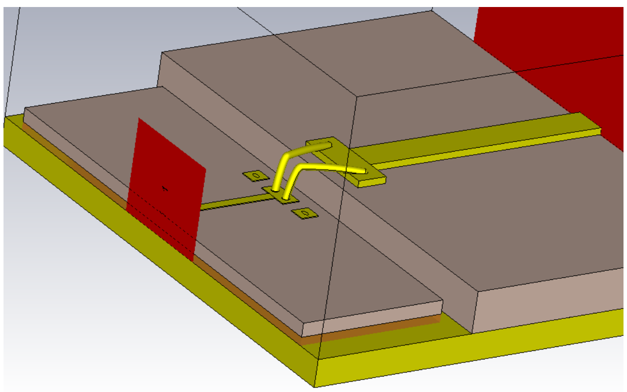
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Wire Bonding

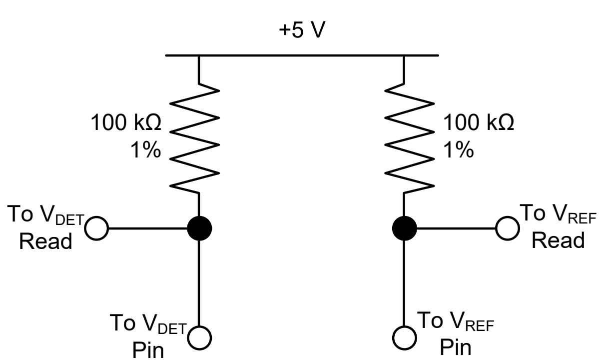
The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below.

Alternatively, a 3 mil bond ribbon could be used.



Detector biasing schematic

As shown in the schematic below, the power detector is implemented by providing 5 V bias and measuring the difference in output voltage. This measure can be achieved by mean of either standard op-amp in a differential mode configuration or analog-to-digital converters.



Handling the Die

This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

Die Attach

For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used.

If using eutectic, an 80% Au / 20% Sn preform is recommended. If using epoxy, a high thermal conductivity epoxy is required and a silver sintering type epoxy is recommended.

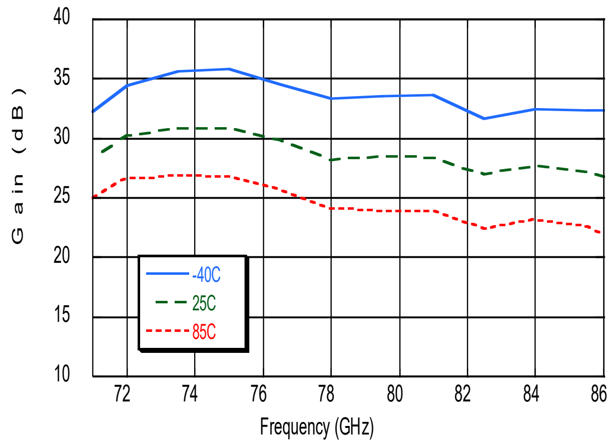
Thermal Considerations

Due to the high power dissipation of this high linearity PA, careful consideration needs to be given to the thermal path in the application. The thermal path to the heatsink must be designed to have sufficiently low thermal resistance to support a maximum of 85ºC temperature at the backside of the die.

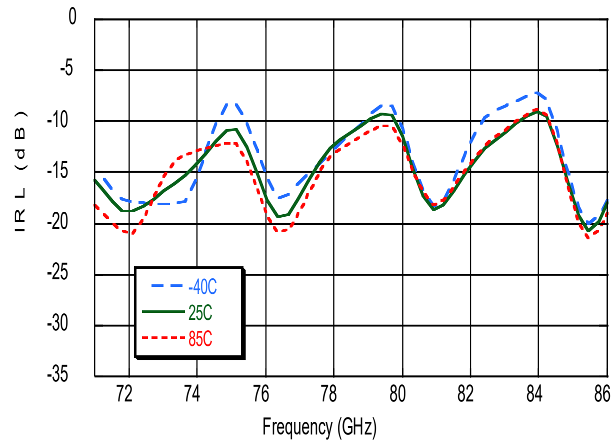
Directly mounting to a metal heatsink using one of the die attach methods outlined is highly recommended. If the MMIC is to be mounted onto a PCB, an embedded copper coin is recommended in the die attach area.

Typical Performance Curves: V_D = 4 V, I_{DSQ} = 2850 mA, Probed On Wafer

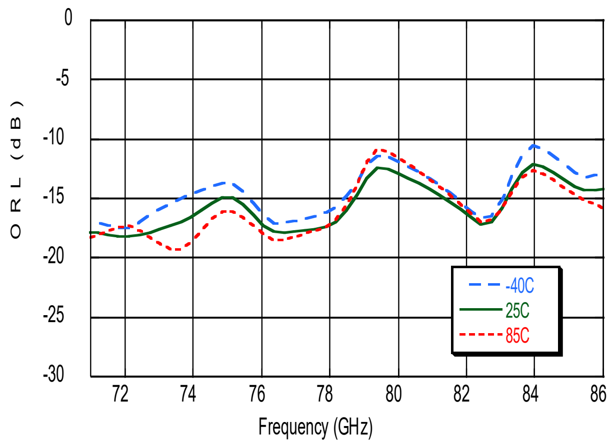
Small Signal Gain vs. Frequency



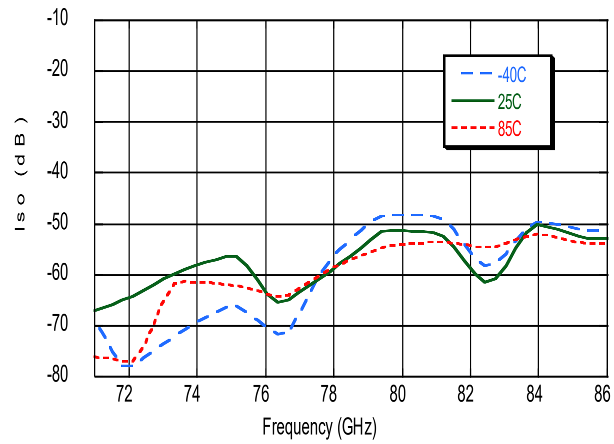
Input Return Loss vs. Frequency



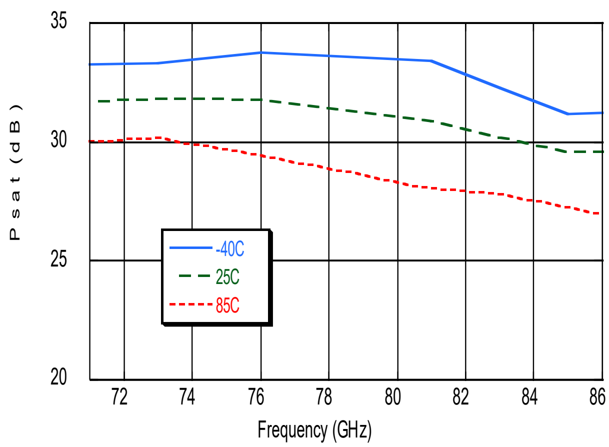
Output Return Loss vs. Frequency



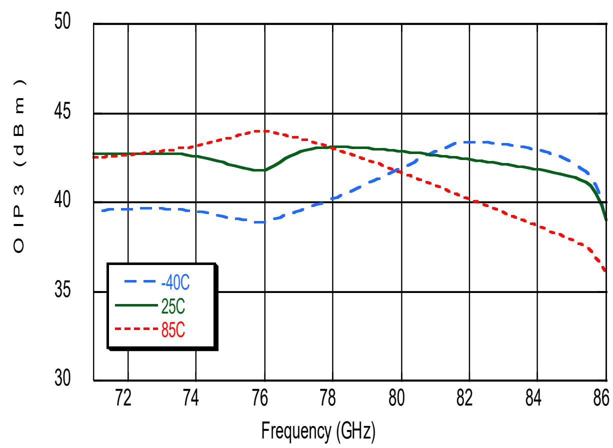
Isolation vs. Frequency @ 25C



Psat vs. Frequency

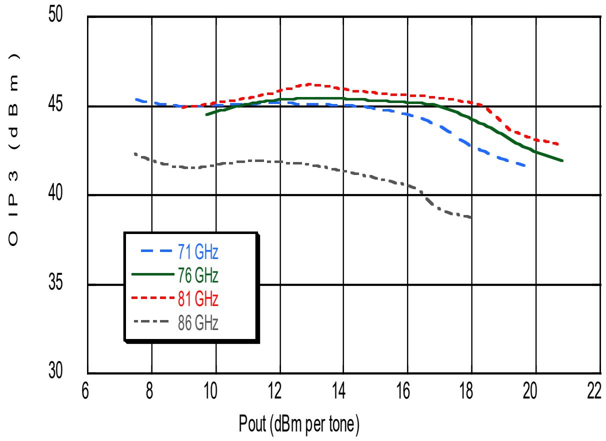


OIP3 vs. Frequency
Pout per Tone 22dBm

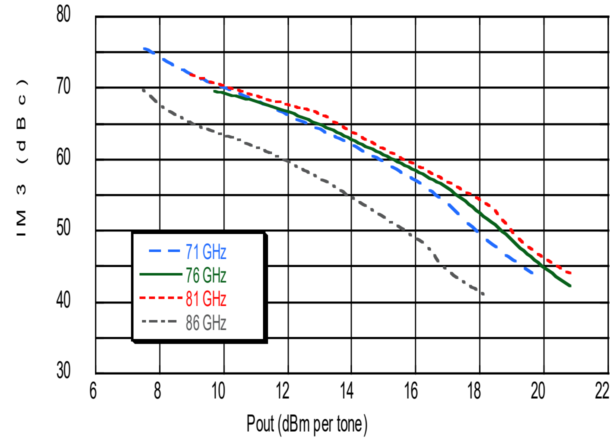


Typical Performance Curves: V_D = 4 V, I_{DSQ} = 2850 mA, Probed On Wafer

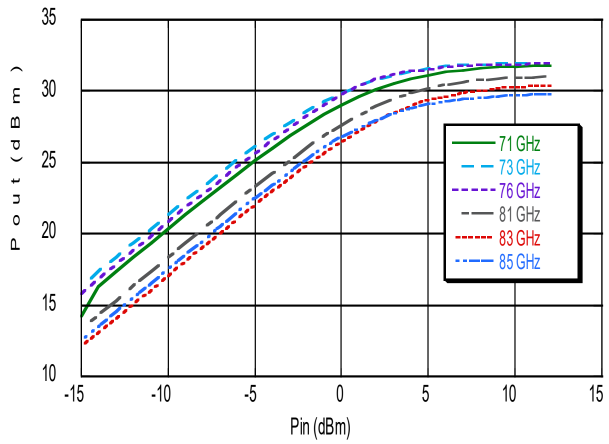
OIP3 vs. Frequency vs. Pout per tone



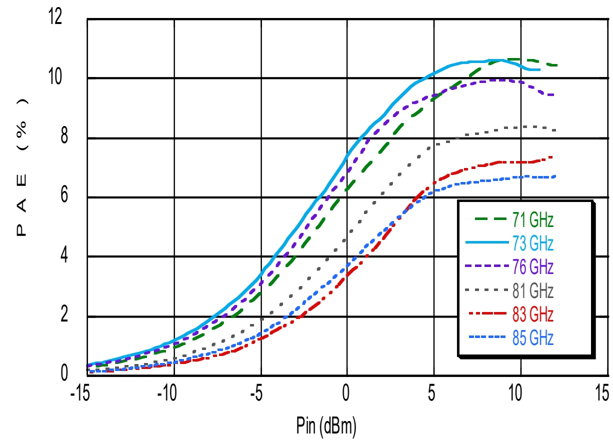
IM3 vs. Frequency vs. Pout per tone



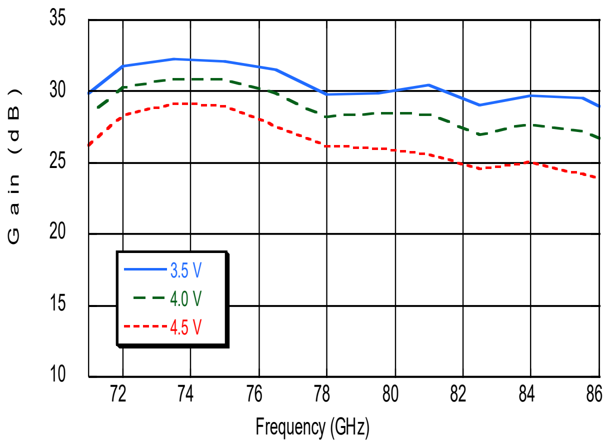
Pout vs. Pin @ 25C



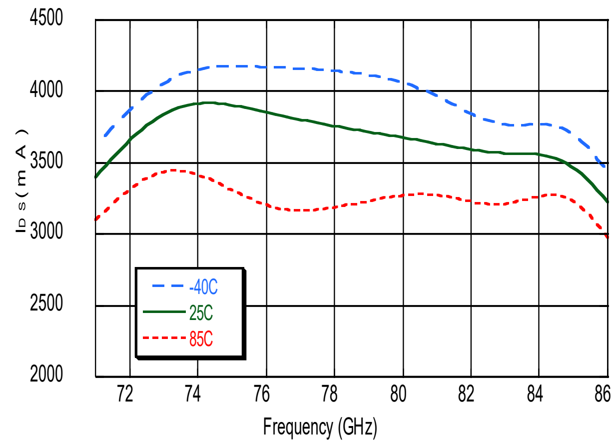
PAE vs. Pin @ 25C



Small Signal Gain vs. Frequency

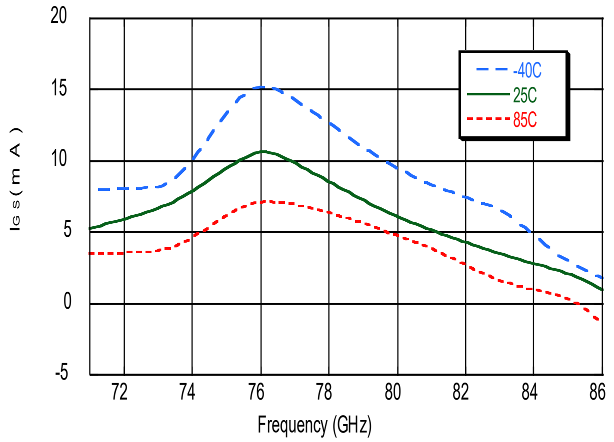


Ids vs. Frequency @ Psat

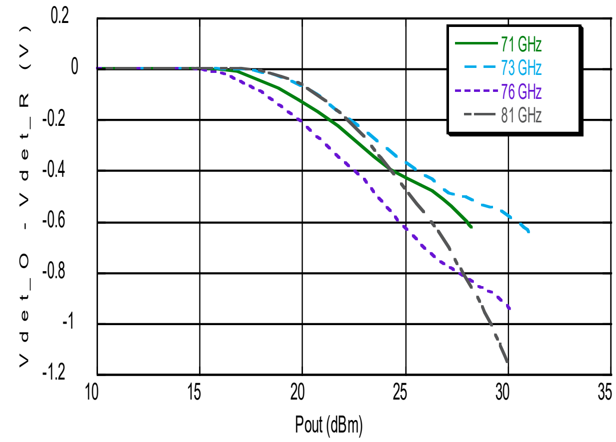


Typical Performance Curves: V_D = 4 V, I_{DSQ} = 2850 mA, T_A = +25°C, Probed On Wafer

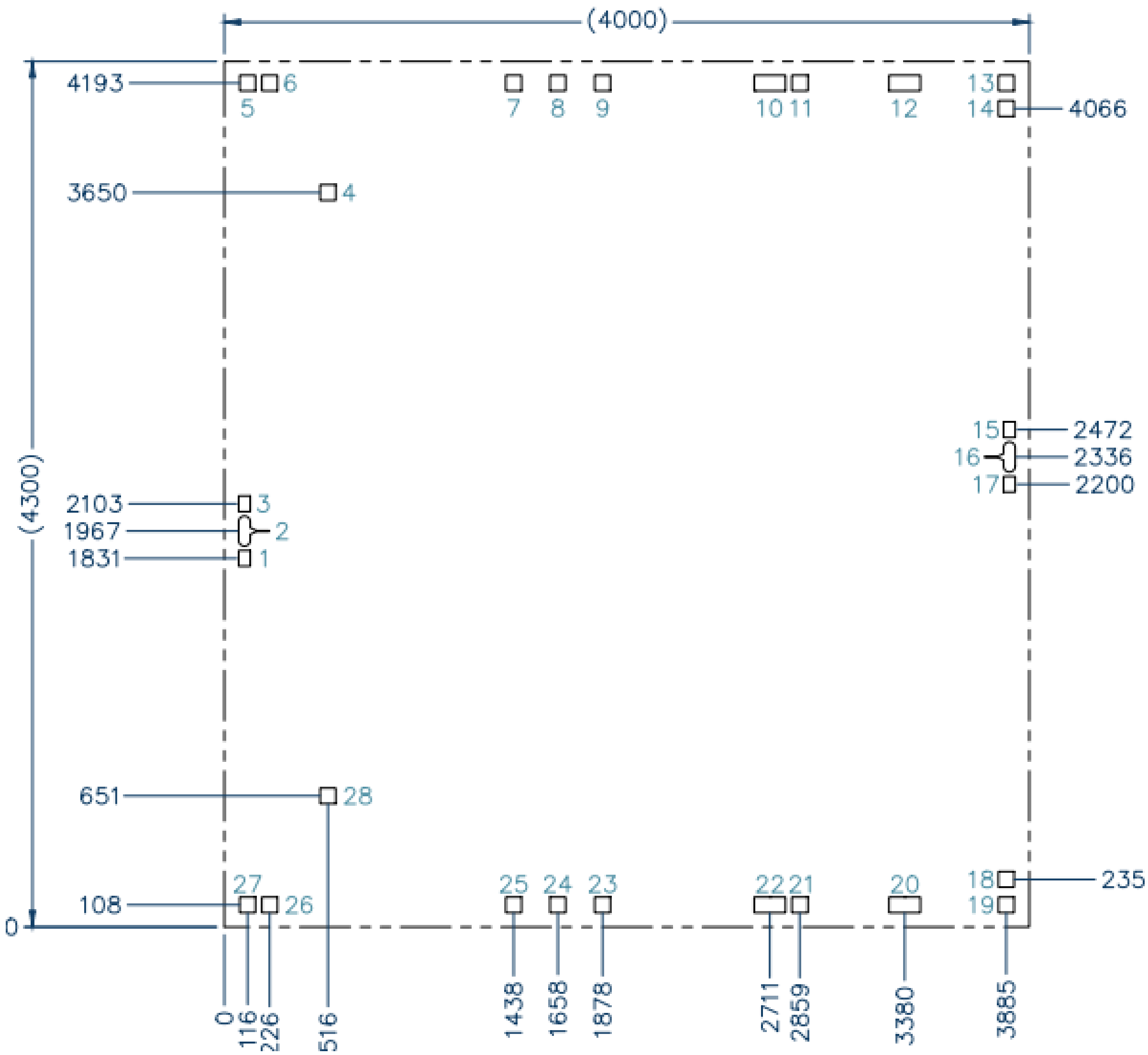
Igs vs. Frequency @ Psat



Detected Voltage vs. Pout @ 25C



MMIC Die Outline[12,13]



Bond Pad Detail (µm)

Pad	Size (x)	Size (y)
7,5,6,7,8,9,11,13,14,18,19,21,23,24,25,26,27,28	78	78
1,3,15,17	58	78
2,16	58	150
10,12,20,22	156	78

9. All units in mm, unless otherwise noted, with a tolerance of ±5 µm
10. Die thickness is 50 µm with a tolerance of ±5 µm
11. Bond pad / backside metallization: gold
12. Die size reflects final dimensions