Features

- High Gain: 22 dB
- P1dB: 29 dBm
- P_{SAT}: 30 dBm
- Output IP3: 39 dBm
- Bias Voltage: V_{DD} = 5 V
- Bias Current: I_{DSQ} = 1500 mA
- 50 Ω Matched Input / Output
- Temperature Compensated Output Power Detector
- Lead-Free 5 x 7 mm 12 lead SMT package
- RoHS* Compliant

Applications

- Test & Measurement
- 5G FR2, EW, ECM
- Radar

Description

The MAAP-011379 is a 1 W distributed power amplifier offered in die form. The power amplifier operates from 20 to 55 GHz and provides 22 dB of linear gain and 30 dBm saturated output power. The device is fully matched across the band and includes a temperature compensated output power detector.

The MAAP-011379 can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for test and measurement, 5G FR2, EW, ECM, and radar applications.

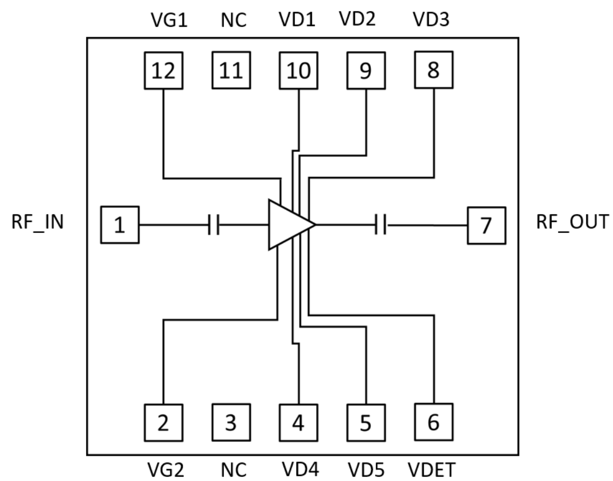
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information

Part Number	Package
MAAP-011379-TR0500	500 piece reel
MAAP-011379-SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3]

Pad #	Pad Name	Description
1	RF_{IN}	RF Input
2	V_{G2}	Gate Voltage 2
3,11	NC[4]	Not Internally Connected
4	V_{D4}	Drain Voltage 4
5	V_{D5}	Drain Voltage 5
6	V_{DET}	Power Detector
7	RF_{OUT}	RF Output
8	V_{D3}	Drain Voltage 3
9	V_{D2}	Drain Voltage 2
10	V_{D1}	Drain Voltage 1
12	V_{G1}	Gate Voltage 1

3. Ground paddle must be connected to RF, DC and thermal ground.
4. It is recommended that these pins are grounded on the application PCB.

AC Electrical Specifications: T_A = +25°C, V_D = 5 V, I_{DSQ} = 1500 mA, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = -10 dBm 20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dB	16.5 — — 17.0 —	19.5 19.5 22.5 21.0 20.0	—
Input Return loss	—	dB	—	15	—
Output Return Loss	—	dB	—	15	—
P1dB	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	24.5 — — 25.0 —	28.0 29.5 28.5 28.5 23.5	—
P_{SAT}	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	—	30.0 30.5 30.0 30.0 26.5	—
OIP3	P_{OUT}/Tone = 21 dBm, Δf = 2 MHz	dBm	—	38.5	—
Drain Current	P_{SAT}, 40 GHz	mA	—	1950	—
Power Added Efficiency	P_{SAT}, 40 GHz	%	—	9	—

Maximum Operating Ratings

Parameter	Rating
Input Power	16 dBm
Drain Voltage	5.5 V
Junction Temperature[5,6]	+160°C
Operating Temperature	-40°C to +85°C

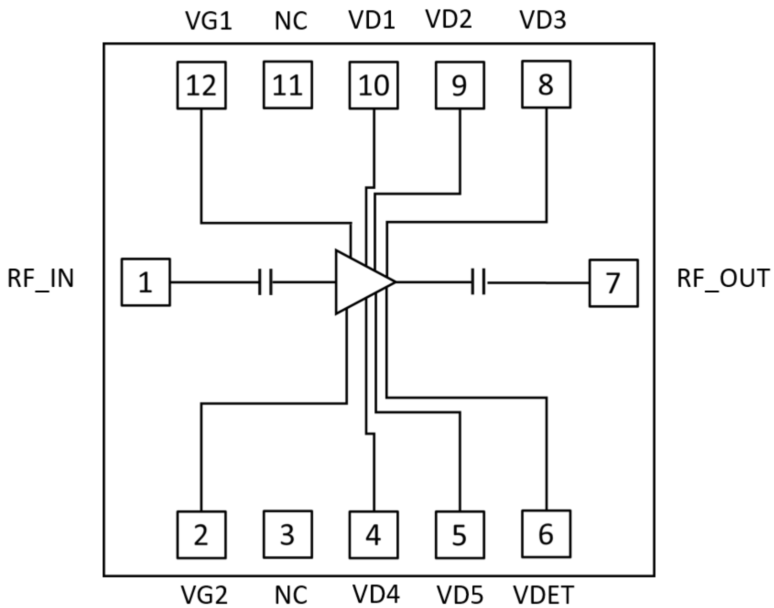
5. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > 1 x 10^6 hours.
6. Junction Temperature (T_J) = T_C + $Θ_{JC}$ * [(V * I) - (P_{OUT} - P_{IN})]. Typical thermal resistance ($Θ_{JC}$) = 5.6°C/W
   a) For T_C = +25°C at the backside of the die
      T_J = 74°C @ 5 V, 1.95 A,
      P_{OUT} = 30 dBm, P_{IN} = 15 dBm
   b) For T_C = +85°C at the backside of the die
      T_J = 134°C @ 5 V, 1.9 A,
      P_{OUT} = 29 dBm, P_{IN} = 15 dBm

Absolute Maximum Ratings[7,8]

Parameter	Absolute Maximum
Input Power	27 dBm
Drain Voltage	6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature[9]	+175°C
Storage Temperature	-65°C to +125°C

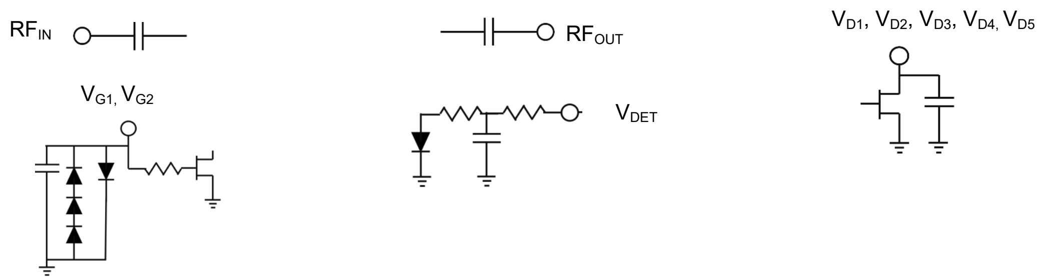
7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1	RF_{IN}	RF Signal Input. This pin is matched to 50 Ω and is AC coupled.
2,12	V_{G1},V_{G2}	Power amplifier gate controls. Adjust from –2 V to 0 V to achieve the desired quiescent current. External bypass capacitors are required as described in the applications schematic. There is no internal connection between pin 2 & 12 and so both need to be externally connected to the gate voltage.
3,11	NC	These pins are not internally connected (i.e. open circuit). It is recommended that these are connected to ground on the application PCB.
4	V_{D4}	Drain bias 4 for the amplifier. External bypass capacitors are required as described in the applications schematic.
5	V_{D5}	Drain bias 5 for the amplifier. External bypass capacitors are required as described in the applications schematic.
6	V_{DET}	Power detector output voltage. There is an internal 5kΩ resistor on this pin.
7	RF_{OUT}	RF Signal Output. This pin is matched to 50 Ω and is AC coupled
8	V_{D3}	Drain bias 3 for the amplifier. External bypass capacitors are required as described in the applications schematic.
9	V_{D2}	Drain bias 2 for the amplifier. External bypass capacitors are required as described in the applications schematic.
10	V_{D1}	Drain bias 1 for the amplifier. External bypass capacitors are required as described in the applications schematic.

Interface Schematics



Biasing Conditions

Recommended biasing conditions are V_D = 5 V, I_{DQ} = 1500 mA (controlled with V_G). The drain bias voltage range is 4 to 5.5 V, and the quiescent drain current biasing range is 1300 to 1700 mA.

Operating the MAAP-011379

Turn-on

1. Apply V_G (-2 V).
2. Apply V_D (5 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically -0.45 V for I_{DQ} = 1500 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -2 V.
3. Decrease V_D to 0 V.

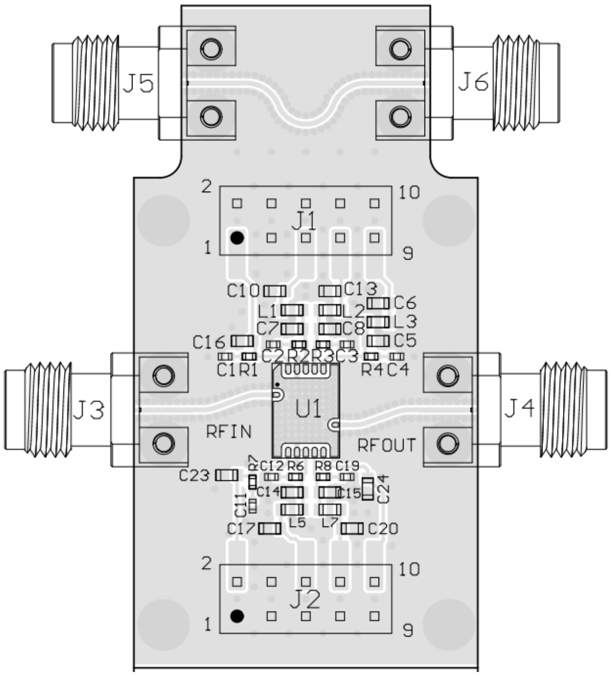
Handling Procedures

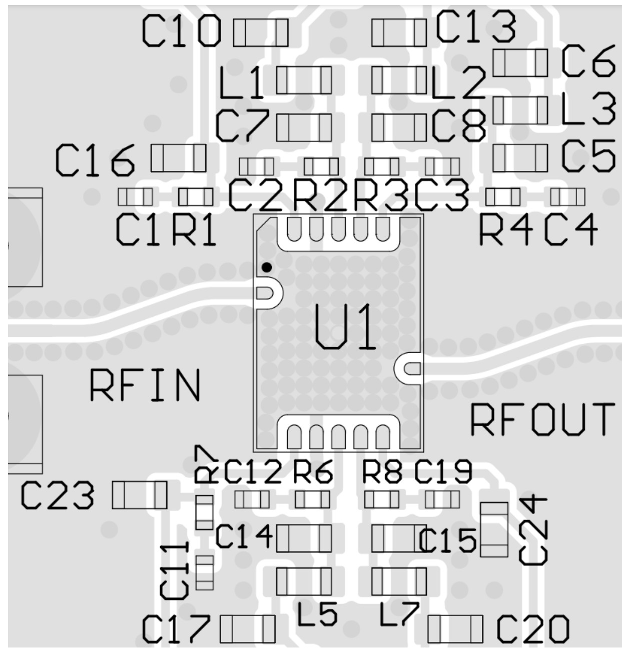
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Evaluation Board Layout





DESIGN NOTES:
RO4003C, 8 MIL THICK, 1/2 COPPER, SOFT GOLD PLATING
RF TRACE: 14 MIL WIDTH AND 6.5 MIL SPACING
RF PROBE: 8 MIL TRACE WIDTH, 4.5 MIL SPACING
EDGE WRAP ON J3, J4, J5, J6.

Parts List

Part	Value	Case Style
C6, C10, C13, C17, C20	1 µF	603
C5, C7, C8, C14, C15, C16, C23, C24	0.1 µF	603
C1, C2, C3, C4, C11, C12, C19	100 pF	402
R1, R2, R3, R4, R6, R7, R8	10 Ω	402
L1, L2, L3, L5, L7	10 nH	603
C9, C18, C21, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C36, C37, C38, C39, C40, C41 R5, R9, R10, R11, R12, R13, R14 L 4, L6, L8, L9, L10	DNI	DNI

Evaluation Board Notes

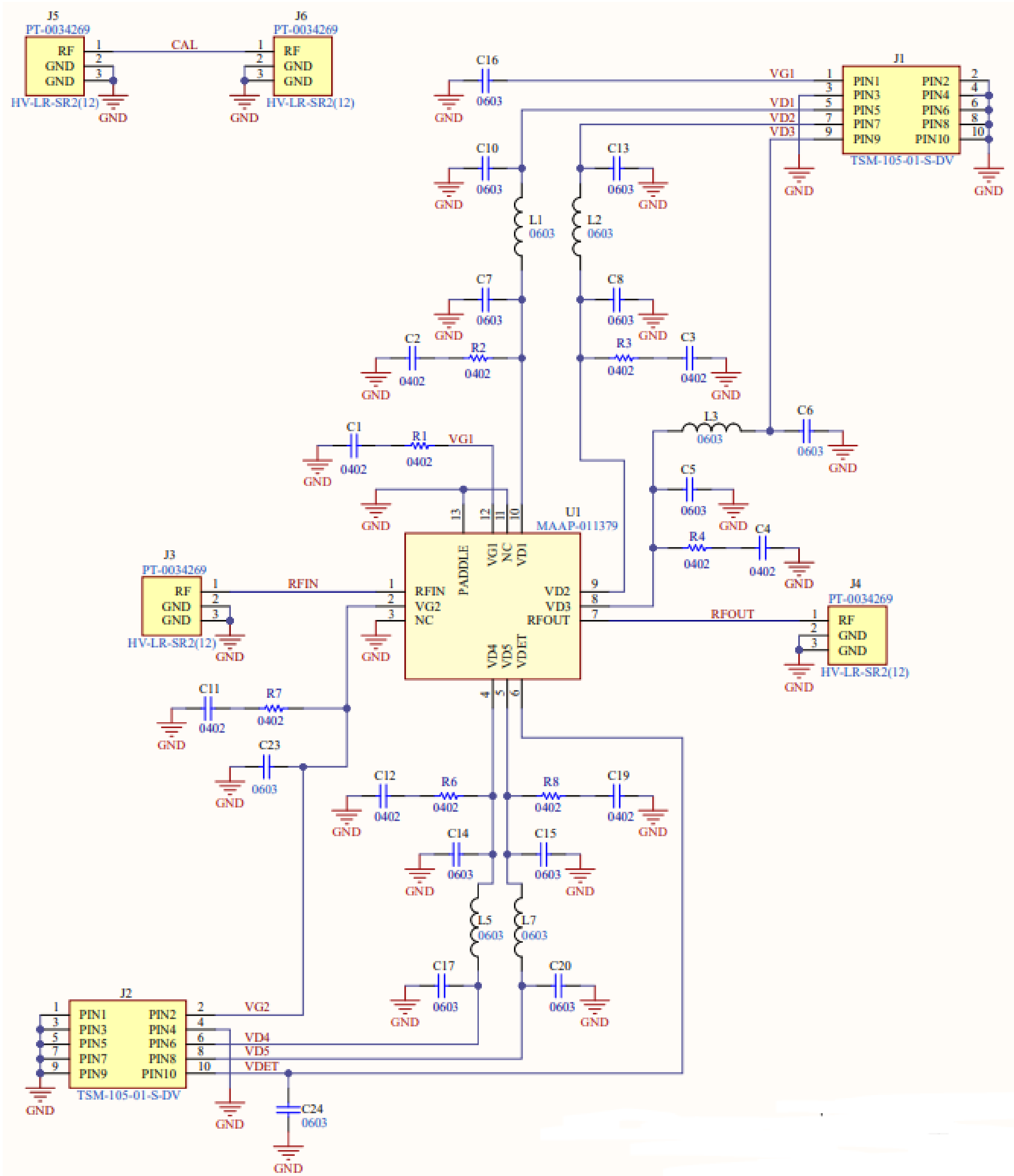
The 100 pF capacitors should be placed as close to the amplifier as practically possible. For the larger 0.1 µF capacitors proximity to the PA is less important. The circuit is not sensitive to the positioning of the 1.0 µF capacitors however these should be on the same PCB as the rest of the biasing components.

The capacitors on the detector output are optional: values will depend on the required response time of the detector output. There is an internal series 5 kΩ resistor on this pin.

To ensure proper grounding the number of ground vias under the device should be maximized (within practical limits imposed by the PCB vendor).

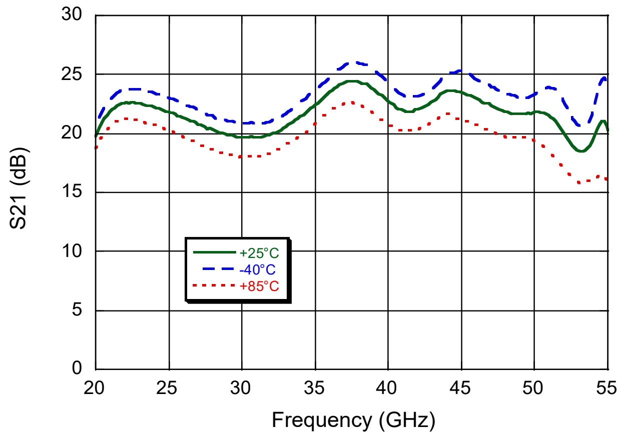
Due to the relatively high power dissipation of this high performance power amplifier, consideration needs to be given to the thermal design of the PCB. MACOM recommends the use of fully copper plated thermal vias beneath the amplifier.

Evaluation Board Schematic

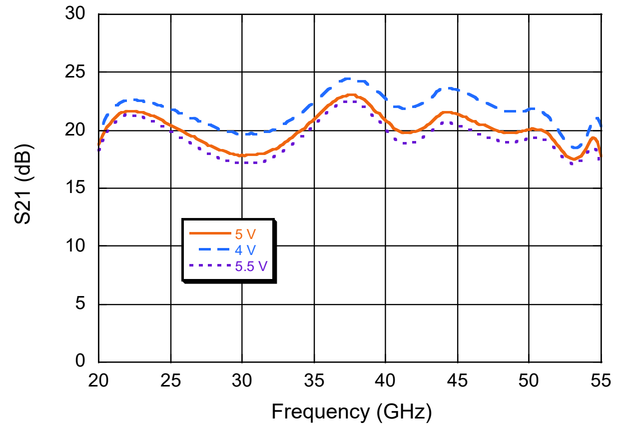


Typical Performance Curves: V_D = 5 V, I_{DSQ} = 1500 mA

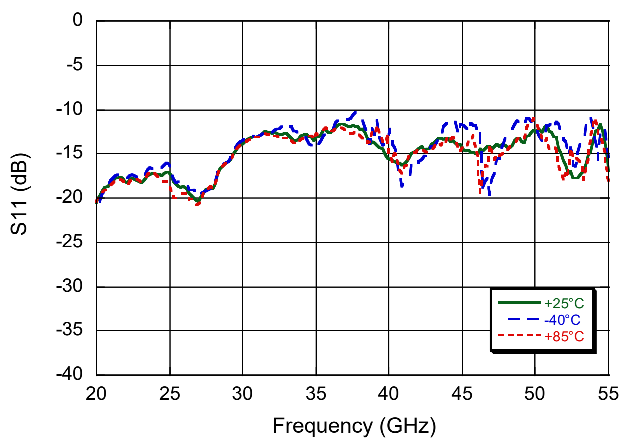
Small Signal Gain vs. Frequency



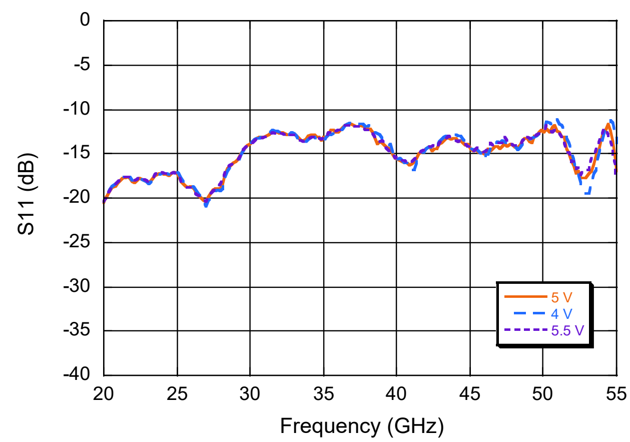
Small Signal Gain vs. Frequency



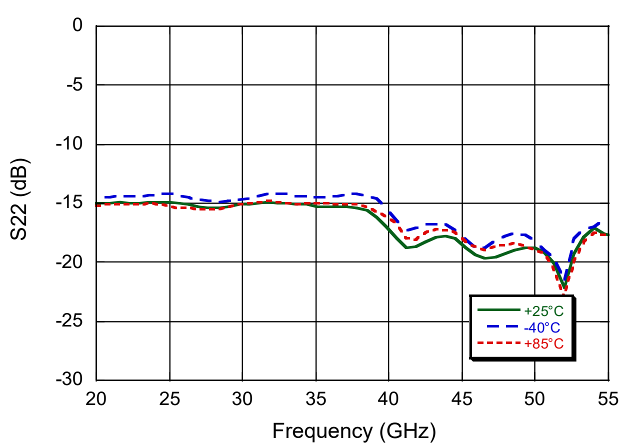
Input Return Loss vs. Frequency



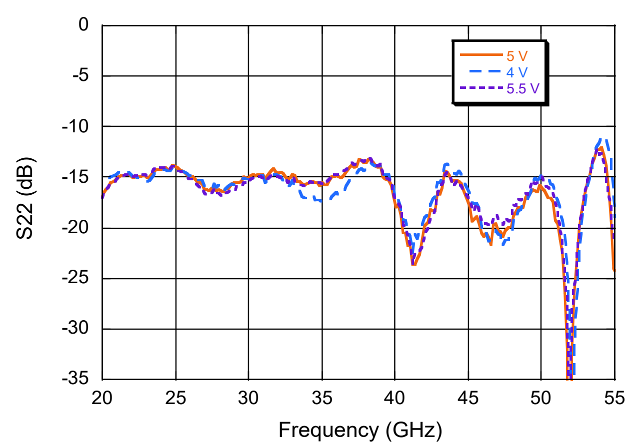
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

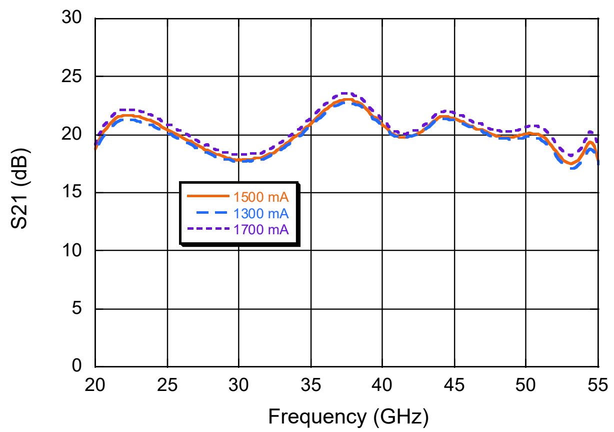


Output Return Loss vs. Frequency

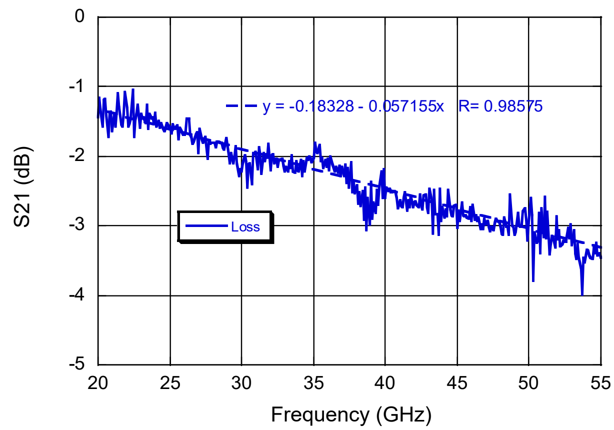


Typical Performance Curves: V_D = 5 V

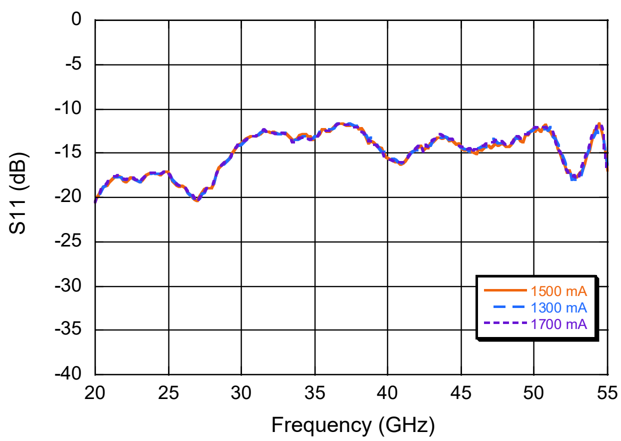
Small Signal Gain vs. Frequency



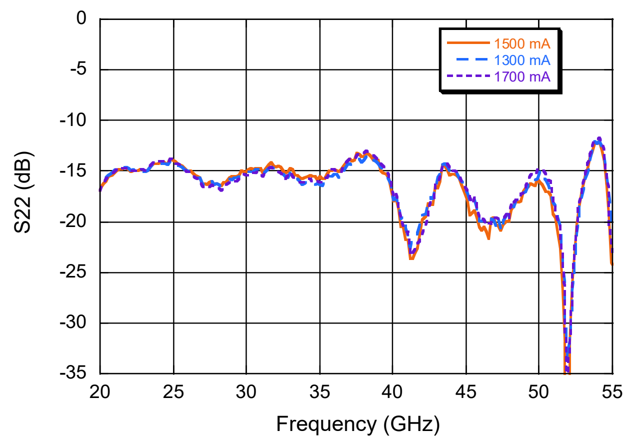
Eval Board Thru Losses



Input Return Loss vs. Frequency

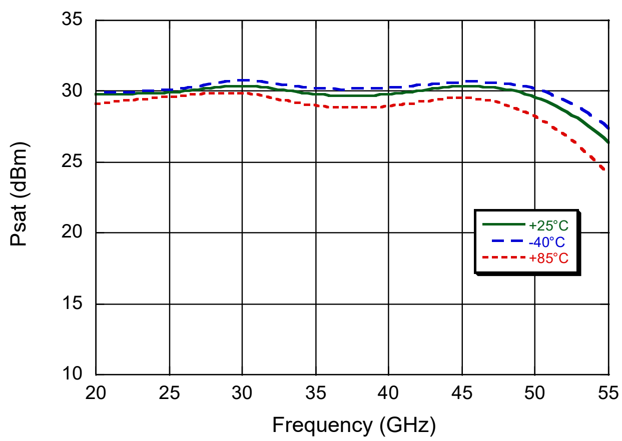


Output Return Loss vs. Frequency

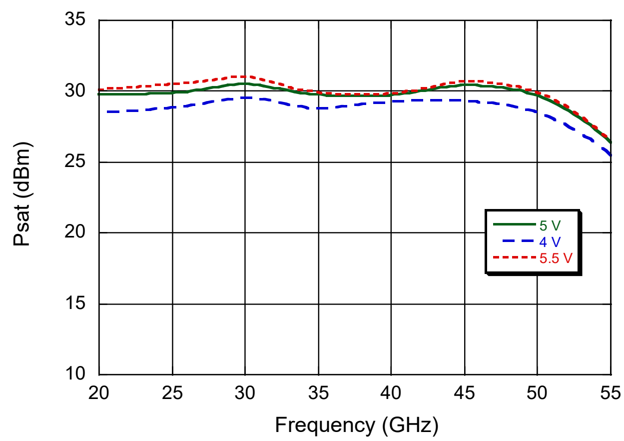


Typical Performance Curves: V_D = 5 V, I_{DSQ} = 1500 mA

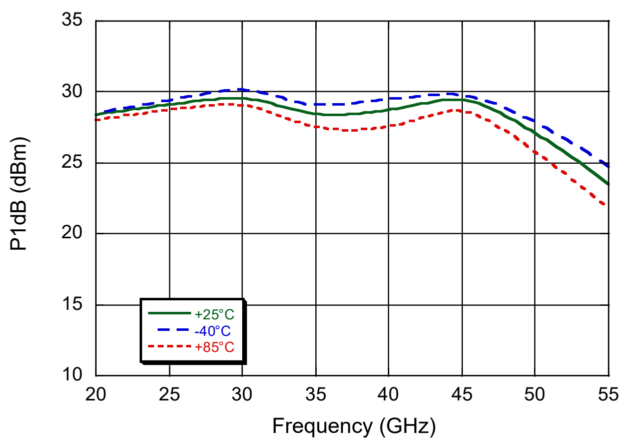
Psat vs. Frequency



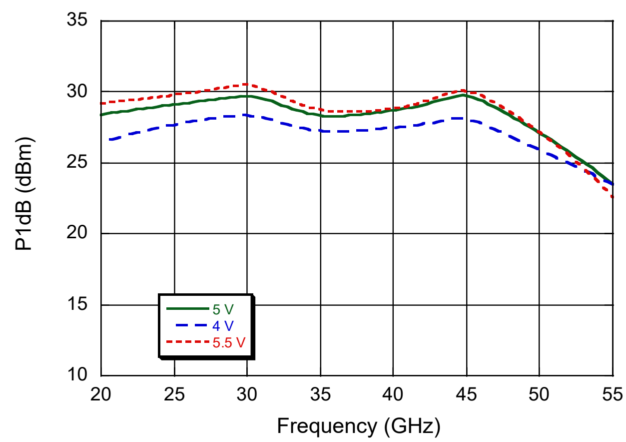
Psat vs. Frequency



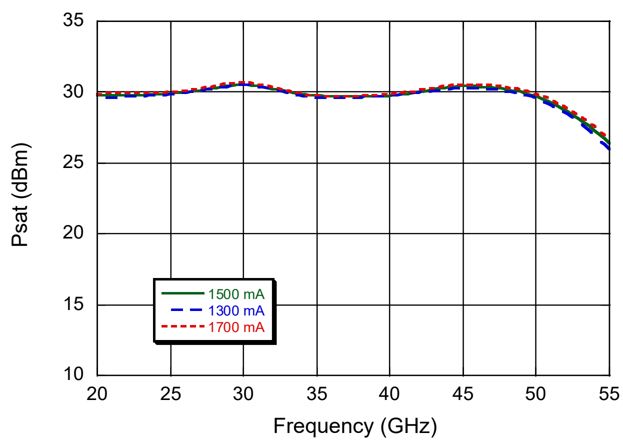
P1dB vs. Frequency



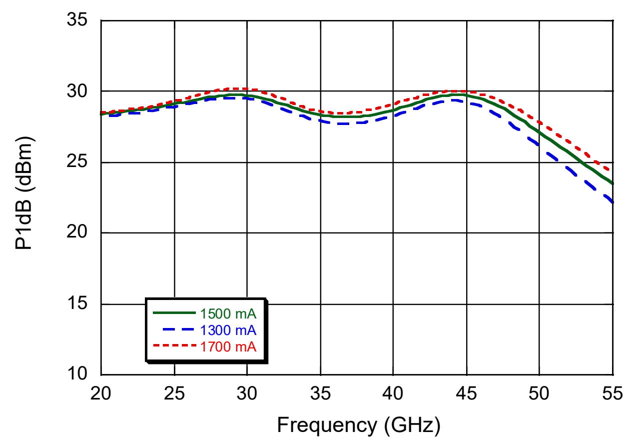
P1dB vs. Frequency



Psat vs. Frequency

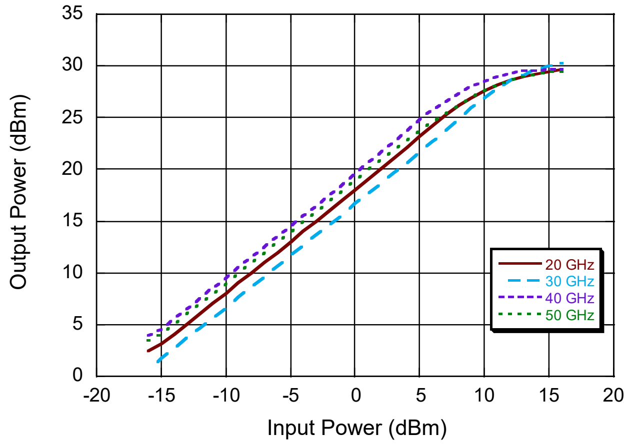


P1dB vs. Frequency

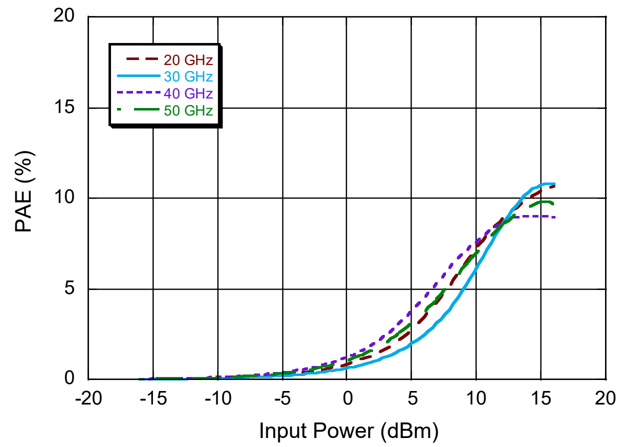


Typical Performance Curves: V_D = 5 V, I_{DSQ} = 1500 mA

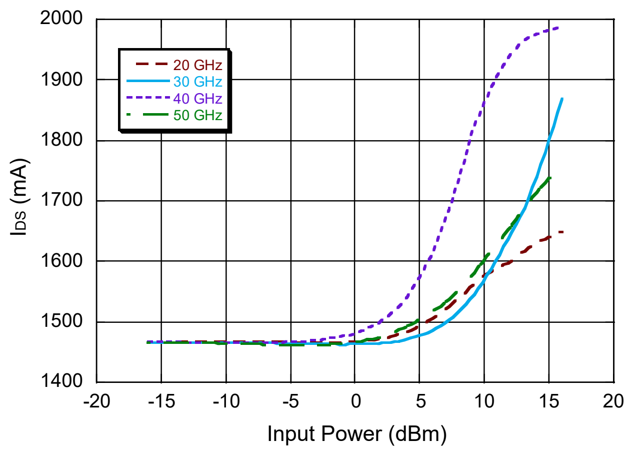
Output Power vs. Input Power



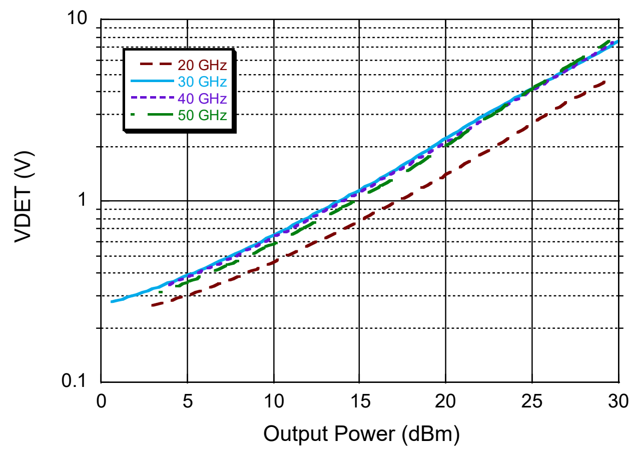
PAE vs. Input Power



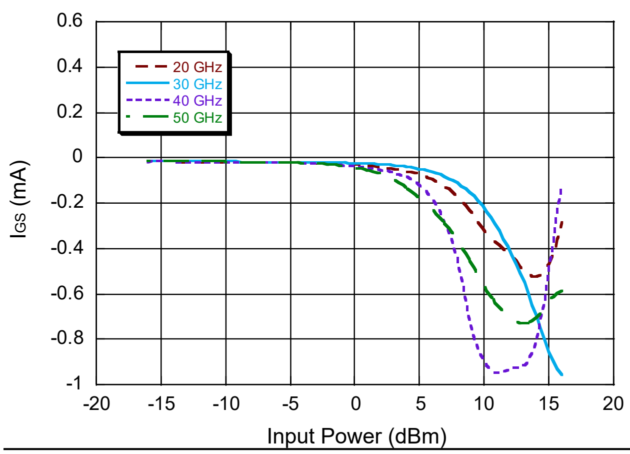
Drain Current vs. Input Power



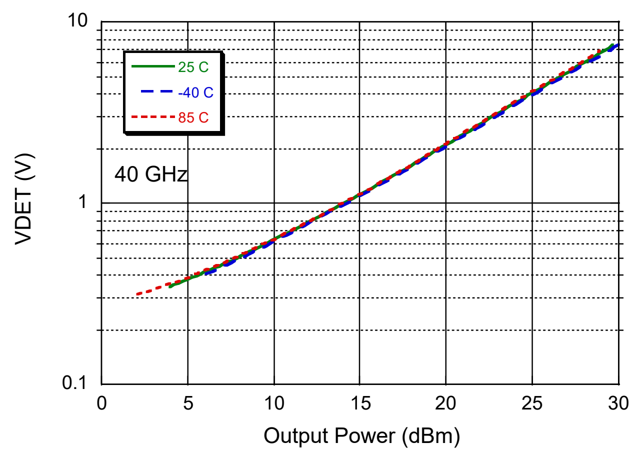
Detector Voltage vs. Output Power



Gate Current vs. Input Power

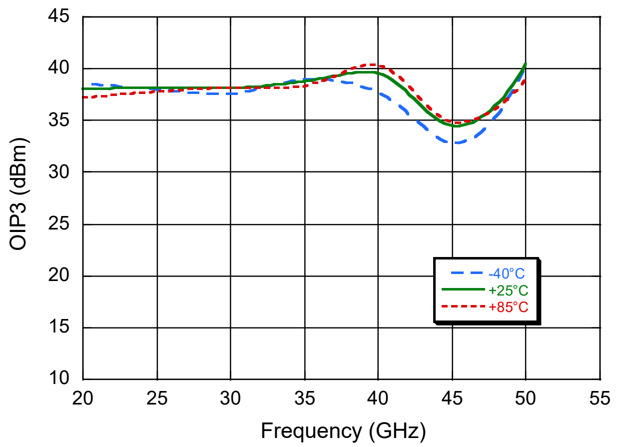


Detector Voltage vs. Output Power and Temperature

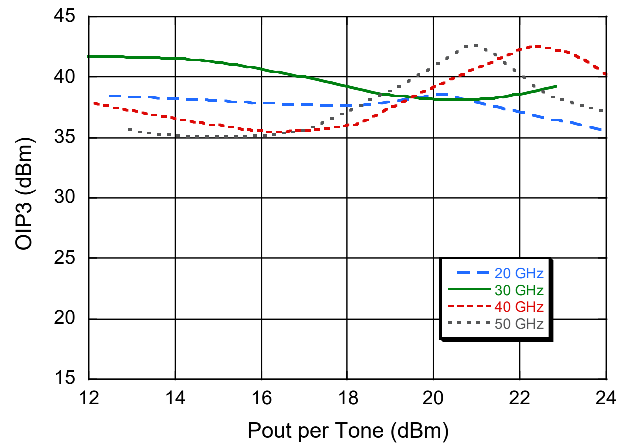


Typical Performance Curves: V_D = 5 V, I_{DSQ} = 1500 mA

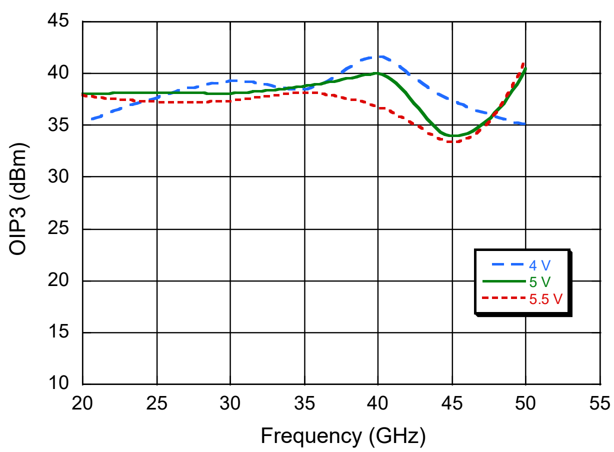
Output IP3 vs. Frequency @ Pout = 21 dBm / Tone



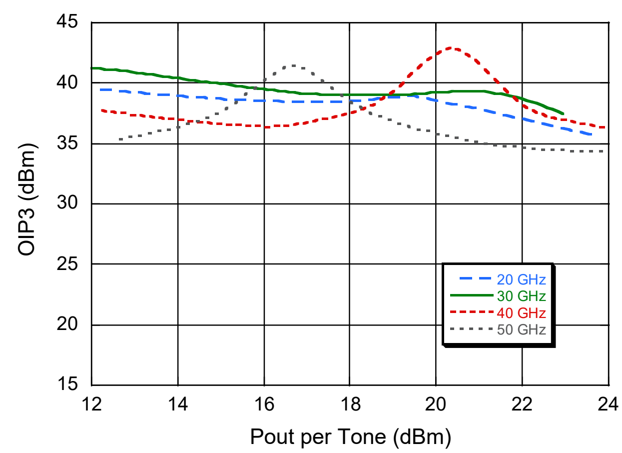
Output IP3 vs. Frequency and Pout per Tone Vd = 5 V



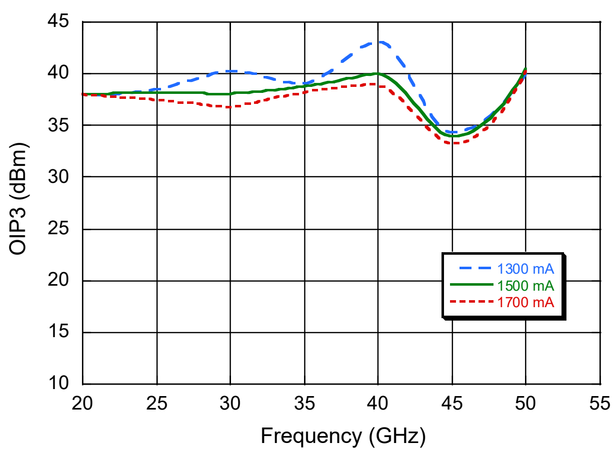
Output IP3 vs. Frequency @ Pout = 21 dBm / Tone



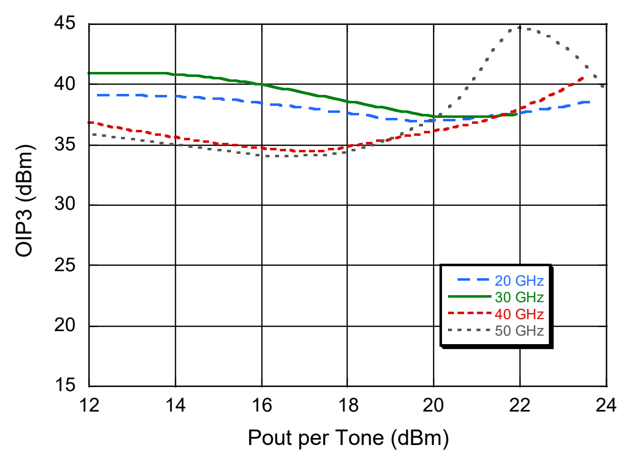
Output IP3 vs. Frequency and Pout per Tone Vd = 4 V



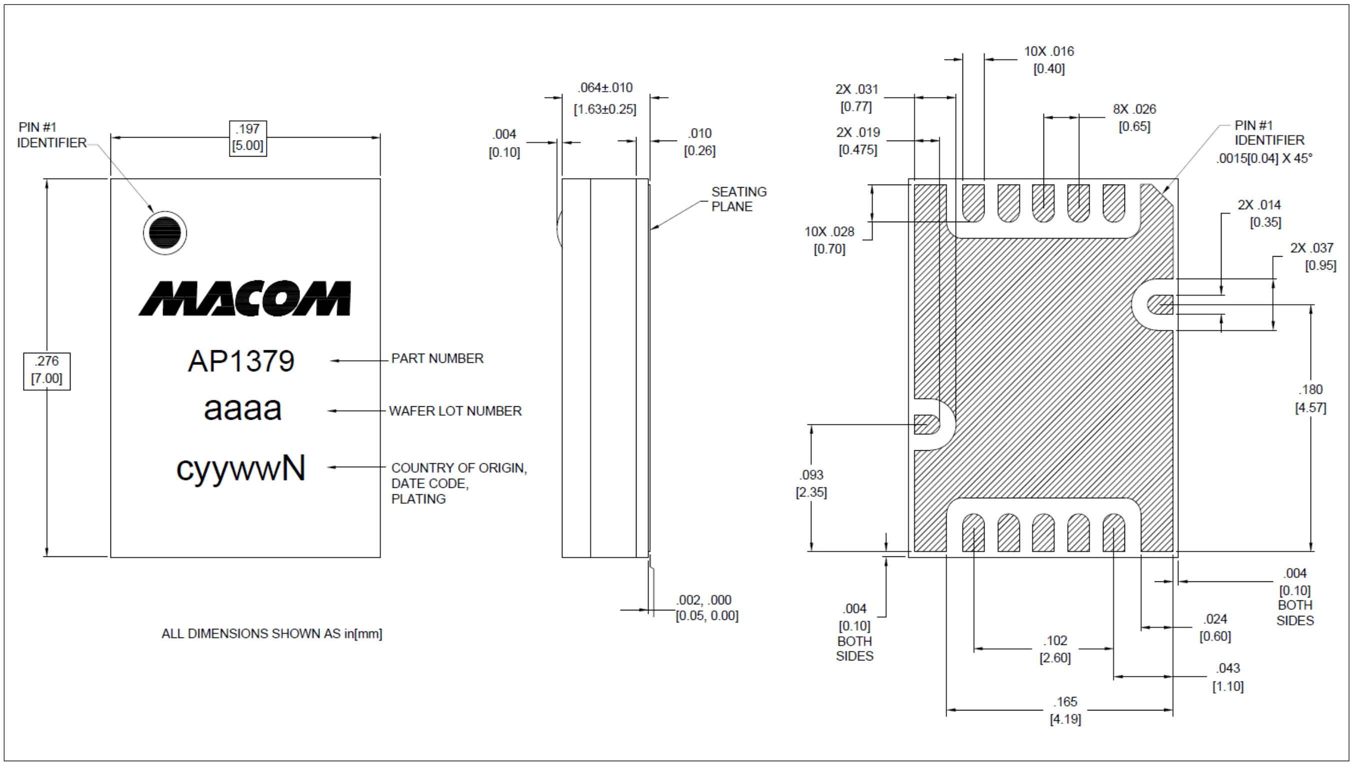
Output IP3 vs. Frequency @ Pout = 21 dBm / Tone



Output IP3 vs. Frequency and Pout per Tone Vd = 5.5 V



Lead-Free 5 mm x 7 mm 12-Lead SMT [10,11,12,13,14]



10. All units in in(mm), unless otherwise noted, with a tolerance of .xxxx = ±.0005 in and .xxx = ±.005 in.
11. Lead finish: NiPdAu plating
12. Marking: line 2 part number; line 3 wafer lot number; line 4 c = country of origin, yyww = date code, N = Nickel/Palladium/Gold plating
13. Reference Application Note S2083 for lead-free solder reflow recommendations.
14. Meets JEDEC moisture sensitivity level 3 requirements.