

Power Amplifier, 1 W 20 - 55 GHz



MAAP-011379-DIE

Rev. V2

Features

- High Gain: 22 dB
- P1dB: 28 dBm
- P_{SAT}: 30 dBm
- Output IP3: 37 dBm
- Bias Voltage: V_{DD} = 5 V
- Bias Current: I_{DSQ} = 1500 mA
- 50 Ω Matched Input / Output
- Temperature Compensated Output Power Detector
- Die Size: 2900 x 3500 x 100 μm
- RoHS* Compliant

Applications

- Test & Measurement
- 5G FR2, EW, ECM
- Radar

Description

The MAAP-011379-DIE is a 1 W distributed power amplifier offered in die form. The power amplifier operates from 20 to 55 GHz and provides 22 dB of linear gain and 30 dBm saturated output power. The device is fully matched across the band and includes a temperature compensated output power detector.

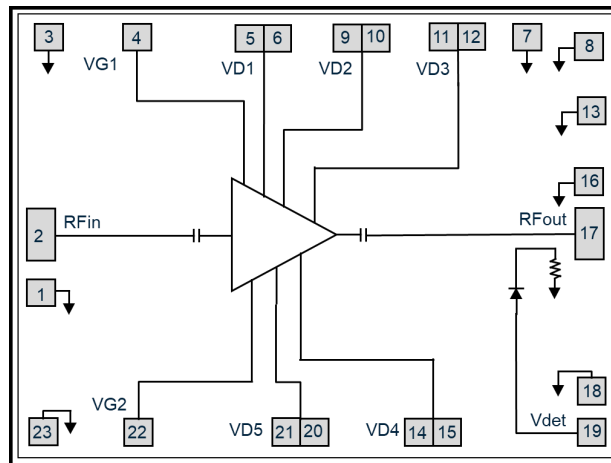
The MAAP-011379-DIE can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for test and measurement, 5G FR2, EW, ECM, and radar applications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information

Part Number	Package
MAAP-011379-DIE	Bare Die

Functional Schematic



Bond Pad Configuration¹

Pad #	Pad Name	Description
1,3,7,8,13,16,18,23	GND	Ground
2	RFIN	RF Input
4, 22	VG1, VG2	Gate Voltages
5,6	VD1	Drain Voltage 1
9,10	VD2	Drain Voltage 2
11,12	VD3	Drain Voltage 3
14,15	VD4	Drain Voltage 4
20,21	VD5	Drain Voltage 5
17	RFOUT	RF Output
19	V _{DET}	Power Detector

1. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

AC Electrical Specifications: $T_A = +25^\circ\text{C}$, $V_D = 5\text{ V}$, $I_{DSQ} = 1500\text{ mA}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	$P_{IN} = -10\text{ dBm}$ 20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dB	16.0 — 17.0 17.0 —	20.0 20.0 22.5 22.0 20.0	—
Input Return loss	—	dB	—	15	—
Output Return Loss	—	dB	—	15	—
P1dB	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	— — — 25.5 —	28.0 30.0 29.0 27.5 24.0	—
P_{SAT}	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	—	30.0 30.5 30.0 29.0 26.0	—
OIP3	$P_{OUT}/\text{Tone} = 20\text{ dBm}$, $\Delta f = 2\text{ MHz}$	dBm	—	37	—
Drain Current	P_{SAT} , 40 GHz	mA	—	1950	—
Power Added Efficiency	P_{SAT} , 40 GHz	%	—	10	—

Maximum Operating Ratings

Parameter	Rating
Input Power	16 dBm
Drain Voltage	5.5 V
Junction Temperature ^{2,3}	+160°C
Operating Temperature	-40°C to +85°C

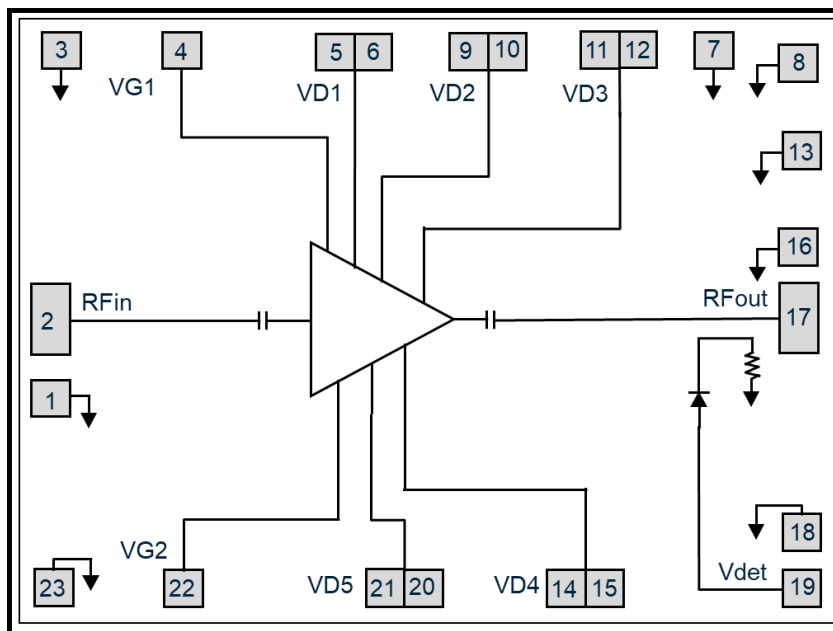
- Operating at nominal conditions with junction temperature $\leq +160^\circ\text{C}$ will ensure MTTF $> 1 \times 10^6$ hours.
- Junction Temperature (T_J) = $T_C + \Theta_{JC} * [(V * I) - (P_{OUT} - P_{IN})]$.
Typical thermal resistance (Θ_{JC}) = 5.6°C/W
 - For $T_C = +25^\circ\text{C}$ at the backside of the die
 $T_J = 74^\circ\text{C}$ @ 5 V, 1.95 A,
 $P_{OUT} = 30\text{ dBm}$, $P_{IN} = 15\text{ dBm}$
 - For $T_C = +85^\circ\text{C}$ at the backside of the die
 $T_J = 134^\circ\text{C}$ @ 5 V, 1.9 A,
 $P_{OUT} = 29\text{ dBm}$, $P_{IN} = 15\text{ dBm}$

Absolute Maximum Ratings^{4,5}

Parameter	Absolute Maximum
Input Power	27 dBm
Drain Voltage	6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature ⁶	+175°C
Storage Temperature	-65°C to +125°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Pin Configuration and Functional Descriptions



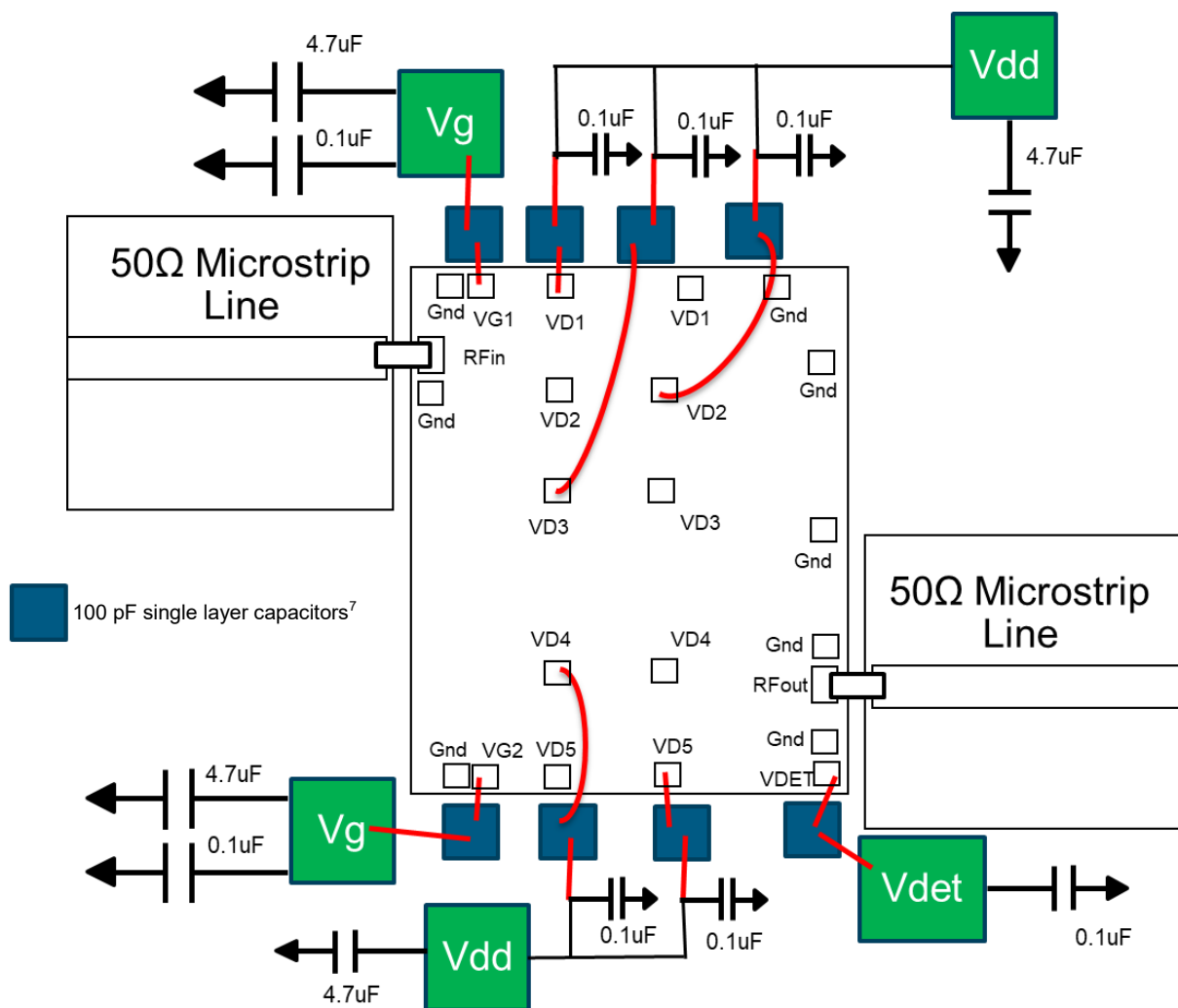
Pin #	Pin Name	Description
1,3,7,8,13,16,18,23	GND	These pads are grounded on the MMIC.
2	RF _{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
4,22	V _{G1} , V _{G2}	Power amplifier gate controls. Adjust from -2 V to 0 V to achieve the desired quiescent current. External bypass capacitors are required as described in the applications schematic. There is no internal connection between pads 4 & 22 and so both need to be externally connected to the gate voltage.
5,6	V _{D1}	Drain bias 1 for the amplifier. External bypass capacitors are required as described in the applications schematic. There is an internal connection between pads 5 and 6 and so only one of the pins need to be externally connected to the drain supply.
9,10	V _{D2}	Drain bias 2 for the amplifier. External bypass capacitors are required as described in the applications schematic. There is an internal connection between pads 9 and 10 and so only one of the pins need to be externally connected to the drain supply.
11,12	V _{D3}	Drain bias 3 for the amplifier. External bypass capacitors are required as described in the applications schematic. There is an internal connection between pads 11 and 12 and so only one of the pins need to be externally connected to the drain supply.
17	RF _{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled
14,15	V _{D4}	Drain bias 4 for the amplifier. External bypass capacitors are required as described in the applications schematic. There is an internal connection between pads 14 and 15 and so only one of the pins need to be externally connected to the drain supply.
19	V _{DET}	Power detector output voltage. There is an internal 5kΩ resistor on this pin.
20,21	V _{D5}	Drain bias 5 for the amplifier. External bypass capacitors are required as described in the applications schematic. There is an internal connection between pads 10 and 11 and so only one of the pins need to be externally connected to the drain supply.

Recommended Bonding Diagram and Application Details:

For optimum performance, RF input and output transmission lines require either 3 mil gold ribbon (wedge bond) or 3 x 1 mil diameter gold wire bonds. The gap between the MMIC and the RF input and output lines should be a nominal 3 mil.

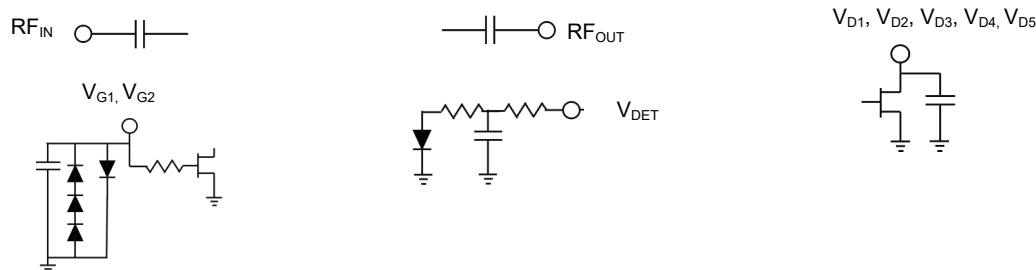
In the configuration shown below 100 pF chip capacitors are used as part of the drain supply bypassing network. These chip capacitors are to be placed as close to the die as practically possible. The larger 0.1 μ F capacitor could be implemented using an SMT component on a PCB instead of a chip cap: in this case, proximity to the MMIC die is less important. The circuit is not sensitive to the positioning of the 4.7 μ F capacitors however these should be on the same PCB as the rest of the biasing components.

The capacitors on the detector output are optional: values will depend on the required response time of the detector output. There is an internal series 5 k Ω resistor on this pin.



7. For the 100 pF single layer capacitors use MACOM MKVC-050100-1453.

Interface Schematics



Biasing Conditions

Recommended biasing conditions are $V_D = 5\text{ V}$, $I_{DQ} = 1500\text{ mA}$ (controlled with V_G). The drain bias voltage range is 4 to 5.5 V, and the quiescent drain current biasing range is 1300 to 1700 mA.

Operating the MAAP-011379-DIE

Turn-on

1. Apply V_G (-2 V).
2. Apply V_D (5 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically -0.45 V for $I_{DQ} = 1500\text{ mA}$).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -2 V.
3. Decrease V_D to 0 V.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

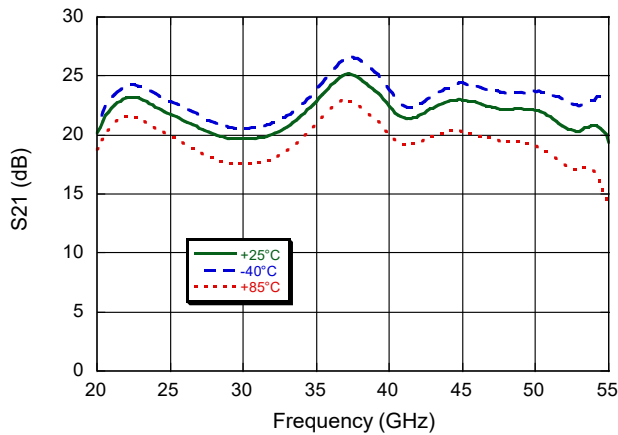
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Handling the Die

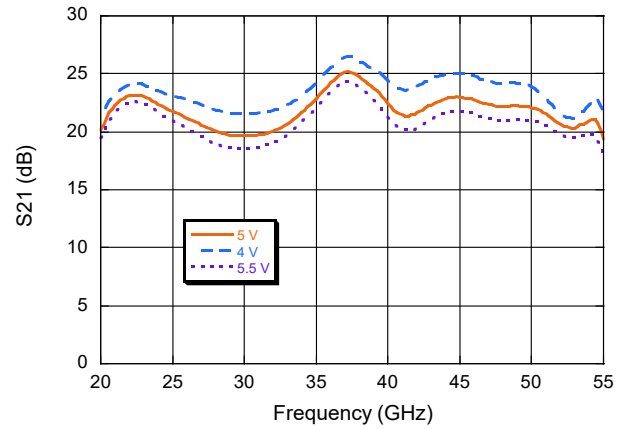
This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DSQ} = 1500\text{ mA}$

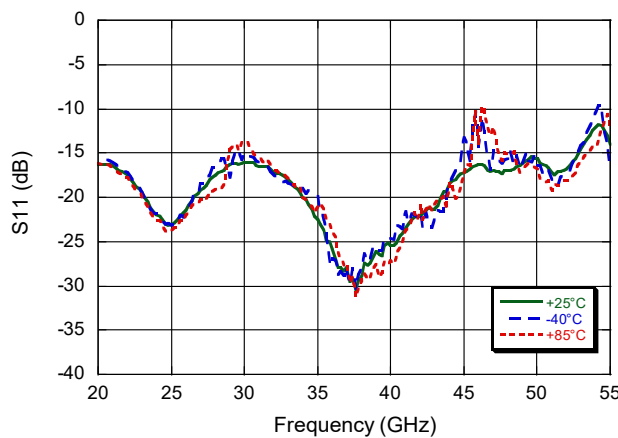
Small Signal Gain vs. Frequency



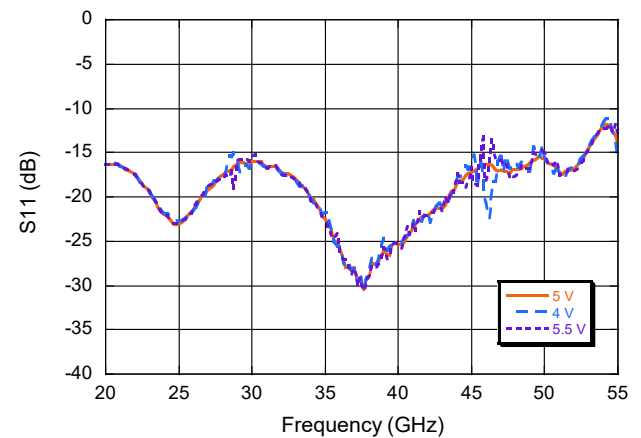
Small Signal Gain vs. Frequency



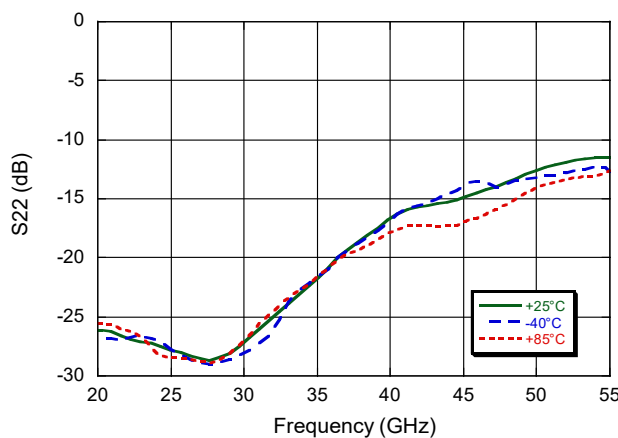
Input Return Loss vs. Frequency



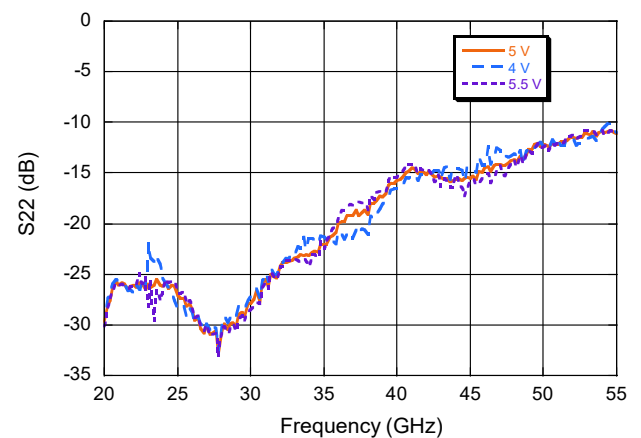
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

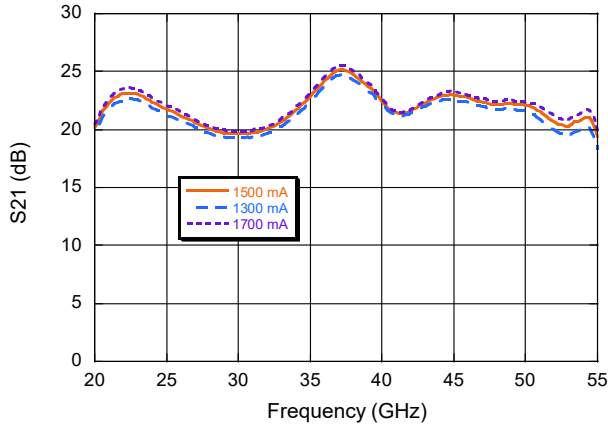


Output Return Loss vs. Frequency

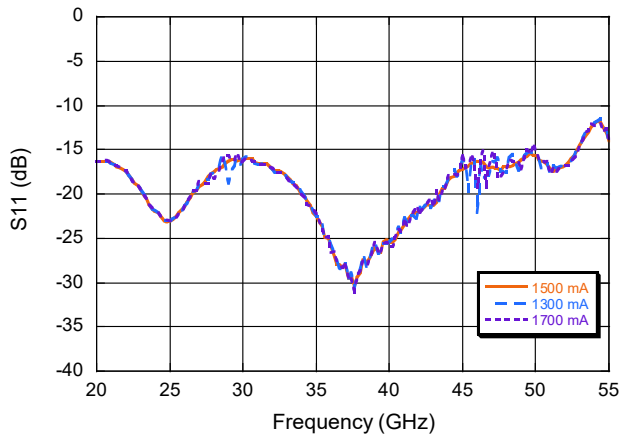


Typical Performance Curves: $V_D = 5\text{ V}$

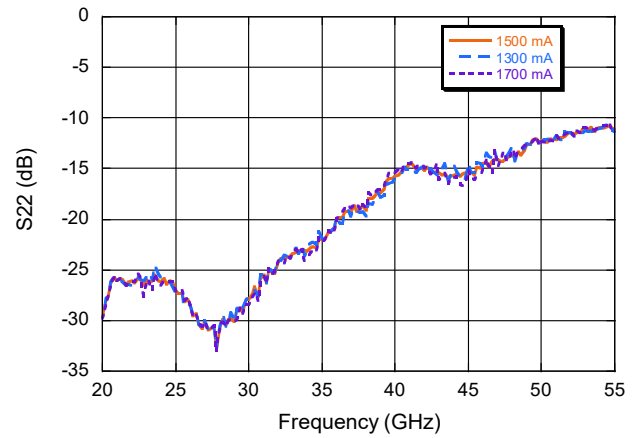
Small Signal Gain vs. Frequency



Input Return Loss vs. Frequency

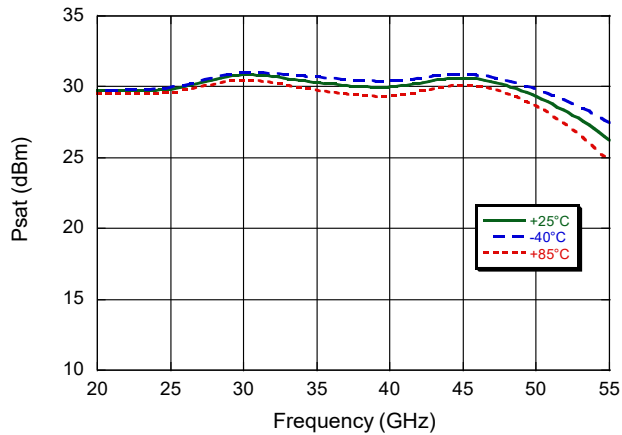


Output Return Loss vs. Frequency

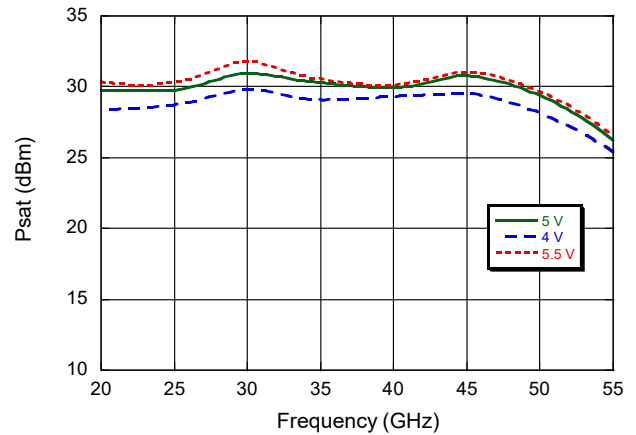


Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DSQ} = 1500\text{ mA}$

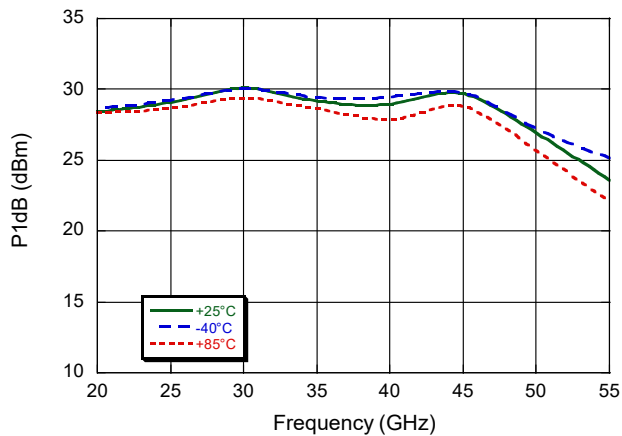
***P_{sat}* vs. Frequency**



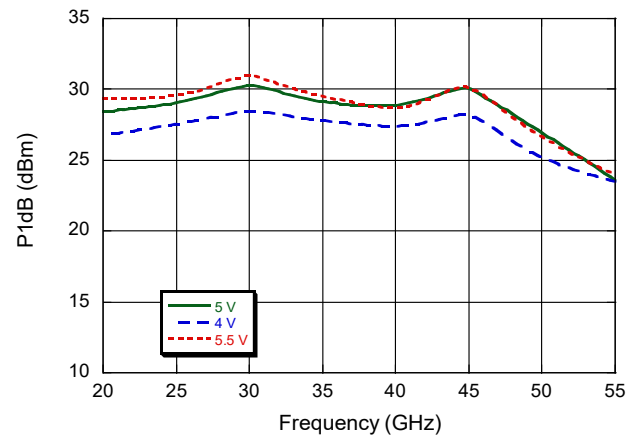
***P_{sat}* vs. Frequency**



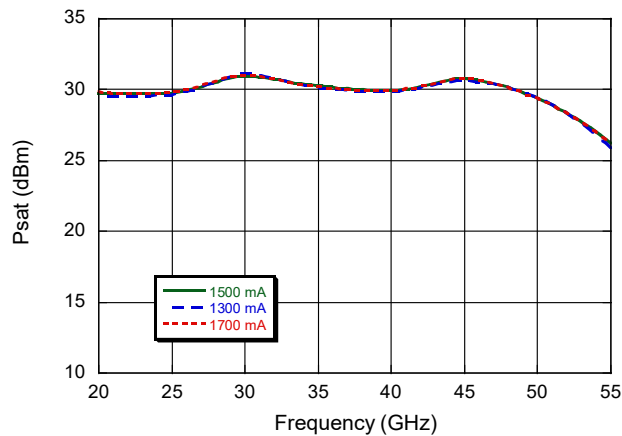
***P_{1dB}* vs. Frequency**



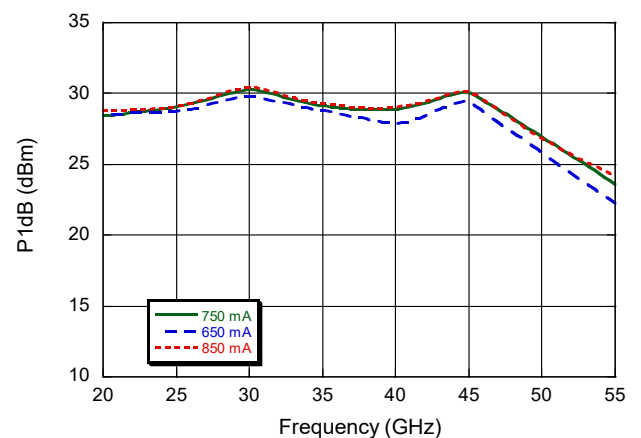
***P_{1dB}* vs. Frequency**



***P_{sat}* vs. Frequency**

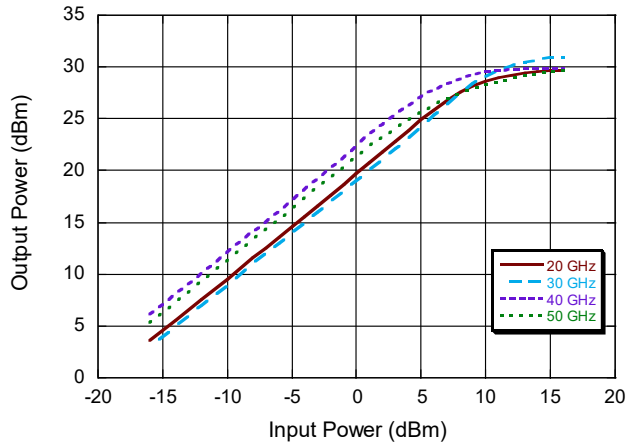


***P_{1dB}* vs. Frequency**

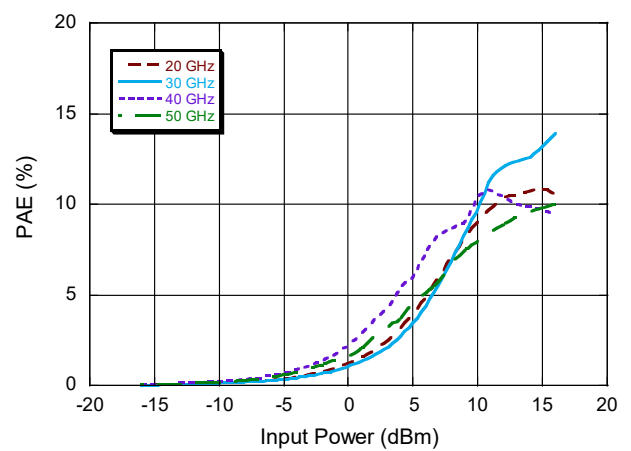


Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DSQ} = 1500\text{ mA}$

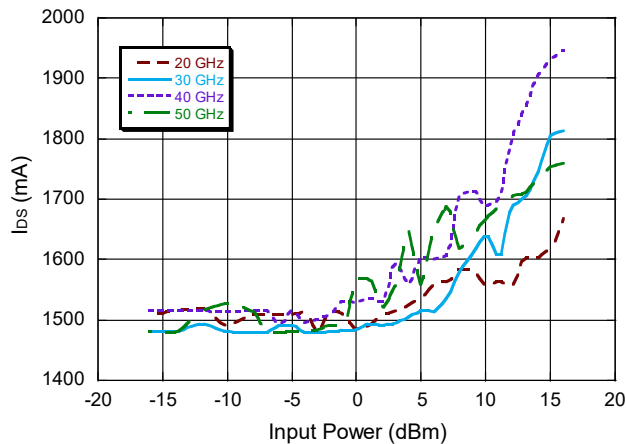
Output Power vs. Input Power



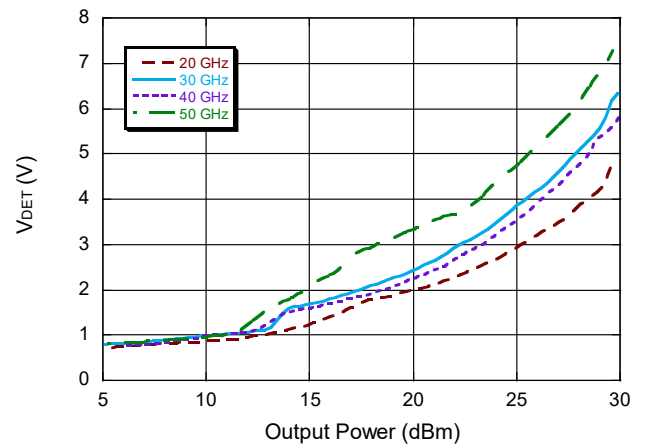
PAE vs. Input Power



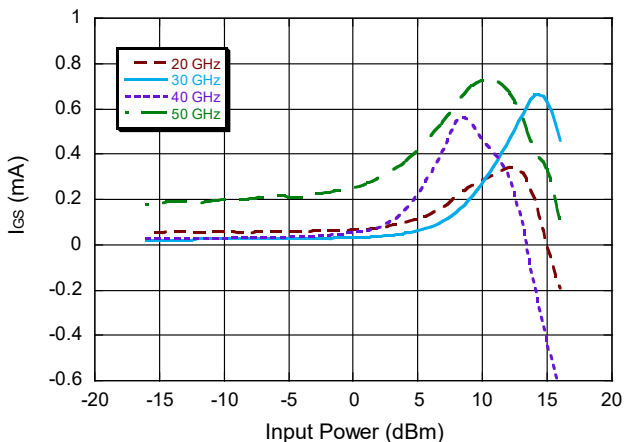
Drain Current vs. Input Power



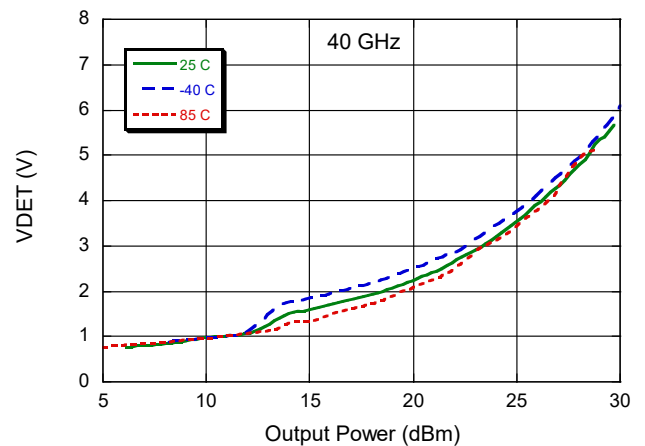
Detector Voltage vs. Output Power



Gate Current vs. Input Power

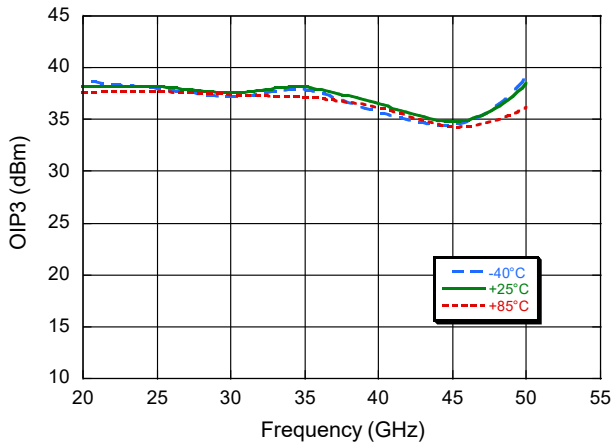


Detector Voltage vs. Output Power and Temperature

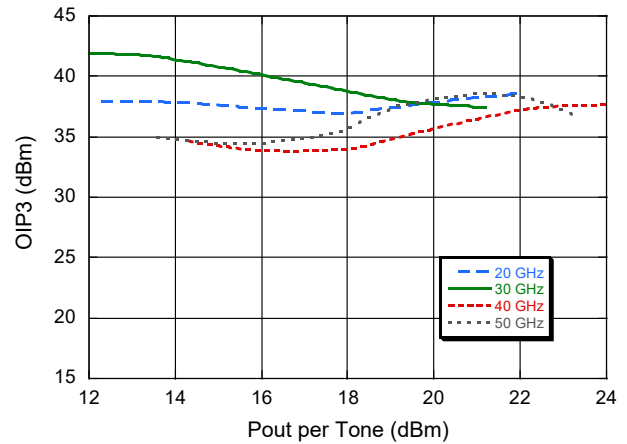


Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DSQ} = 1500\text{ mA}$

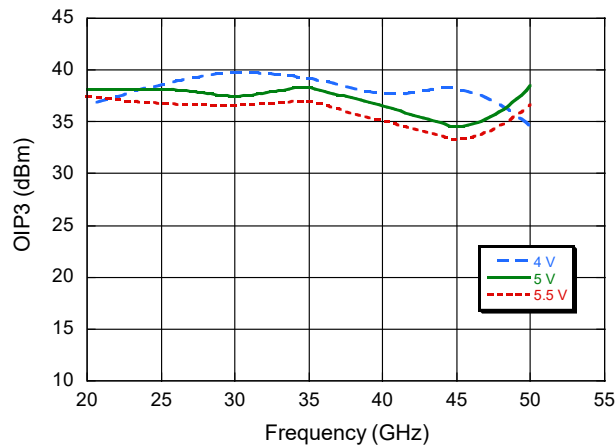
Output IP3 vs. Frequency @ $P_{out} = 21\text{ dBm}$ / Tone



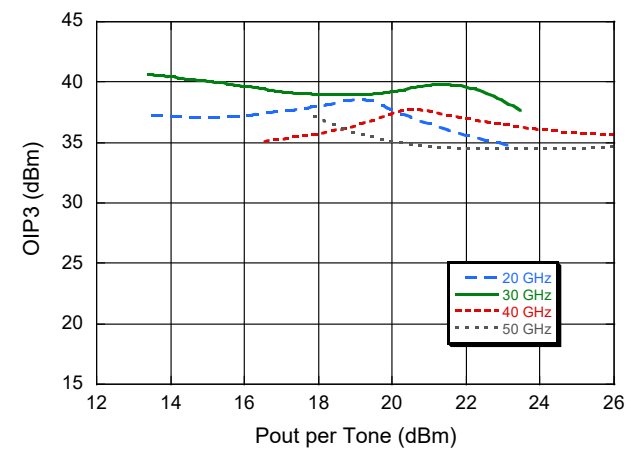
Output IP3 vs. Frequency and P_{out} per Tone
 $V_d = 5\text{ V}$



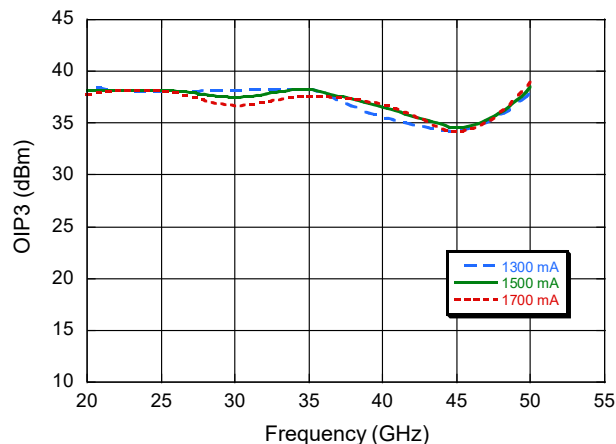
Output IP3 vs. Frequency @ $P_{out} = 21\text{ dBm}$ / Tone



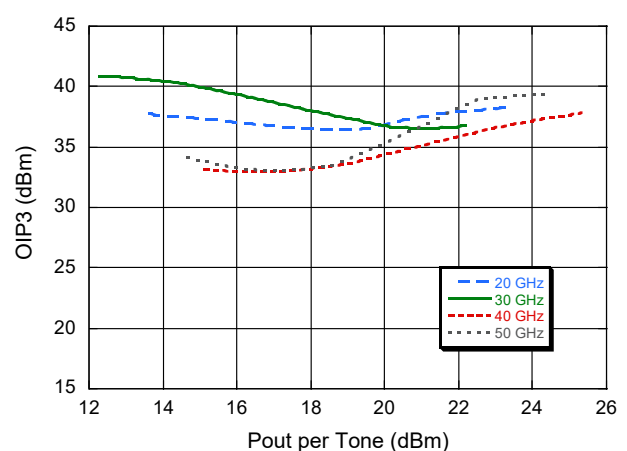
Output IP3 vs. Frequency and P_{out} per Tone
 $V_d = 4\text{ V}$



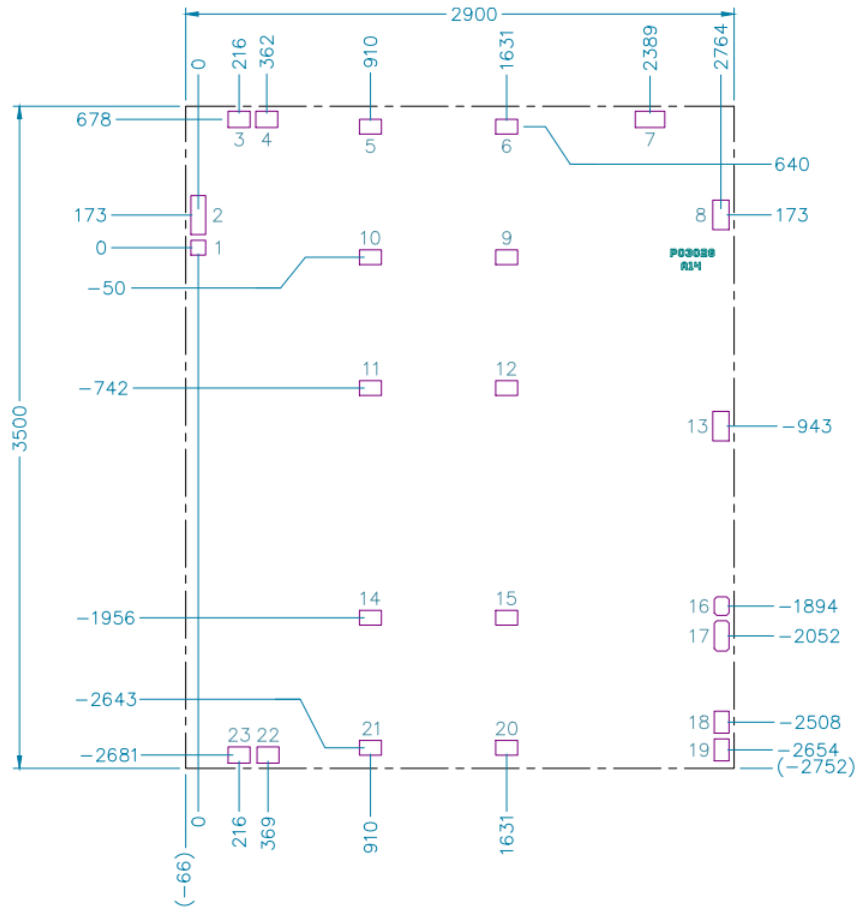
Output IP3 vs. Frequency @ $P_{out} = 21\text{ dBm}$ / Tone



Output IP3 vs. Frequency and P_{out} per Tone
 $V_d = 5.5\text{ V}$



Die Dimensions



Pad Dimensions (µm)

Pad #	X	Y
1	78	78
2	78	206
3,4,22,23	116	86
5,6,9,10,11,12, 14,15,20,21	116	78
7	156	86
8,13	88	156
16	78	98
17	78	160
18,19	80	120

Units are in microns with a tolerance of $\pm 5 \mu\text{m}$, except for die exterior dimensions which are street-center-to-street-center – nominal saw or laser kerf $\sim 25 \mu\text{m}$ tolerance each dimension. Pad and backside metal is gold. Die thickness is $100 \pm 10 \mu\text{m}$.

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