MAAP-011218-DIE

0.5 W Power Amplifier
71 - 86 GHz

Rev. V2

Features

- 4 Stage Power Amplifier for E-Band
- 20 dB Gain
- 8 dB Input and Output Match
- 27 dBm Saturated Output Power
- 31 dBm OIP3
- Variable Gain with Adjustable Bias
- Integrated Detector
- 2790 × 1950 × 50 μm Bare Die
- RoHS* Compliant

Description

The MAAP-011218 is a bare die power amplifier that operates from 71 - 86 GHz. The amplifier provides 20 dB small signal gain, 27 dBm output power and 31 dBm Output Third Order Intercept Point (OIP3). An integrated temperature compensated power detector is on-chip. The input and output are matched to 50 Ω with bond wires to external board.

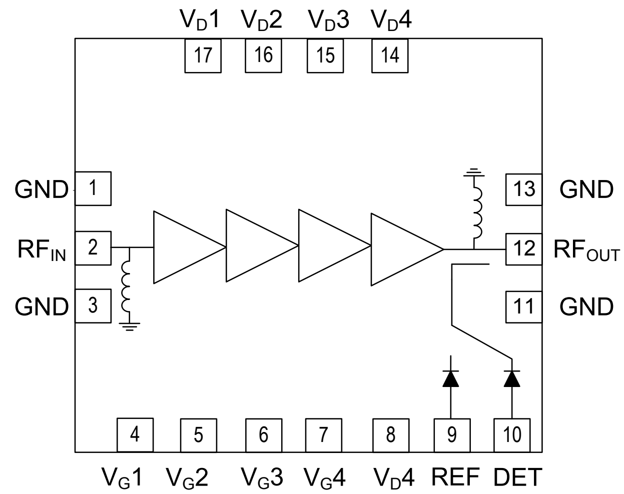
This amplifier is designed for use as a power amplifier stage in transmit chains and is ideally suited for E-band point-to-point radios. Each device is 100% RF tested to ensure performance compliance.

Ordering Information

Part Number	Package
MAAP-011218-DIE	Vacuum Release Gel Pak[1]

1. Die quantity varies.

Functional Schematic



Bond-pad Configuration

Pin #	Function	Pin #	Function
1	Ground[2]	10	DET
2	RF_{IN}	11	Ground[2]
3	Ground[2]	12	RF_{OUT}
4	V_G1	13	Ground[2]
5	V_G2	14	V_D4
6	V_G3	15	V_D3
7	V_G4	16	V_D2
8	V_D4	17	V_D1
9	REF	18	Ground[3]

2. These pads are internally connected to ground.
3. The backside of the die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC-0009861

Electrical Specifications: I_{DQ} = 760 mA (Full Bias), V_D = 4 V, Z_0 = 50 Ω, T_A = 25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	17 15 15	21 18 17	—
Input Return Loss	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	8 10 5	—
Output Return Loss	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	7 10 10	—
Noise Figure	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	7 7 7	—
OIP3	P_{IN} = -5 dBm/tone, 11 MHz Tone Spacing 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	—	32 31 31	—
Output P1dB	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	—	26 25 25	—
P_{SAT}	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	25 25 25	28 26 26	—
Efficiency	@ P1dB 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz @ P_{SAT} 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	%	—	12 6 6 15 9 9	—

Electrical Specifications: I_{DQ} = 460 mA (Reduced Bias), V_D = 4 V, Z_0 = 50 Ω, T_A = 25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	17 14 14	—
Input Return Loss	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	8 10 5	—
Output Return Loss	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	6 8 8	—
Noise Figure	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dB	—	7 7 7	—
OIP3	P_{IN} = -5 dBm/tone, 11 MHz Tone Spacing 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	—	29 29 29	—
Output P1dB	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	—	26 24 24	—
P_{SAT}	71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	dBm	—	27 25 25	—
Efficiency	@ P1dB 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz @ P_{SAT} 71 - 76 GHz 76 - 81 GHz 81 - 86 GHz	%	—	9 6 6 15 9 9	—

Recommended Quiescent Bias Currents, All Drain Supply Voltages are +4 V

Bias	I_D1 mA	I_D2 mA	I_D3 mA	I_D4 mA	Total mA
Full Bias	120	120	200	320	760
Reduced Bias	70	70	120	200	460

Absolute Maximum Ratings[4,5]

Parameter	Absolute Maximum
Drain Voltage	+4.3 V
Gate Bias Voltage	-1.5 V < V_G < +0.3 V
Drain Current	1135 mA
Input Power	20 dBm
Junction Temperature[6,7]	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF >1 x 10^6 hours .
7. Typical thermal resistance (Θ_{JC}) = 10.95°C/W.
   Junction Temperature (T_J) = Back Plate Temperature (T_{BP}) + Θ_{jc} * (V*I).
   a) For T_{BP} = +25°C,
      T_J = 58°C @ 4 V, 760 mA
   b) For T_{BP} = +85°C,
      T_J = 118°C @ 4 V, 760 mA

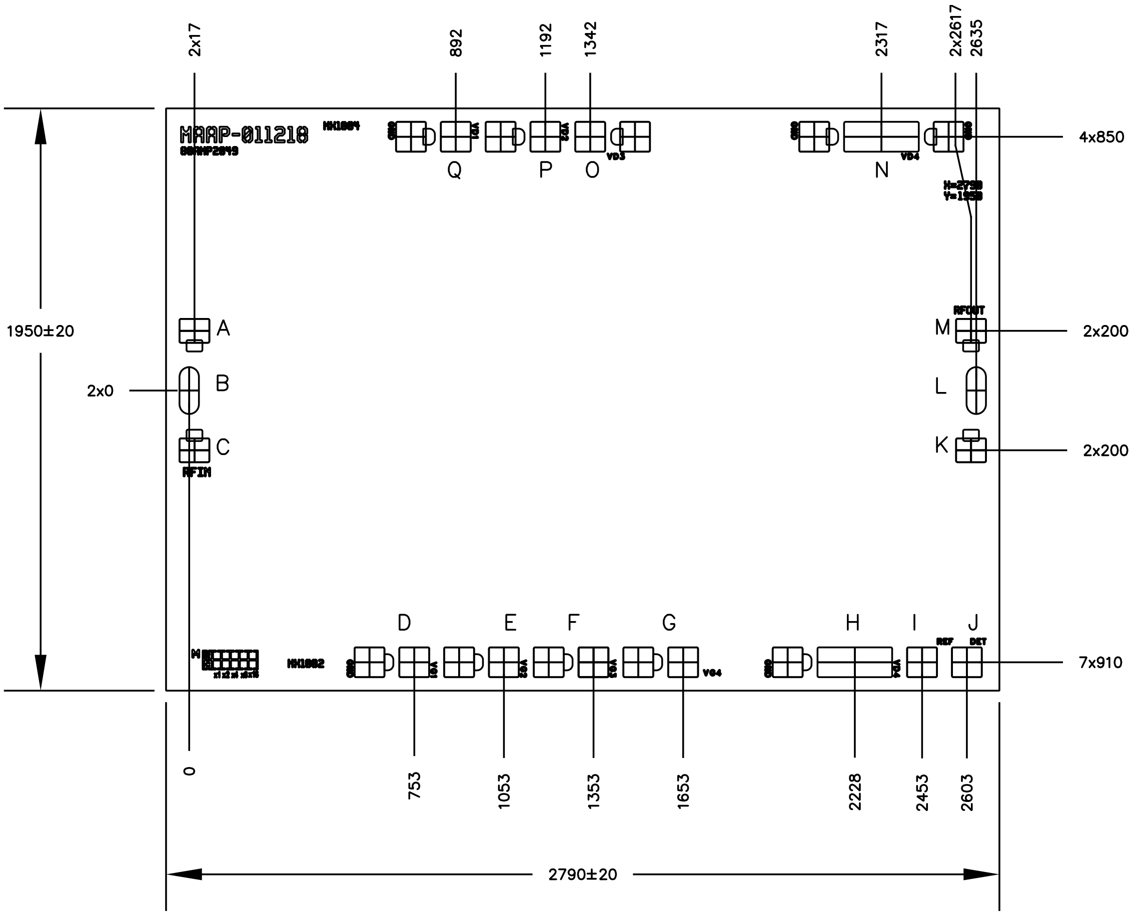
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These Class 1B electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Layout Dimensions[8,9]



8. All units in the outline drawing are microns, with a tolerance of ± 5 µm, except for die exterior dimensions which are street-centre-to-centre minus the nominal kerf, ± 20 µm tolerance.
9. Die Thickness is 50 ± 10 µm.

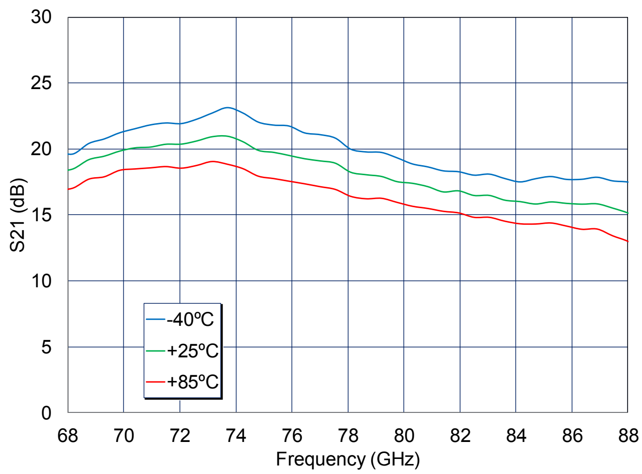
Bond Pad Opening Detail

Pad	Size (x) µm	Size (y) µm
B, L	65	157
D,E,F,G,I,J,O,P,Q	100	100
H, N	250	100
A,C,K,M	100	80

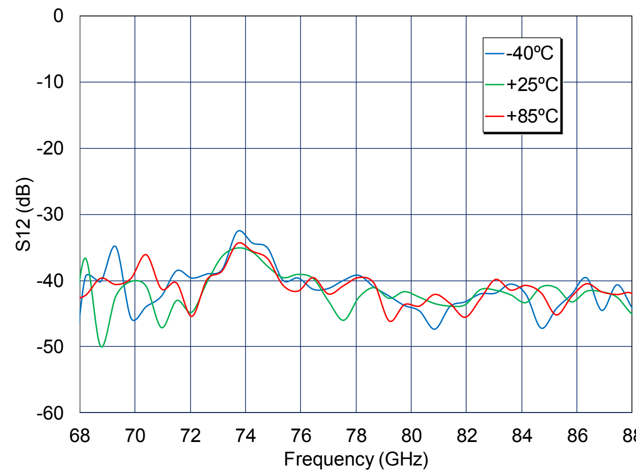
DC-0009861

Typical Performance Curves: I_{DQ} = 760 mA, V_D = 4 V, Full Bias

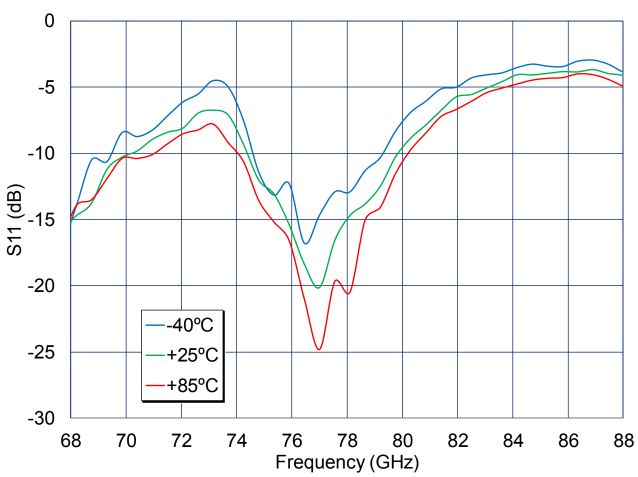
S21



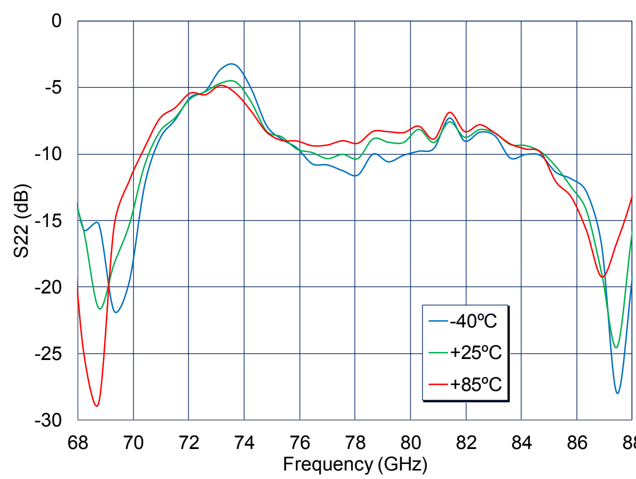
S12



S11

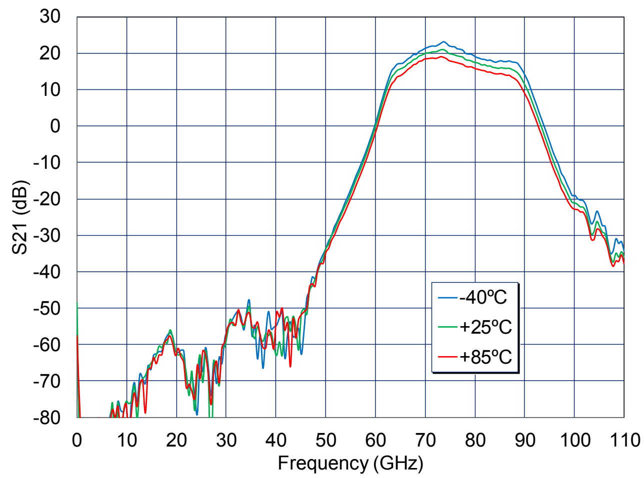


S22

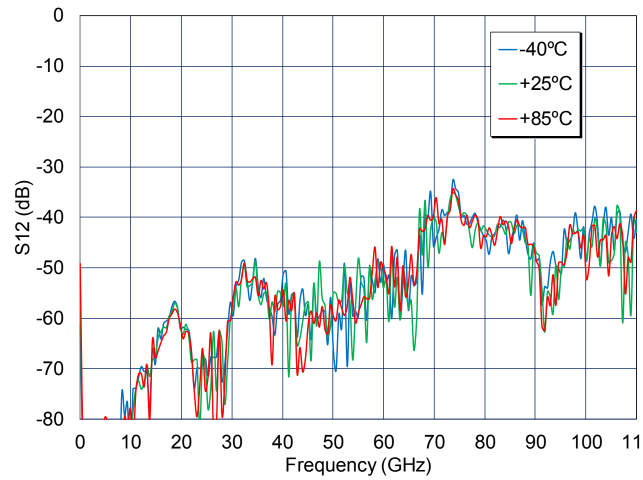


Typical Performance Curves: I_{DQ} = 760 mA, V_D = 4 V, Full Bias

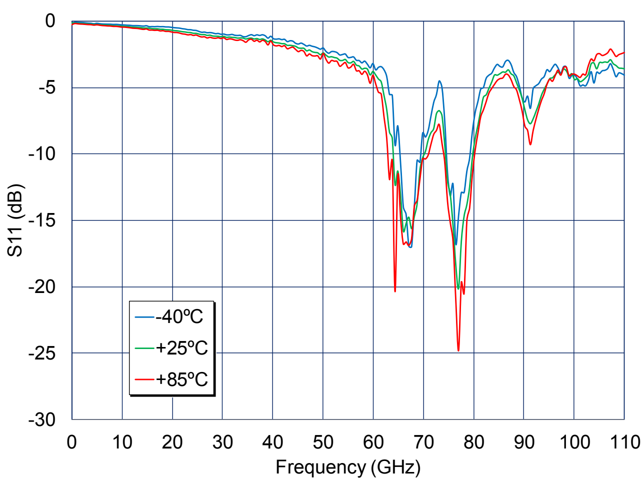
S21 (Wideband)



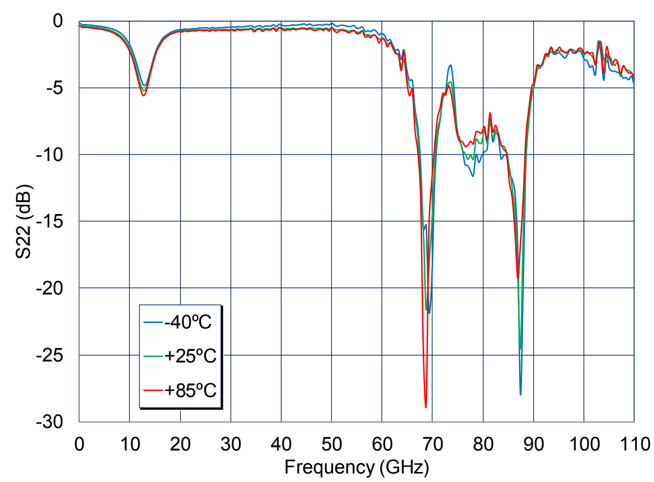
S12 (Wideband)



S11 (Wideband)

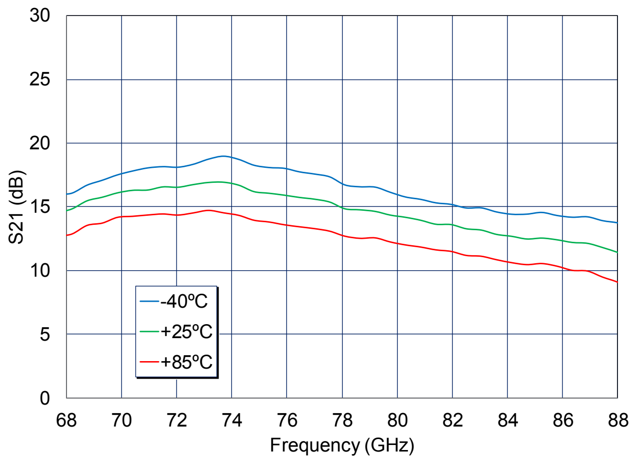


S22 (Wideband)

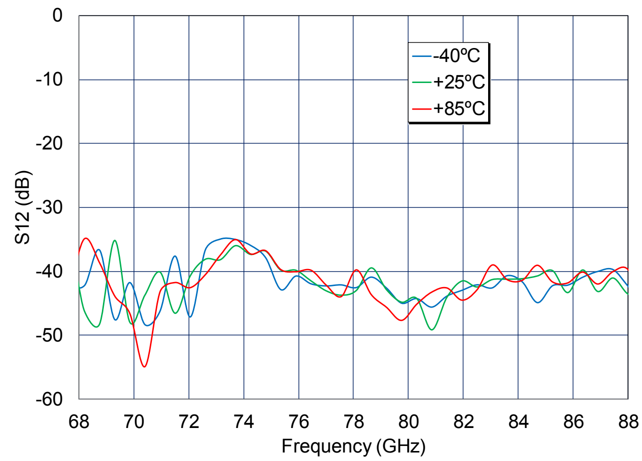


Typical Performance Curves: I_{DQ} = 460 mA, V_D = 4 V, Reduced Bias

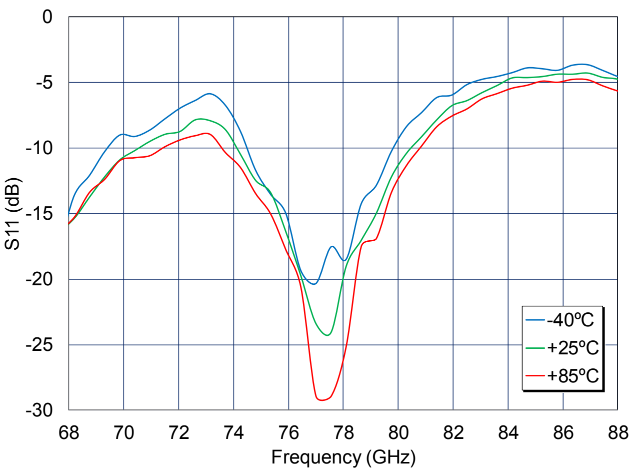
S21



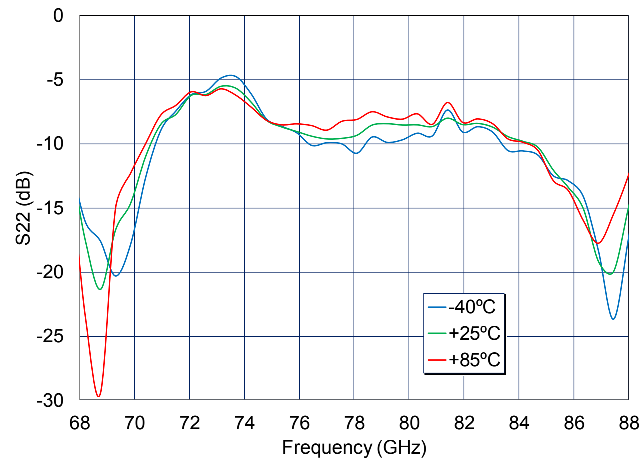
S12



S11

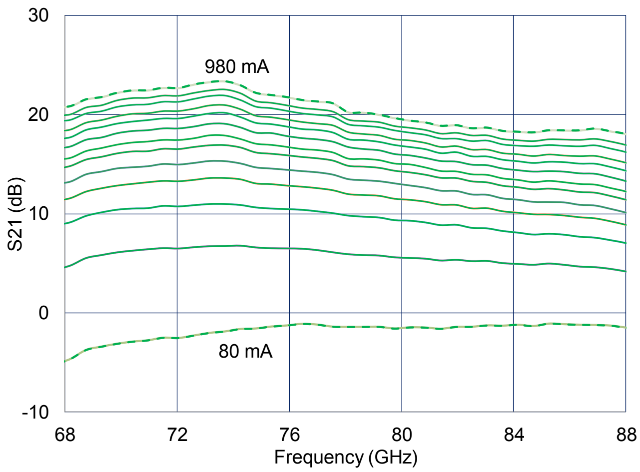


S22

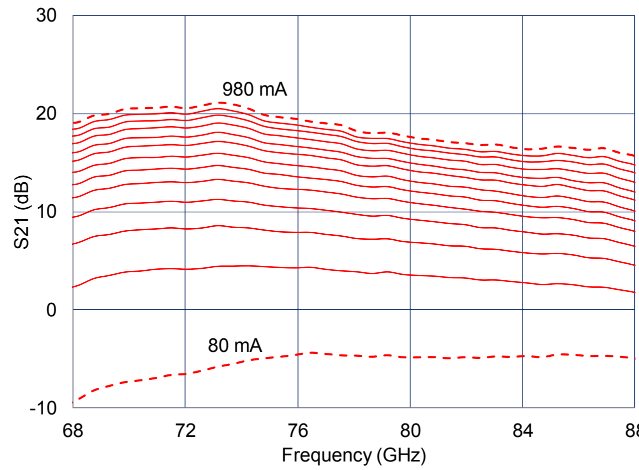


Typical Performance Curves: V_D = 4 V

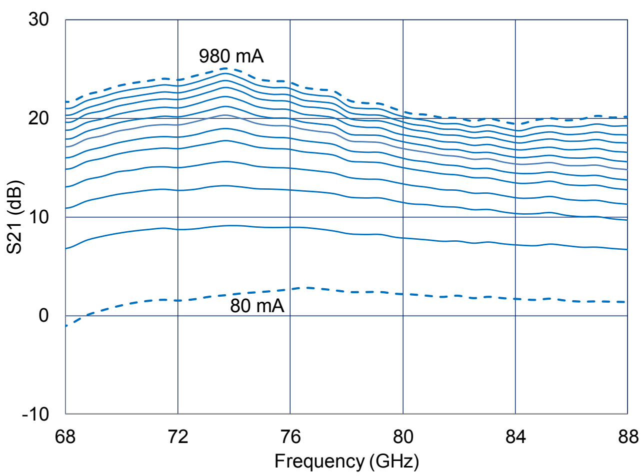
*S21 at Room Temperature vs. Total Drain Current**



*S21 at Hot Temperature vs. Total Drain Current**



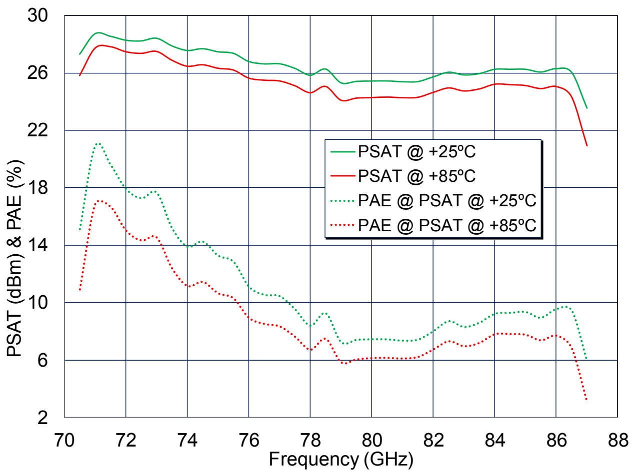
*S21 at Cold Temperature vs. Total Drain Current**



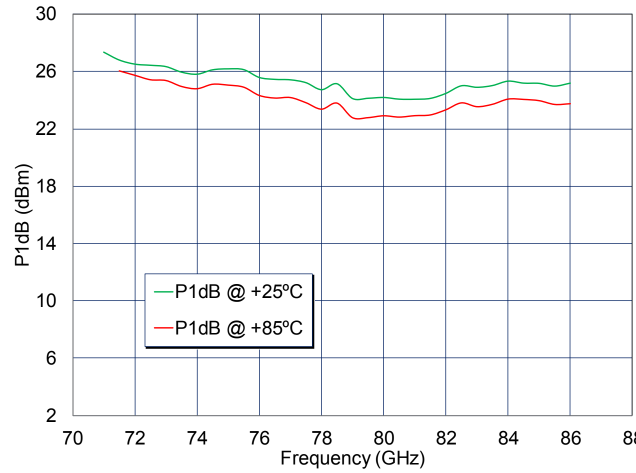
*Total Drain currents were set at 80,150, 230, 300, 380, 460, 530, 610, 680, 760, 840, 910, and 980 mA.

Typical Performance Curves: I_{DQ} = 760 mA, V_D = 4 V (Full Bias)

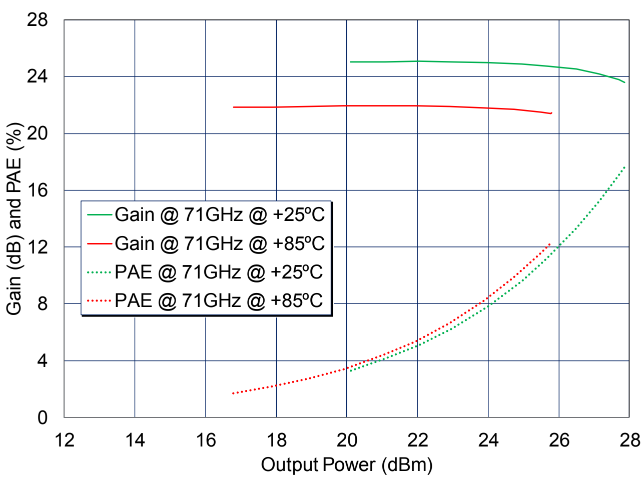
Saturated Power and PAE



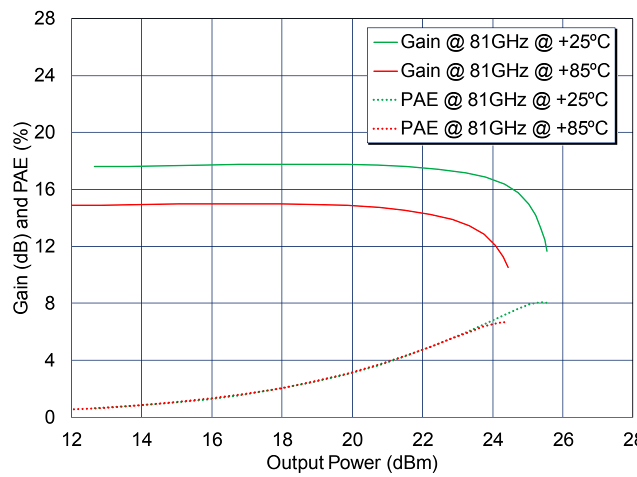
Output P1dB



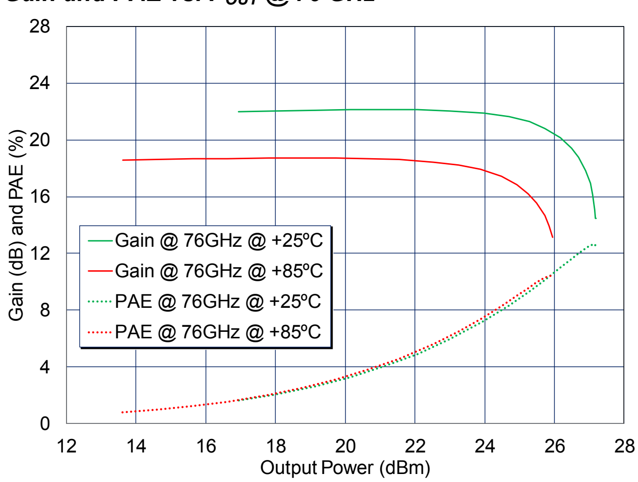
Gain and PAE vs. P_{OUT} @ 71 GHz



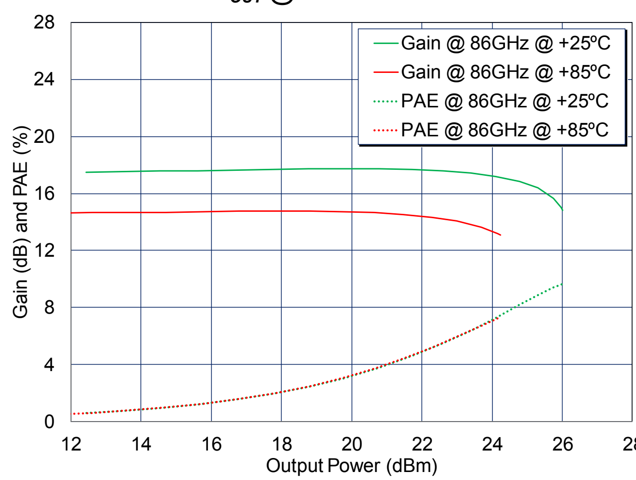
Gain and PAE vs. P_{OUT} @ 81 GHz



Gain and PAE vs. P_{OUT} @ 76 GHz

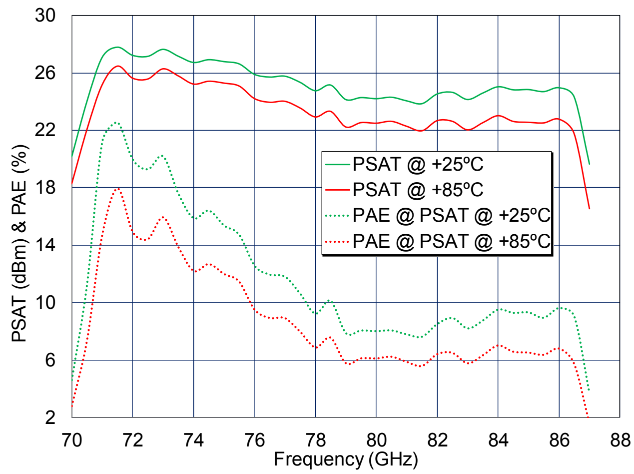


Gain and PAE vs. P_{OUT} @ 86 GHz

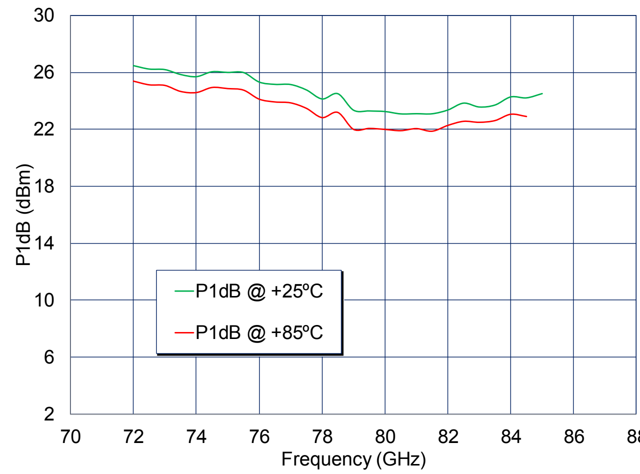


Typical Performance Curves: I_{DQ} = 460 mA, V_D = 4 V (Reduced Bias)

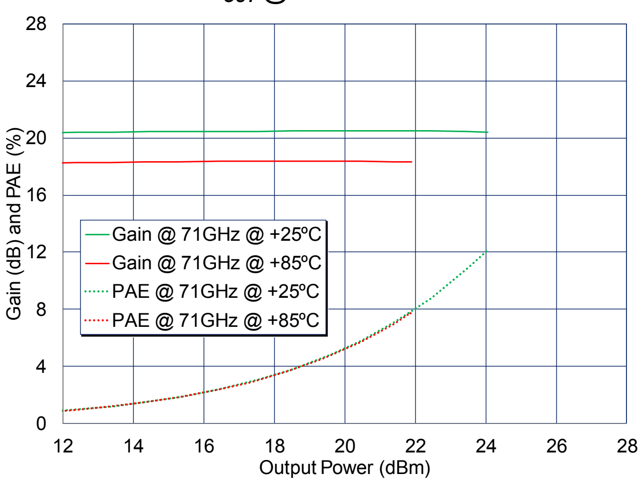
Saturated Power and PAE



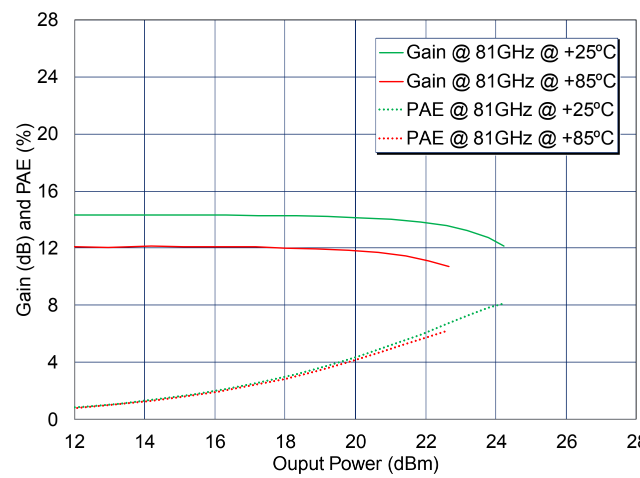
Output P1dB



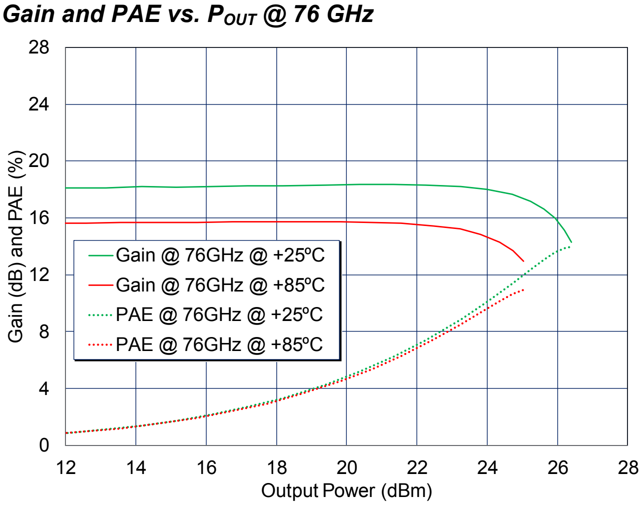
Gain and PAE vs. P_{OUT} @ 71 GHz



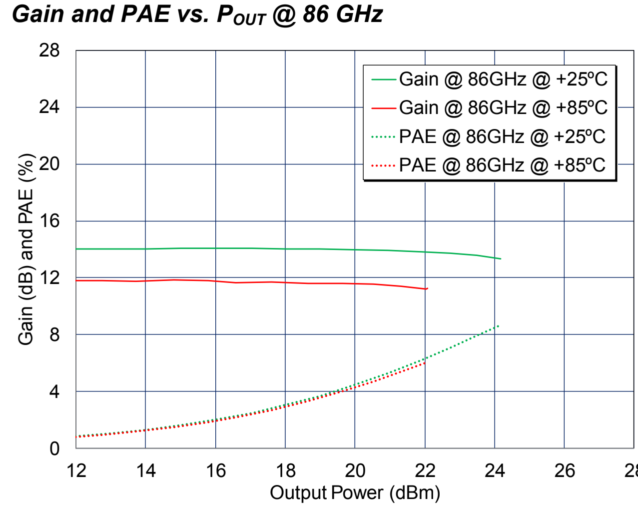
Gain and PAE vs. P_{OUT} @ 81 GHz



Gain and PAE vs. P_{OUT} @ 76 GHz

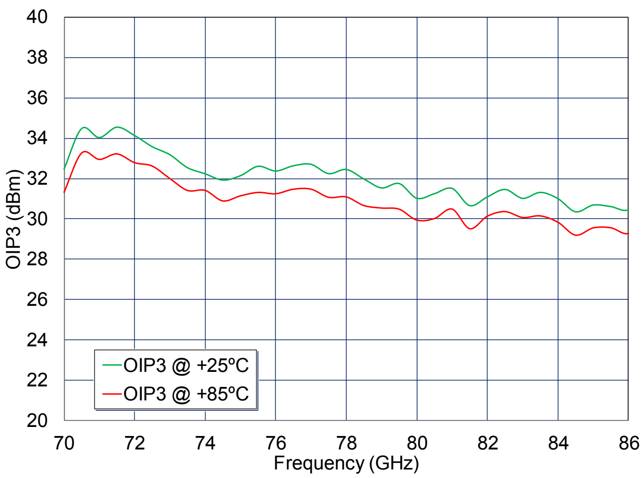


Gain and PAE vs. P_{OUT} @ 86 GHz

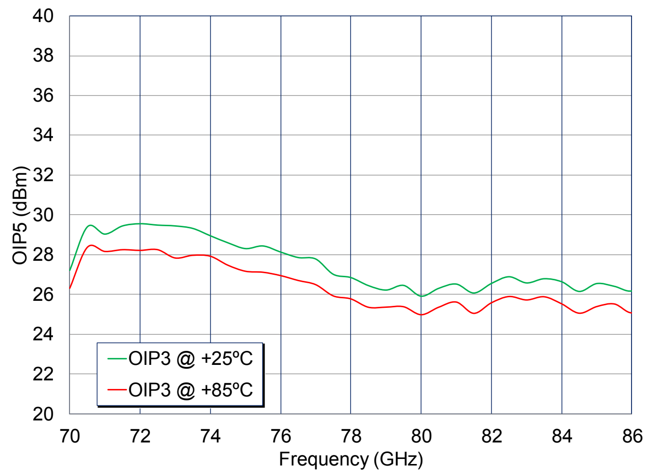


Typical Performance Curves: I_{DQ} = 760 mA, V_D = 4 V, Full Bias, RF P_{IN} = -5 dBm/tone

OIP3

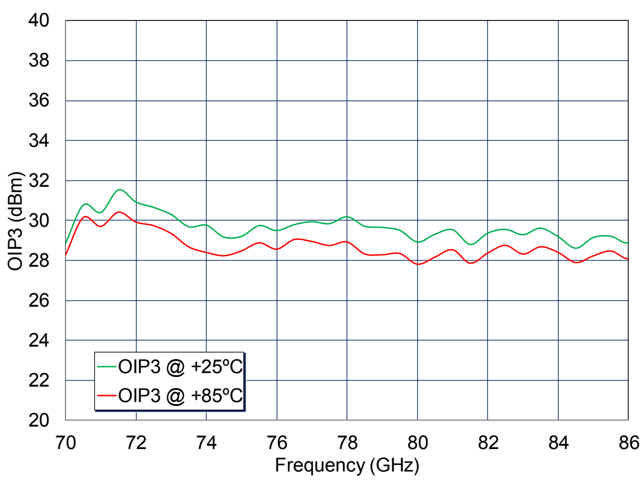


OIP5

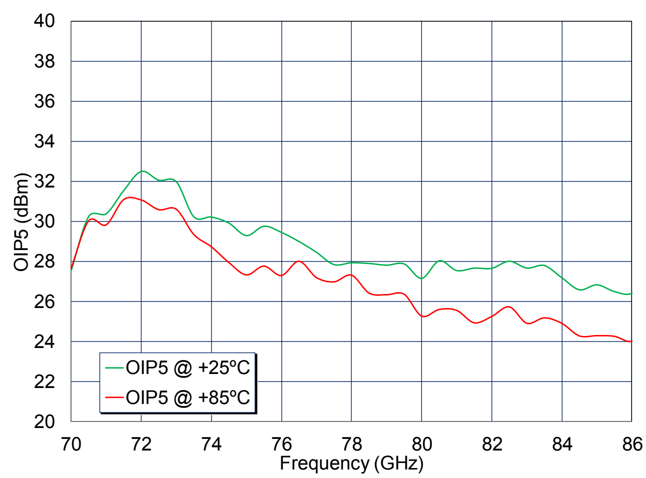


Typical Performance Curves: I_{DQ} = 460 mA, V_D = 4 V, Reduced Bias, RF P_{IN} = -5 dBm/tone

OIP3

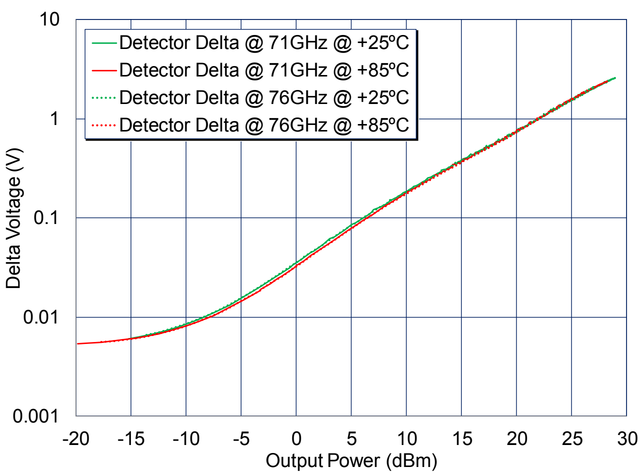


OIP5

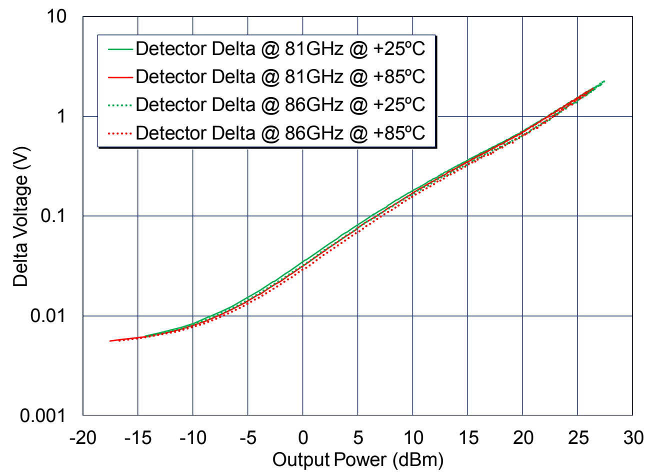


Typical Performance Curves: I_{DQ} = 760 mA, V_D = 4 V, Full Bias

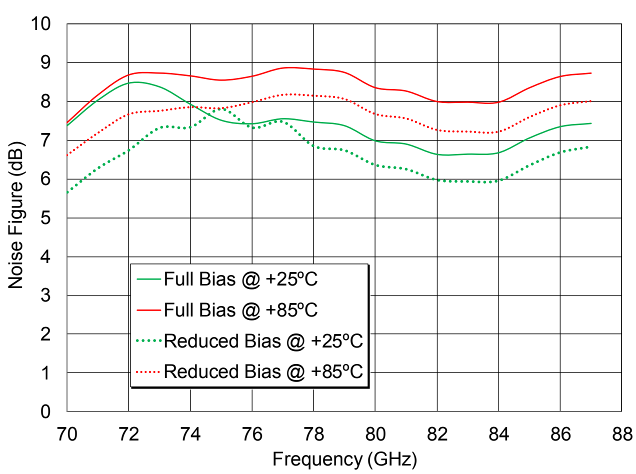
Detector Delta Voltage vs. Output Power, 71 - 76 GHz



Detector Delta Voltage vs. Output Power, 81 - 86 GHz



Noise Figure @ Full and Reduced Bias



Calibration Plane -

All data was measured on die with 200 µm pitch probes. All data was measured with an ISS cal.

App Note [1] Biasing -

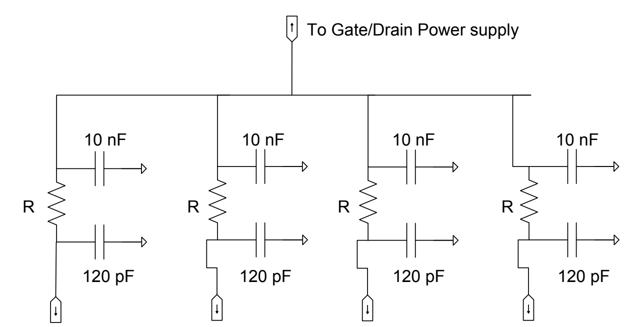
All gates should be pinched-off (V_G < -1 V) before applying drain voltage (V_D = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent full bias is V_D = 4 V, I_D1 = 120 mA, I_D2 = 120 mA, I_D3 = 200 mA and I_D4 = 320 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -

Each DC pin (V_D1,2,3,4 and V_G1,2,3,4) needs to have bypass capacitors (120 pF and 10 nF) mounted as close to the MMIC as possible.

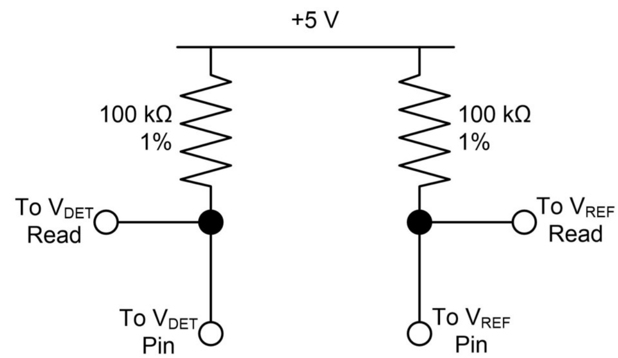
App Note [3] Common Gates and Drains -

When biasing the device with only a single gate or drain source additional isolation is required between each stage. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bypass capacitors should still accompany each stage as per App Note [2].



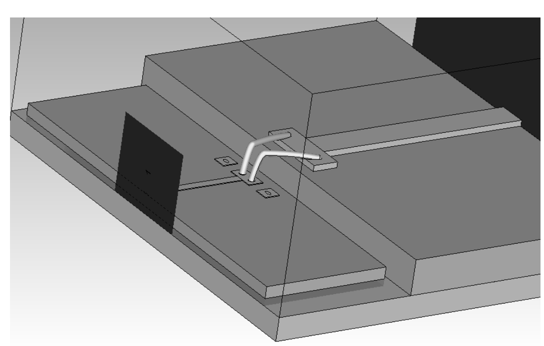
App Note [4] Detector Biasing Schematic -

As shown in the schematic below, the power detector is biased by matched 100 kΩ resistors to a +5 V supply. The difference voltage between V_{DET} and V_{REF} pins can be obtained using a differencing circuit.



App Note [5] Wire Bonding -

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 20 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below. Please see App Note [6] for further details.

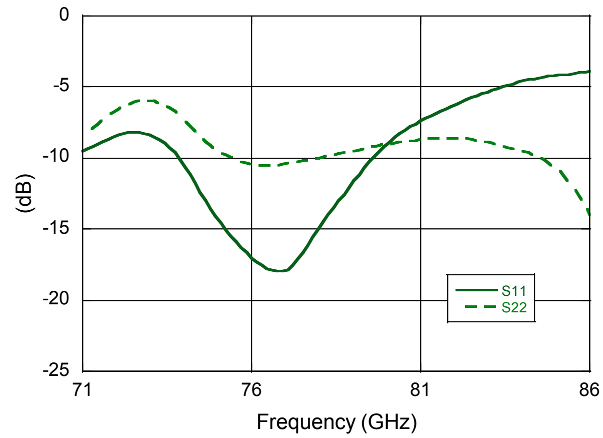


App Note [6] RF Matching -

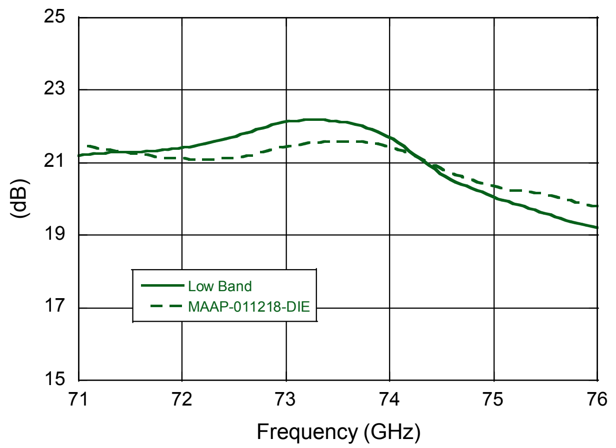
MAAP-011218 is designed to be a wideband RF power amplifier covering the 71 - 86 GHz band. By covering the full band, it enables customers to simplify BOM and circuitry for simple wideband performance. In cases where narrower band performance is preferred, external matching can be used to further optimise the return loss of the MMIC.

The board material used for matching was Isola Astra MT77. This has a dielectric constant (D_k) = 3 and a loss tangent (tan δ) of 0.0015. Simulations of the transition were performed in Analyst and can be provided on request. Transitions have been simulated to maintain return loss of -8 dB across the two bands of interest using Analyst.

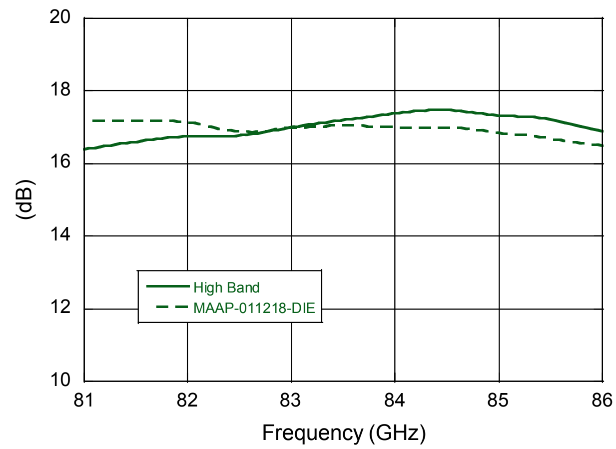
Return Loss



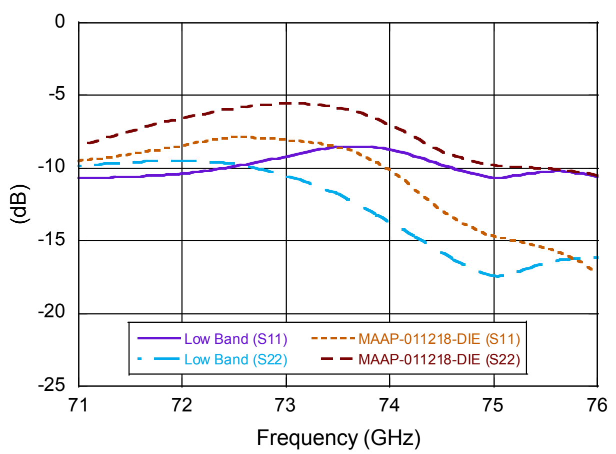
Low Band Gain



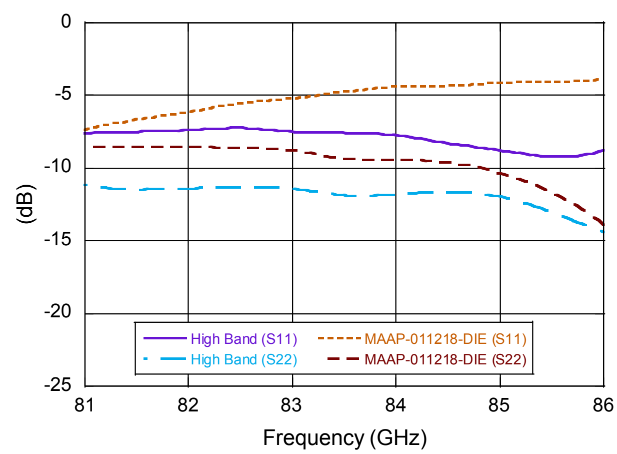
High Band Gain



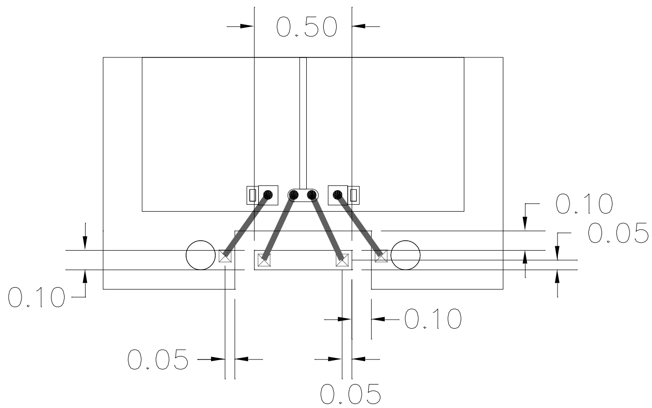
Low Band Return Loss

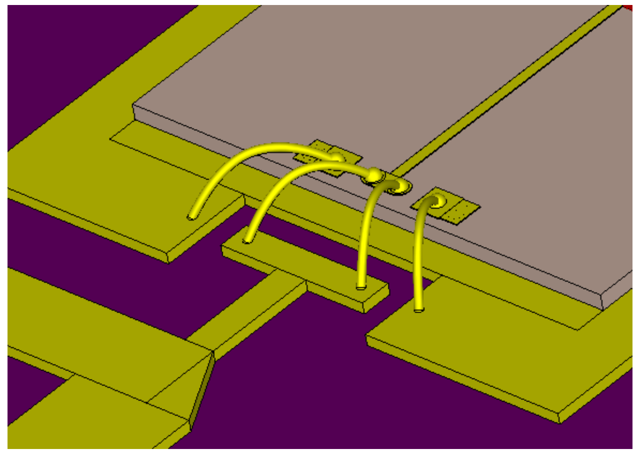


High Band Return Loss

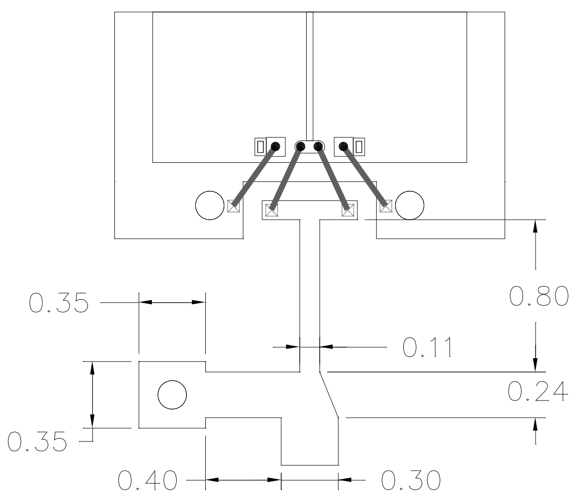


Input Dimensions
Common to every optimisation

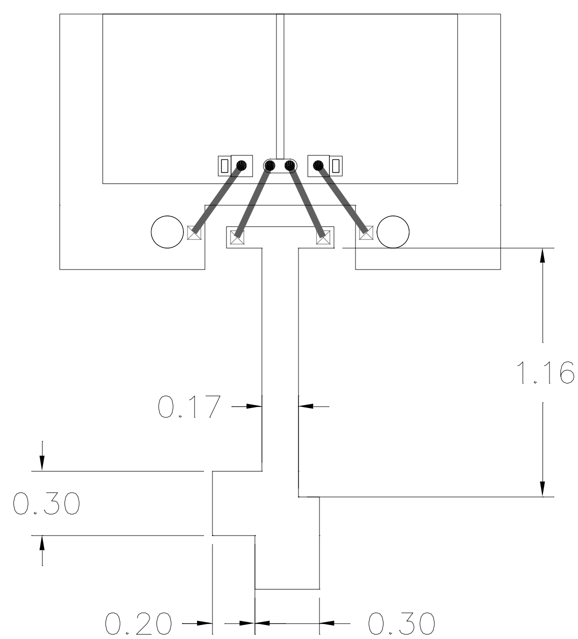




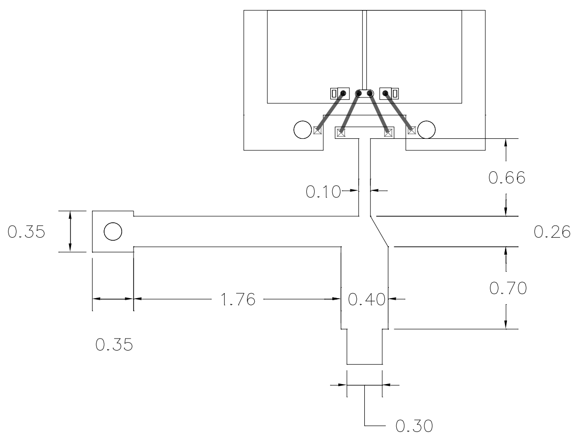
Low Band Optimisation
Input Side



Low Band Optimisation
Output Side



High Band Optimisation
Input Side



High Band Optimisation
Output Side