

MAAP-011215-DIE

Rev. V1

Features

- Saturated Output Power: 25 dBm
- Gain: 25 dBm
- OIP3: 32 dBm
- OIP5: 28 dBm
- Input Return Loss: 15 dBm
- Output Return Loss: 15 dBm
- Power Added Efficiency: 15%
- Variable gain with adjustable bias
- Integrated power detector
- Dimension: 2000 x 1700 x 50 μm
- RoHS* Compliant
- Bare Die

Applications

- Point-to-Point Communications / Short Haul
- Radar Front Ends
- Test and Measurement
- Communication Transmitters

Description

The MAAP-011215-DIE is a balanced four stage GaAs pHEMT MMIC power amplifier achieving an output power of 25 dBm in the range 55 to 70 GHz.

Functional Schematic



Pad Configuration¹

Pad #	Function		
1	RF Input		
2,11,13,24	GND		
3	Drain Voltage 1		
4,6,8,10,17,19,21,23	NC		
5	Drain Voltage 2		
7	Drain Voltage 3		
9	Drain Voltage 4		
12	RF Output		
14	Detector Output		
15	Detector Reference		
16	Gate Voltage 4		
18	Gate Voltage 3		
20	Gate Voltage 2		
22	Gate Voltage 1		

1. The exposed metal on the MMIC bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Package

Vacuum Release Gel Pack

For further information and support please visit: <u>https://www.macom.com/support</u>

Ordering Information

Part Number

MAAP-011215-DIE

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Electrical Specifications²: Frequency = 55 - 70 GHz, $T_A = +25^{\circ}C$, $V_D = 4 V$, $I_{DQ} = 400 mA$

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Gain	55 GHz 60 GHz 65 GHz 70 GHz	dB	18 18 17 17	25 25 24 24	
Input Return Loss	_	dB	—	15	—
Output Return Loss	—	dB	—	15	—
Saturated Output Power	—	dBm	—	25	—
OIP3	—	dBm	—	32	—
Drain Bias Voltage	—	V	—	4	—
Power Added Efficiency	—	%	—	15	—

2. Quiescent DC Bias: I_{D1} = 40 mA, I_{D2} = 80 mA, I_{D3} = 120 mA, I_{D4} = 160 mA. Total DC power = 1.6 W.

Absolute Maximum Ratings^{3,4,5}

Parameter	Absolute Maximum		
Drain Voltage	4.3 V		
Drain Current	635 mA		
Gate Bias Voltage (V _G 1,2,3)	1,2,3) -1.5 V < V _G < +0.3 V		
Input Power	20 dBm		
Storage Temperature	-55°C to +150°C		
Operating Temperature	-40°C to +85°C		
Junction Temperature ^{5,6}	+150°C		

3. Exceeding any one or combination of these limits may cause permanent damage to this device.

- 4. MACOM does not recommend sustained operation near these survivability limits.
- 5. Operating at nominal conditions with $T_J \le +150^{\circ}C$ will ensure MTTF > 1 x 10⁶ hours.

6. Typical thermal resistance (θjc) = 25.6°C/W. Junction Temperature (T_J) = Back Plate Temperature (T_{bp}) + θ_{jc} * (V * I)
a) For T_{bp} = +25°C, T_J = 66°C @ 4 V, 400 mA
b) For T_{bp} = +85°C, T_J = 129°C @ 4 V, 400 mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A (HBM) devices.

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(25, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600 mA) S-parameter @ I_{DSQ} = 400 mA Gain 35 40 20 25 = 25 mA 400 m 600 m/ 0 S-Parameters (dB) 15 -20 S21 (dB) 5 S2 -40 S11 -5 -60 -15 -80 -25 -100 -35 -120 54 56 58 60 62 64 66 68 70 0 10 20 30 40 Frequency (GHz) Frequency (GHz) Gain 54 - 70 GHz **Reverse Isolation** 35 0 30 25 mA 25 -20 -400 mA 600 mA 20 15 S21 (dB) -40 S12 (dB) 10

Typical S-Parameter Performance Curves @ +25°C, V_D = 4 V,

5 0 **2**5 mA 400 mA -5 600 m/ -10 -15 -20 54 56 58 60 62 64 66 68 70 Frequency (GHz)

Input Return Loss



Output Return Loss

-60

-80

-100

0 10 20



60

Frequency (GHz)

70 80 90 100

30

40 50

50 60 70 80 90 100

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S-parameter @ I_{DSQ} = 400 mA





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Typical S-Parameter Performance Curves over Temperature

P1dB @ I_{DSQ} = 400 mA









P4dB @ I_{DSQ} = 400 mA







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Typical Power Performance Curves @ +25°C and +85°C

Scalar Gain @ 60 GHz vs. PIN and IDSQ



PAE @ 60 GHz vs. PIN and IDSQ



Output Power @ 60 GHz vs. PIN and IDSQ



Power Detector Output @ 55, 60, 65 and 70 GHz



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OIP3 and P_{IN} = -10 dBm per Tone



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Typical Linearity Performance Curves @ 400 mA, V_D = 4 V, +25°C and +85°C

40 30 OIP3 (dBm) 20 +25°C 10 +85°0 0 54 56 58 60 62 64 66 68 70 Frequency (GHz)

OIP7 and P_{IN} = -5 dBm per Tone







OIP5 and $P_{IN} = -10$ dBm per Tone



Gain, OIP3 and IIP3 vs. Drain Current at 60 GHz







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Calibration Plane

All data was measured on die with 200 μ m pitch probes. The calibration plane is at the middle of the through, 178.5 μ m from the middle of the RF pad.

App Note [1] Biasing -

All gates should be pinched-off (V_G <-1 V) before applying drain voltage (V_D = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is V_D = 4 V, I_D1 = 40 mA, I_D2 = 80 mA, I_D3 = 120 mA and I_D4 = 160 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -

Each DC pin (V_D 1,2,3,4 and V_G 1,2,3,4) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.



App Note [3] Common Gates and Drains -

When biasing the device with only a single gate or drain source additional isolation is required between each stage. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bias pass capacitance should still be applied to each stage as per App Note [2].

App Note [4] Wire Bonding -

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25μ m) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below.



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App Note [5] Detector biasing schematic -

As shown in the schematic below, the power detector is implemented by providing 5 V bias and measuring the difference in output voltage. This measure can be achieved by mean of either standard op-amp in a differential mode configuration or analog-to-digital converters.



App Note [6] Handling the Die -

This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

App Note [7] Die Attach -

For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used.

If using eutectic, an 80% Au / 20% Sn preform is recommended. If using epoxy, a high thermal conductivity epoxy is required and a silver sintering type epoxy is recommended.



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Die Outline



Unless otherwise specified, all dimensions shown are μ m, with a tolerance of ± 5 μ m. Die thickness is 50 μ m ± 10 μ m. Bondpad backside metallization: Gold Die size reflects final dimensions.

Bond Pad Dimensions (µm)

Pad #	X	Y	Pin Label	
1	65	157	RF Input	
2,11,13,24	80	80	GND	
3	100	90	Drain Voltage 1	
4,6,8,10,17,19,21,23	92	142	NC	
5	100	90	Drain Voltage 2	
7	100	90	Drain Voltage 3	
9	100	90	Drain Voltage 4	
12	65	157	RF Output	
14	100	90	Detector Output	
15	100	90	Detector Reference	
16	100	90	Gate Voltage 4	
18	100	90	Gate Voltage 3	
20	100	90	Gate Voltage 2	
22	100	90	Gate Voltage 1	

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