Power Amplifier
71 - 86 GHz

MAAP-011205
Rev. V4

Features

- Linear Power Amplifier
- 19 dB Gain
- 23.5 dBm Output Power
- Variable Gain with Adjustable Bias
- Wide Dynamic Range Power Detector
- Lead-free 7 mm Air Cavity Package
- RoHS* Compliant

Applications

- E-Band Radar

Description

The MAAP-011205 is a surface mount E-band amplifier. This power amplifier operates from 71 - 86 GHz, and is designed to be used in transmit chains and is ideally suited for E-band radar applications.

Each device is 100% RF tested to ensure performance compliance.

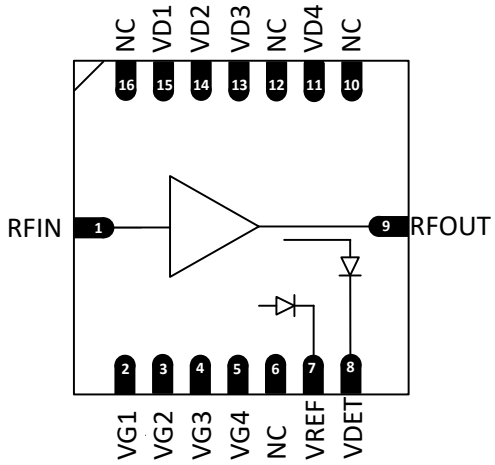
The MAAP-011205 is available in a 7 mm air cavity package that is RoHS complaint.

Ordering Information[1]

Part Number	Package
MAAP-011205	Bulk
MAAP-011205-TR0100	100 piece reel
MAAP-011205-TR0500	500 piece reel
MAAP-011205-SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration[3]

Pin #	Pin Name	Description
1	RF_{IN}	RF Input
2	V_{G1}	Gate Voltage, Stage 1
3	V_{G2}	Gate Voltage, Stage 2
4	V_{G3}	Gate Voltage, Stage 3
5	V_{G4}	Gate Voltage, Stage 4
6,10,12,16	NC[2]	No Connection
7	V_{REF}	Detector Reference Voltage
8	V_{DET}	Detector Output Voltage
9	RF_{OUT}	RF Output
11	V_{D4}	Drain Voltage, Stage 4
13	V_{D3}	Drain Voltage, Stage 3
14	V_{D2}	Drain Voltage, Stage 2
15	V_{D1}	Drain Voltage, Stage 1

2. MACOM recommends connecting unused package pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: Freq. = 71-86 GHz, T_C = 25°C, V_D = +4 V, I_{DQ} = 720 mA, Z_0 = 50

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	P_{IN} ≤ -10 dBm 71 GHz 76 GHz 81 GHz 86 GHz	dB	—	 19 18 18 20	—
Output P1dB	—	dBm	—	21	—
Output Power	P_{IN} = +10 dBm 71 GHz 76 GHz 81 GHz 86 GHz	dBm	—	 23 23.5 24 24	—
Input Return Loss	—	dB	—	-10	—
Output Return Loss	—	dB	—	-12	—
Detector Output Voltage Range	—	mV	10	—	1000
Output Detector Voltage (V_{DET} - V_{REF})	P_{OUT} = 6 dBm P_{OUT} = 16 dBm P_{OUT} = 26 dBm	dBm	—	0.25 0.4 1.0	—
Drain Current	Quiescent Bias P_{IN} = +10 dBm	mA	—	720 1500	— 1800

Maximum Operating Conditions

Parameter	Maximum
Input Power	13 dBm
Drain Supply Voltage	4.2 V
Quiescent Current	910 mA
Junction Temperature[4,5]	+150°C
Operating Temperature	-40°C to +85°C

4. Operating at nominal conditions with T_J ≤ +150°C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 18°C/W.
   a) For T_C = +25°C,
   T_J = 77°C @ 4 V, 720 mA
   b) For T_C = +85°C,
   T_J = 137°C @ 4 V, 720 mA

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power	16 dBm
Drain Supply Voltage	4.5 V
Quiescent Current	1.05 A
Junction Temperature[8]	+160°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1A devices.

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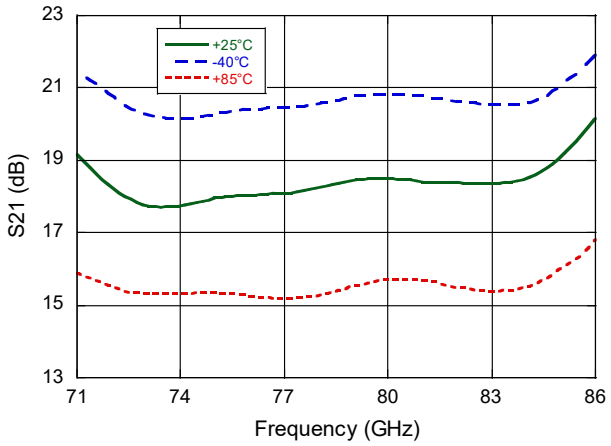
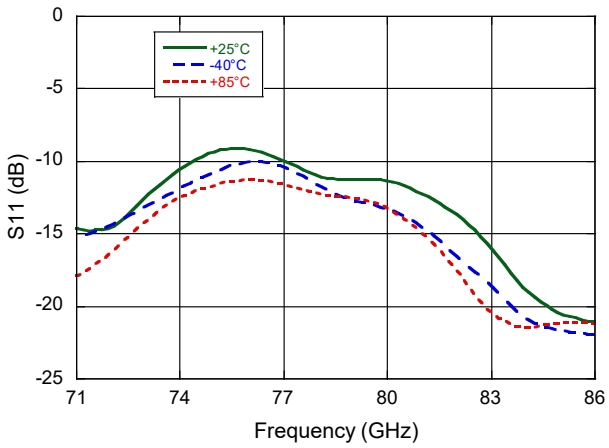
Typical Performance Curves

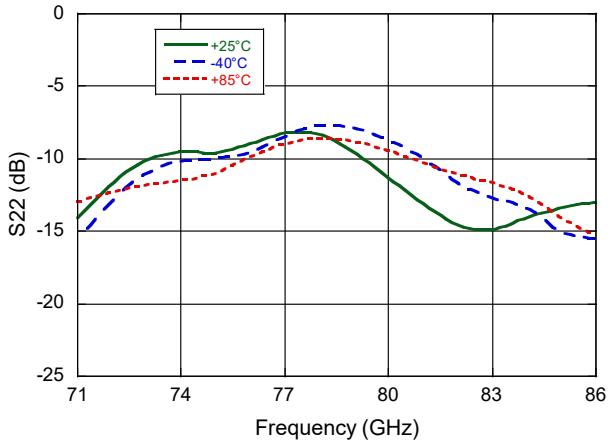
Small Signal Gain



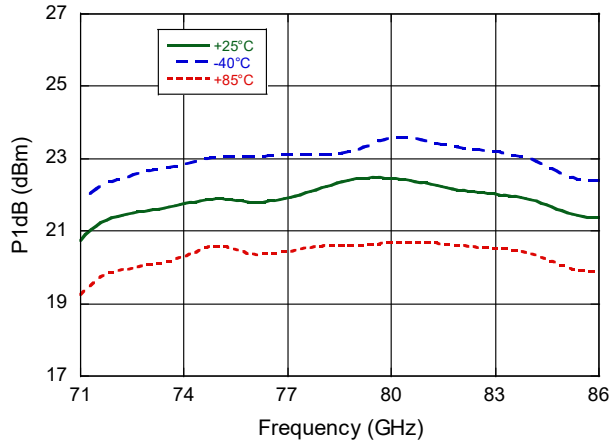
Input Return Loss



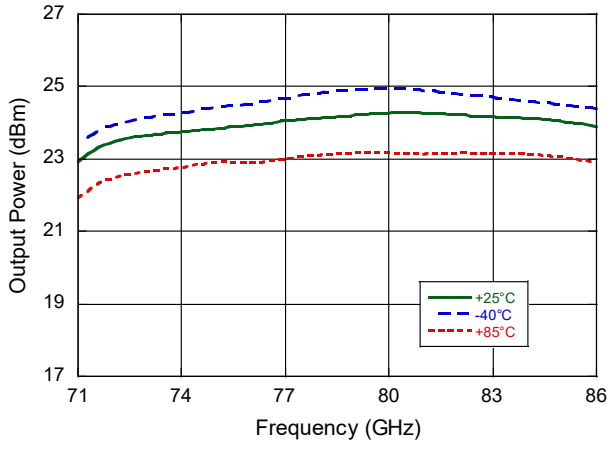
Output Return Loss



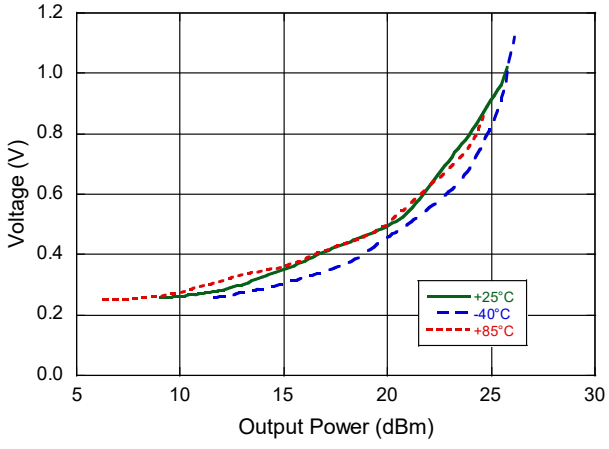
P1dB



Output Power @ P_{IN} = 13 dBm



Vdetector



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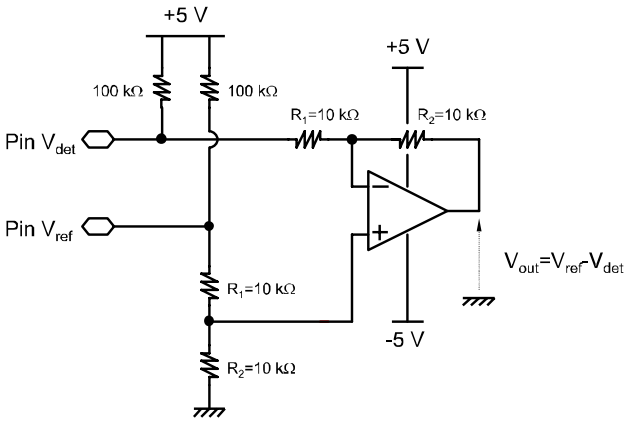
Application Notes



App Note [1] Biasing - It is recommended to bias the amplifier with V_D = 4 V and I_D = 720 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results.

App Note [2] Bias Arrangement - Each DC pin (V_D1,2,3,4 and V_G1,2,3,4) must have a DC bypass capacitor with a value of 0.1 µF as close to the package as possible.

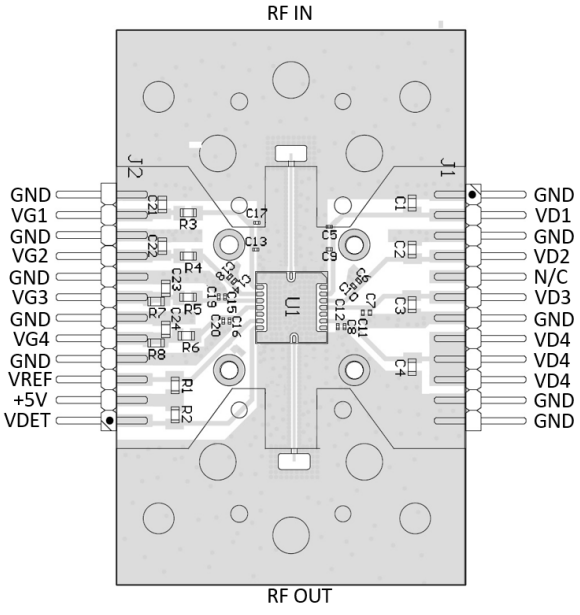
App Note [3] Power Detector - As shown in the schematic below, the power detector is implemented by providing 5 V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

App Note [4] Sample Board Biasing - For most consistent and highest performance, it is recommended to bias the amplifier by adjusting the gate voltages for each stage to achieve target drain currents.

Stage 1 = 60 mA,
Stage 2 = 120 mA,
Stage 3 = 240 mA,
Stage 4 = 300 mA.
Total = 720 mA

App Note [5] Sample Board Biasing - Each gate and drain bias should have grounds combined at the sample board. Combining grounds at the power supplies can produce ground loops which can introduce instability. This is manifested by the drain currents changing as each stage is powered up.

App Note [6] Sample board DC connector pinout - As shown in the figure to the right.



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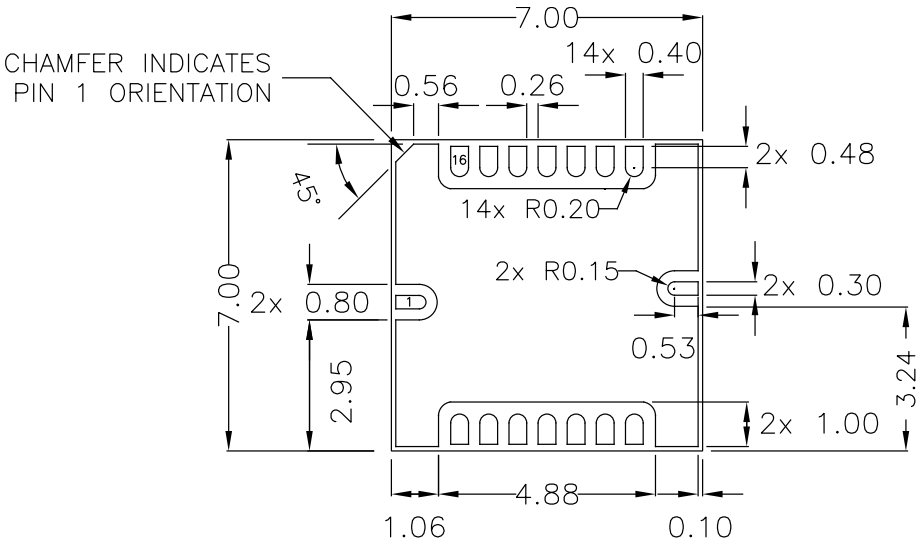
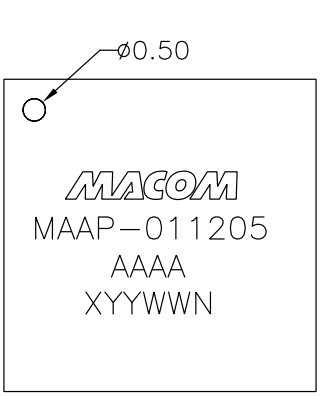
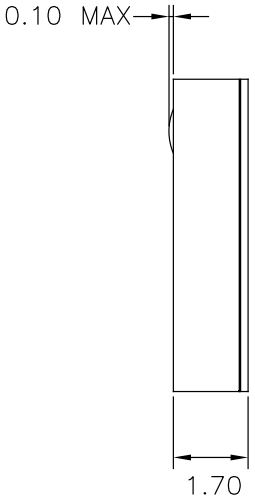
Package Dimensions†



Footprint (Viewed from Above)



Top View



Side View

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is ENEPIG.
All dimensions are in millimeters.

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