# MAAP-011199

## Power Amplifier
## 80 - 100 GHz

***Preliminary*** **- Rev. V2P**

### Features

- Saturated Output Power: 24 dBm
- Gain: 12 dB
- Input Return Loss: >15 dB
- Output Return Loss: >15 dB
- Reverse Isolation: >30 dB
- Dimension: 1800 x 2000 $\mu m^2$
- RoHS* Compliant
- Bare Die

### Description

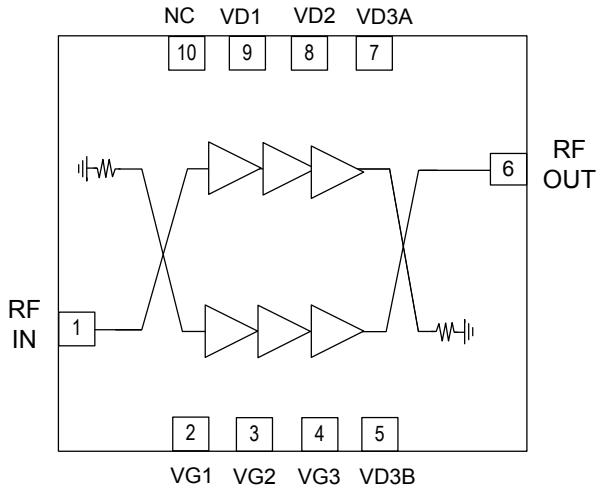
The MAAP-011199 is a balanced 3 stage GaAs pHEMT MMIC power amplifier. The device operates from 80 to 100 GHz and provides typically 24 dBm of output power. The power amplifier's balanced architecture results in excellent input and output match to 50 Ω across the entire 80 - 100 GHz frequency band and the multi-stage design provides high gain of 12 dB.

The device is well suited to communication, sensor, imaging and instrumentation applications

### Ordering Information

| Part Number | Package |
|---|---|
| MAAP-011199-DIEPPR | Pre-Production Samples |

### Functional Schematic




### Pin Configuration

| Pin No. | Function |
|---|---|
| 1 | RF IN |
| 2 | VG1 |
| 3 | VG2 |
| 4 | VG3 |
| 5 | VD3B |
| 6 | RF OUT |
| 7 | VD3A |
| 8 | VD2 |
| 9 | VD1 |
| 10 | NC |

Preliminary Information

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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*Preliminary* - Rev. V2P

### Electrical Specifications[1]: Freq. = 80 - 100 GHz, $T_A$ = 25°C, $V_D$ = 4 V, $V_G$ = - 0.5 V, $Z_0$ = 50

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Gain | dB | — | 12 | — |
| Input Return Loss | dB | — | 15 | — |
| Output Return Loss | dB | — | 15 | — |
| Quiescent Drain Current | mA | — | 400 | — |
| $P_{1dB}$ | dBm | — | 22 | — |
| Saturated Output Power | dBm | — | 24 | — |

1. Quiescent DC Bias: $I_D1$ = 100 mA, $I_D2$ = 100 mA, $I_D3$ = 200 mA. Total DC power = 1.6 W.

### Absolute Maximum Ratings[2,3,4,5]

| Parameter | Absolute Maximum |
|---|---|
| Drain Voltage | +4.3 V |
| Drain Current | 670 mA |
| Gate Bias Voltage ($V_G$1,2,3) | -1.5 V < $V_G$ < 0.3 V |
| Input Power | 17 dBm |
| Storage Temperature | -55°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Junction Temperature | 150°C |
| Thermal Resistance | 22.5 °C/W |

2. Thermal resistance value and maximum drain current limits assume no RF cooling effect.
3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x $10^6$ hours.

### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. This device is classified as Class 1C for HBM test and Class II for CDM test.

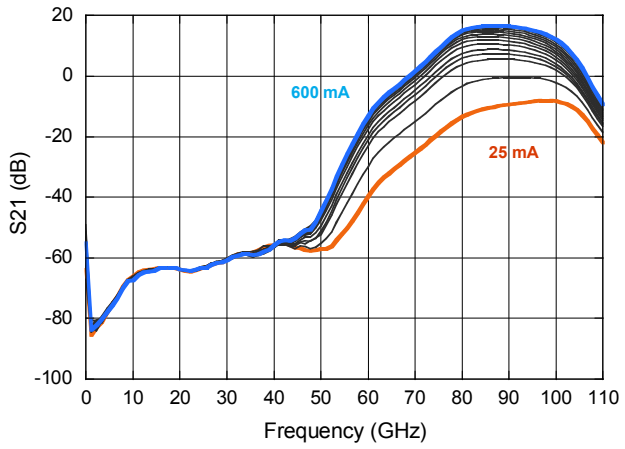
### Calibration Plane

All data was measured with an ISS calibration to the probe tip.

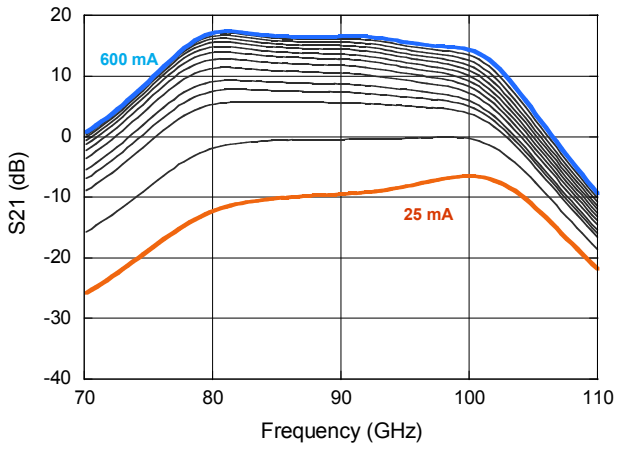
Preliminary Information

## Typical Performance Curves @ +25°C

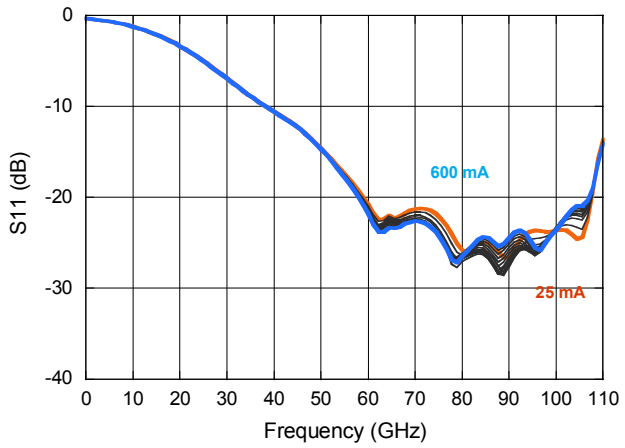
***Gain***



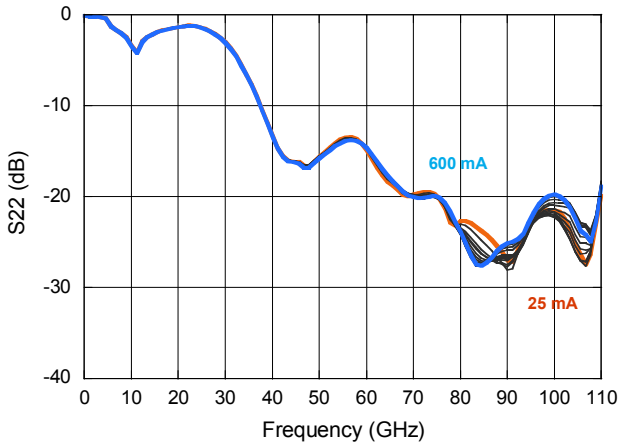

***Gain 70 - 110 GHz***



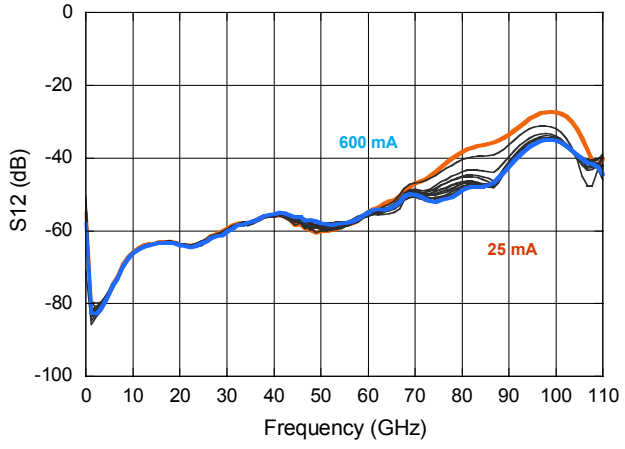

***Input Return Loss***




***Output Return Loss***




***Reverse Isolation***

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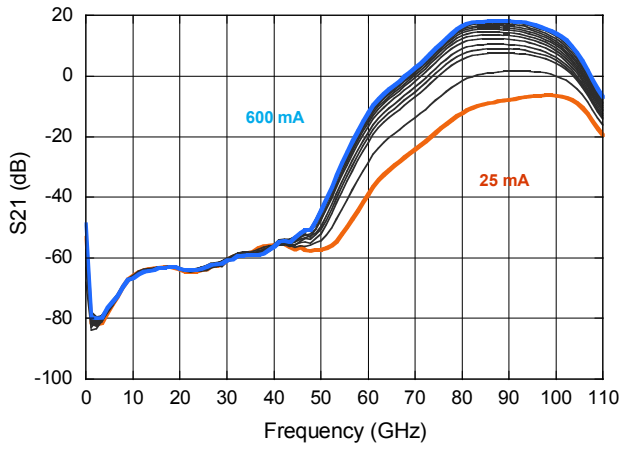
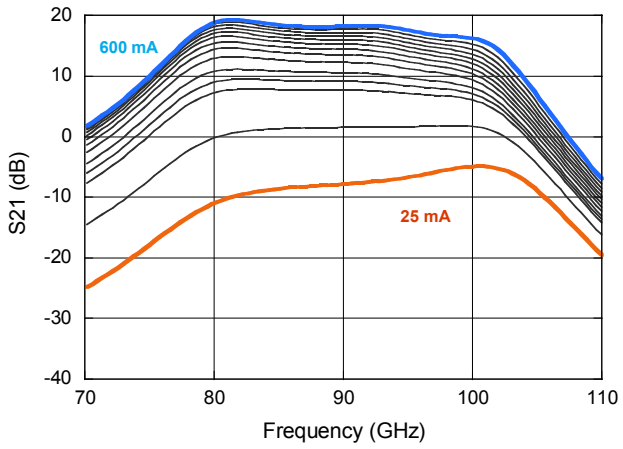
## Typical Performance Curves @ -40°C

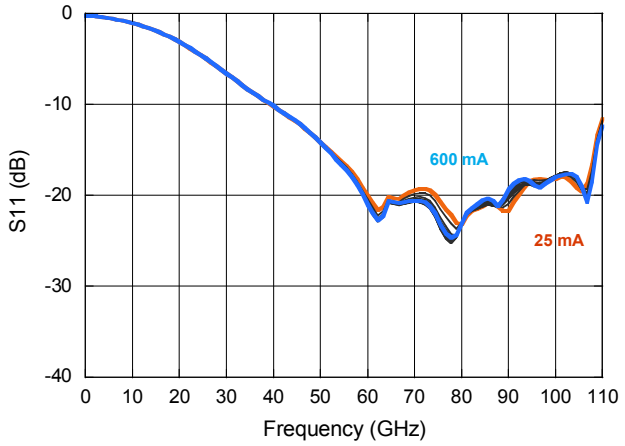
***Gain***



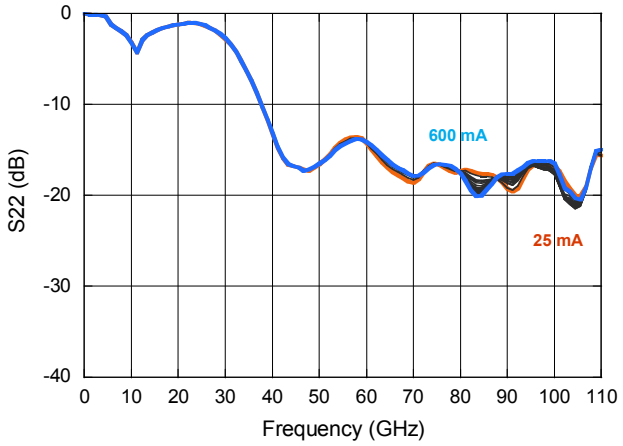

***Gain 70 - 110 GHz***



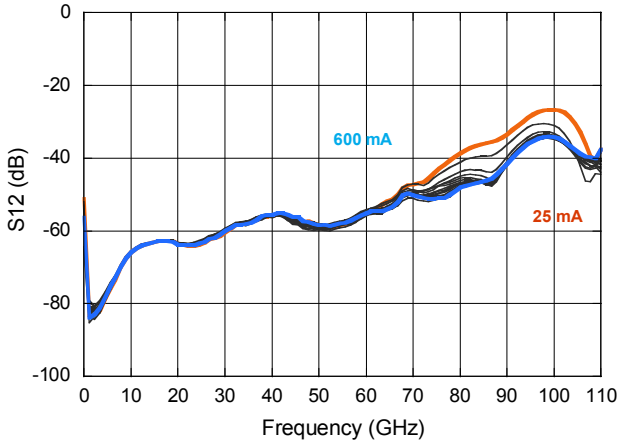

***Input Return Loss***




***Output Return Loss***




***Reverse Isolation***

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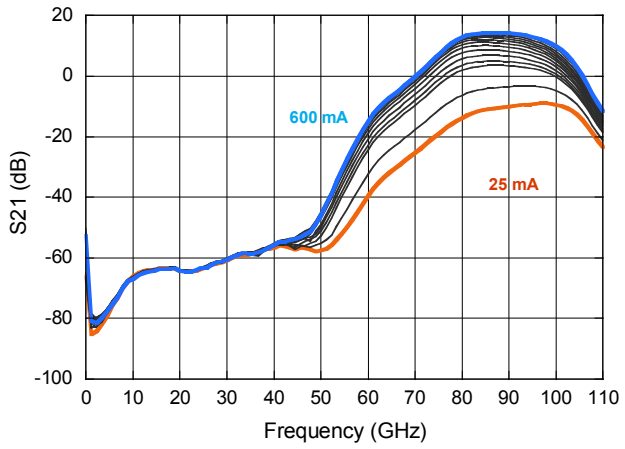
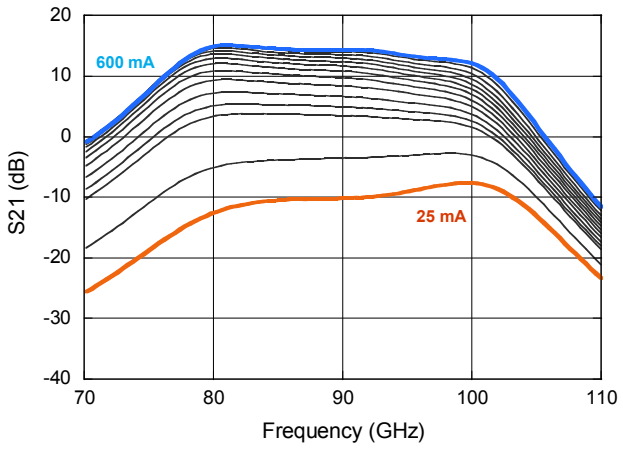
## Typical Performance Curves @ +85°C

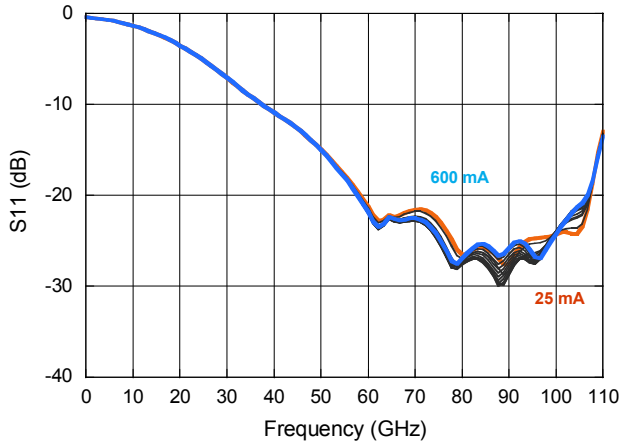
***Gain***



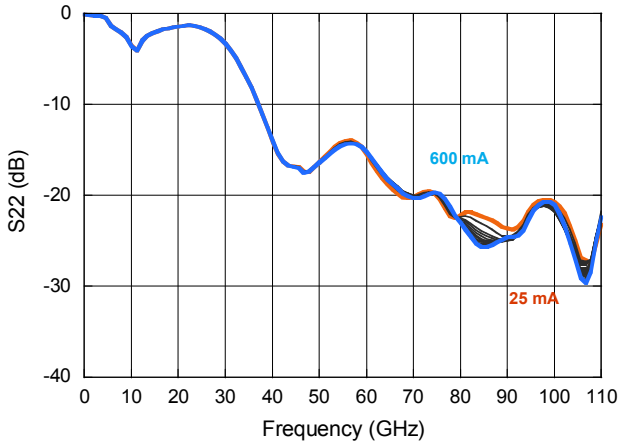

***Gain 70 - 110 GHz***



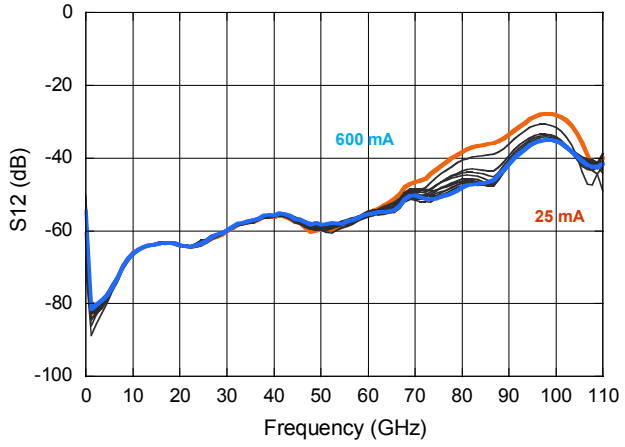

***Input Return Loss***




***Output Return Loss***



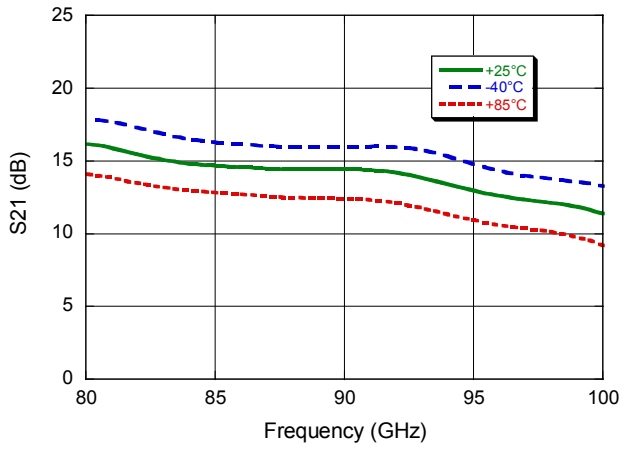

***Reverse Isolation***



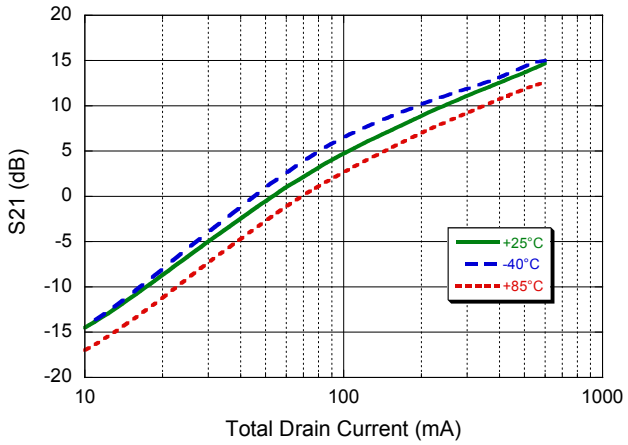

Preliminary Information

## Typical Performance Curves

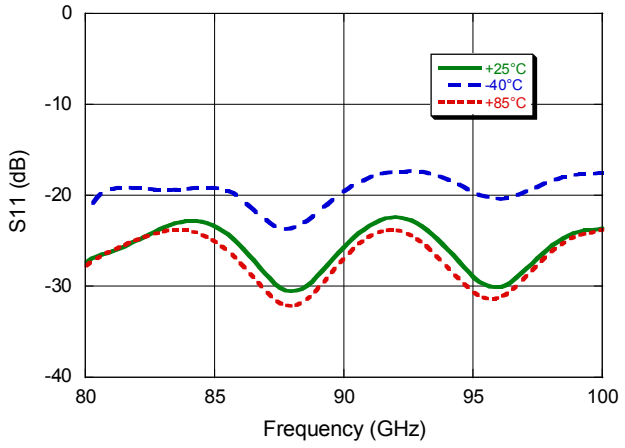
***Gain vs. Frequency @ 400 mA***



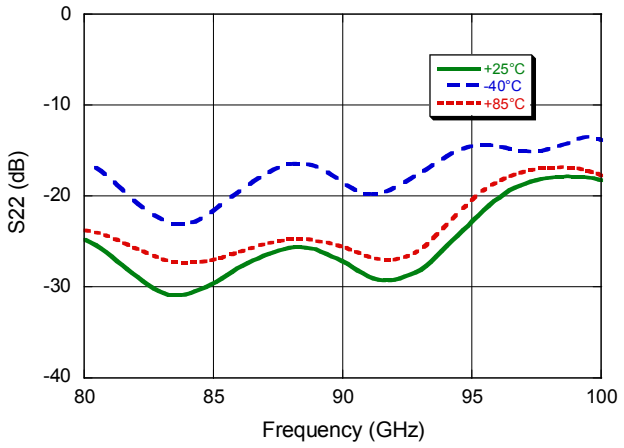

***Gain vs. Drain Current @ 94 GHz***



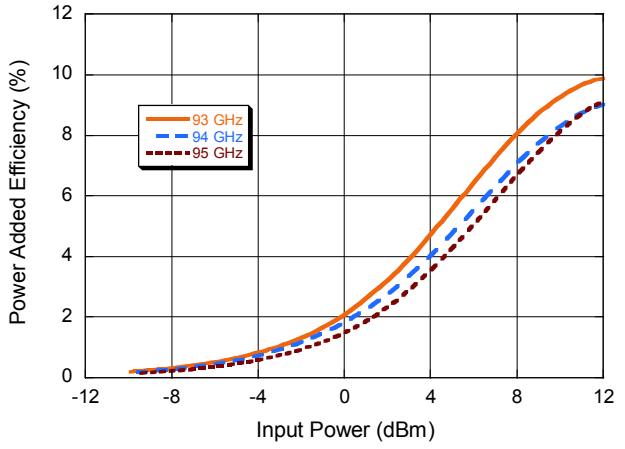

***Input Return Loss vs. Frequency @ 400 mA***



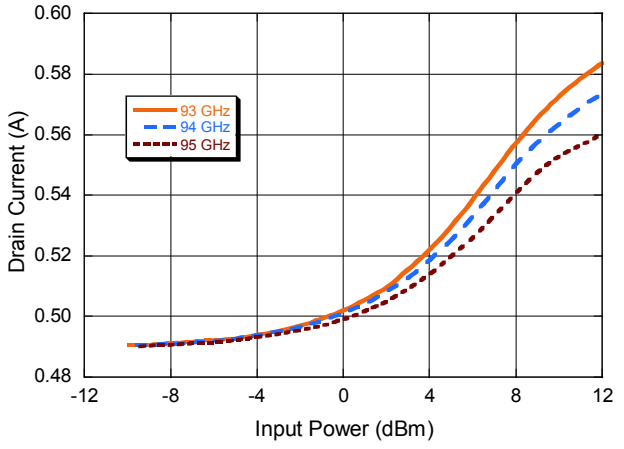

***Output Return Loss vs. Frequency @ 400 mA***




***PAE vs. Input Power***




***Drain Current vs. Input Power***

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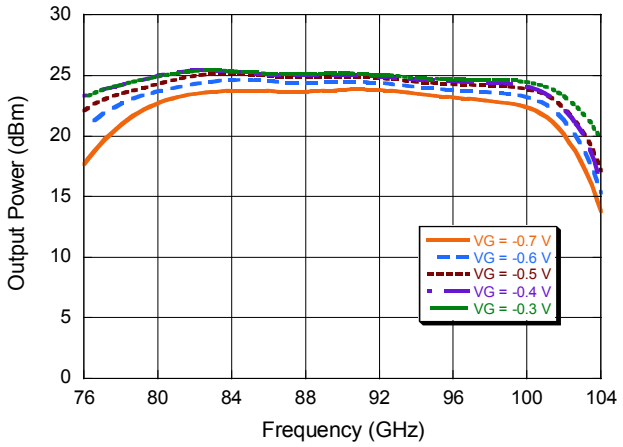
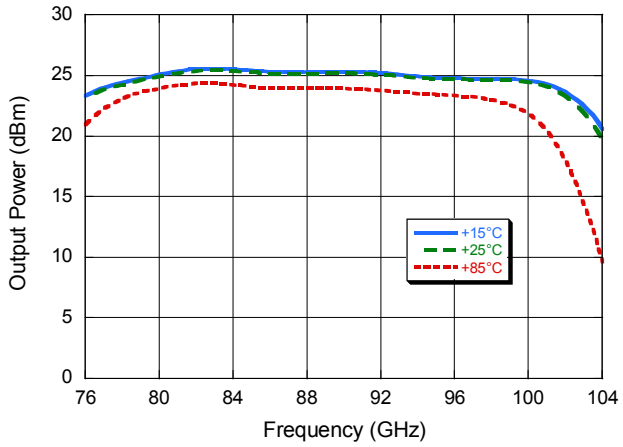
## Typical Performance Curves

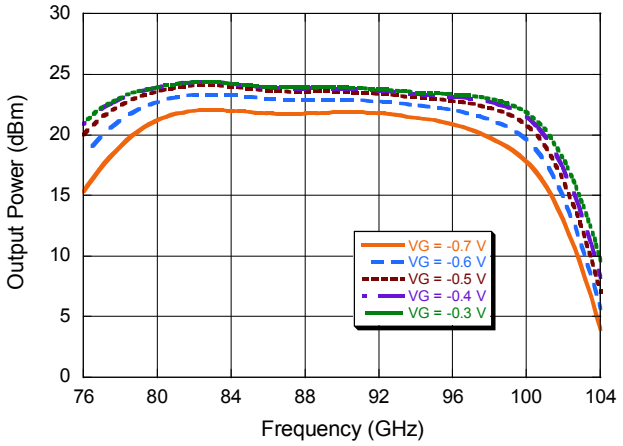
***$P_{SAT}$ vs. Frequency over Gate Voltage @ +25°C***



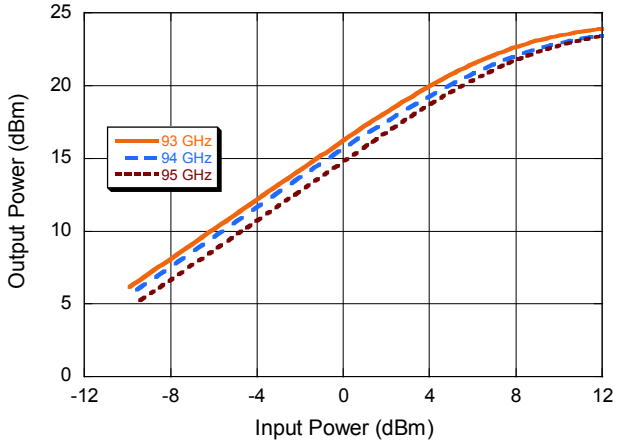

***$P_{SAT}$ vs. Frequency over Backside Temp. @ Vg = -0.3 V***



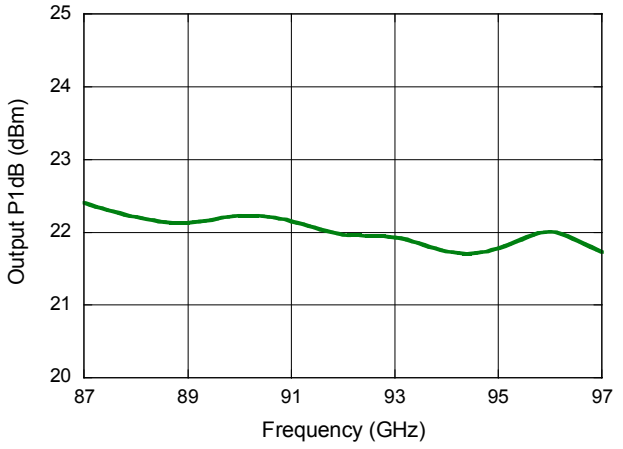

***$P_{SAT}$ vs. Frequency over Gate Voltage @ +85°C***




***Output Power vs. Input Power***




***Output P1dB vs. Frequency***

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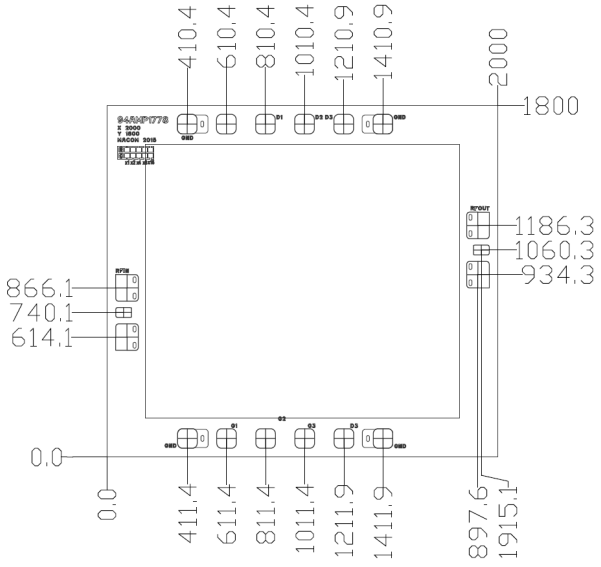
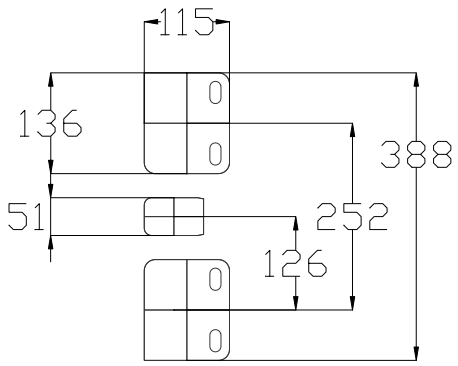
### *MMIC Bare Die*



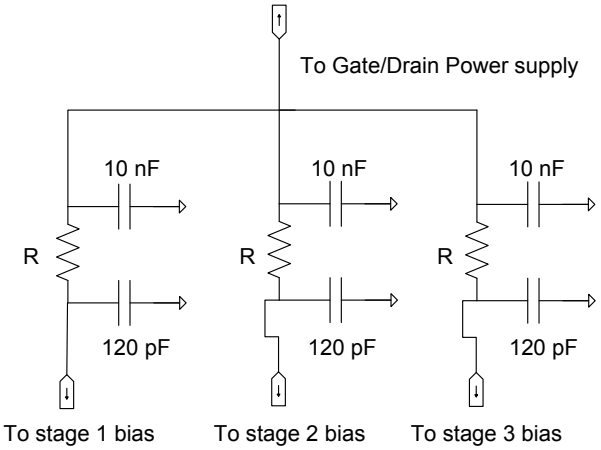

### *RF Probe*




**App Note [1] Biasing** -
All gates should be pinched-off ($V_G$ < -1 V) before applying drain voltage ($V_D$ = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is $V_D$ = 4 V, $I_D1$ = 100 mA, $I_D2$ = 100 mA, and $I_D3$ = 200 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

**App Note [2] Bias Arrangement** -
Each DC pin ($V_{D1}$, $V_{D2}$, $V_{D3A}$, $V_{D3B}$, and $V_{G1}$, $V_{G2}$, $V_{G3}$) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.

**App Note [3] Common Gates and Drains** -
When biasing the device with only a single gate or drain source additional isolation is required. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bias pass capacitance should still be applied to each stage as per App Note [2].

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