Power Amplifier, 3 W
21.15 - 23.65 GHz

MAAP-011146-DIE

Rev. V1

Features

- 25 dB Small Signal Gain
- 41 dBm Third Order Intercept Point (OIP3)
- >2 W Output P1dB
- 35.5 dBm Saturated Output Power
- Integrated Power Detector
- Bias 1330 mA @ 6 V
- RoHS* Compliant

Applications

- Point-to-Point

Description

The MAAP-011146-DIE is a power amplifier with a temperature compensated integrated power detector operating from 21.15 to 23.65 GHz. The circuit provides 25 dB gain, 41 dBm OIP3, 2 W P1dB and 35.5 dBm saturated output power.

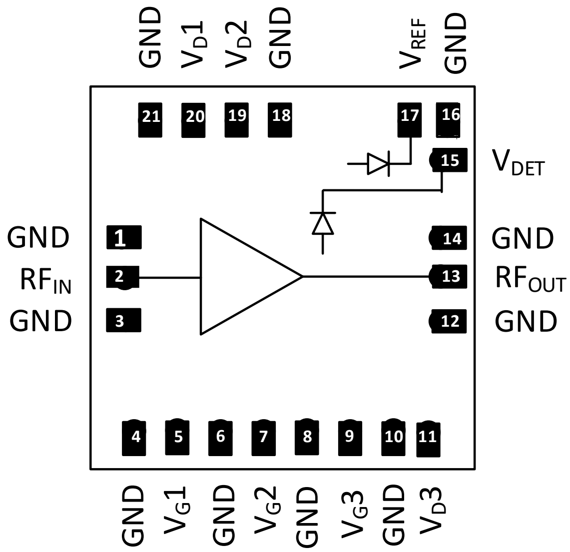
The device includes ESD protection and by-pass capacitors for ease of implementation and volume assembly.

This power amplifier is specifically designed for use in point-to-point radios for cellular backhaul applications in the 23 GHz band.

Ordering Information

Part Number	Package
MAAP-011146-DIE	Gel Pack
MAAP-011146-DIESMB	Sample Board

Functional Schematic



Pin Configuration[1]

Pin #	Function
1,3,4,6,8,10,12,14,16,18,21	Ground
2	RF Input
5	Gate 1 Bias
7	Gate 2 Bias
9	Gate 3 Bias
11	Drain 3 Bias
13	RF Output
15	Power Detector
17	Reference
19	Drain 2 Bias
20	Drain 1 Bias

1. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: V_{DD} = 6 V, I_{DQ}^{2} = 1330 mA, T_A = +25°C

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	21.7	25	—
P_{SAT} (RF & DC pulsed at 10% duty cycle)	dBm	34	35.5	—
Output IP3, +20 dBm SCL	dBm	—	41	—
Output IP3, +24 dBm SCL	dBm	—	39	—
P1dB	dBm	—	34	—
Input Return Loss	dB	—	15	—
Output Return Loss	dB	—	10	—
Detector V_{DIFF}, at Pin 0dBm	V	—	2.2	—
Noise Figure	dB	—	6	—
Gain Ripple over frequency	dB	—	2	—
Gate Voltage	V	—	—	-0.60

2. Adjust V_G1, V_G2 and V_G3 between -1.2 and -0.6 V to achieve specified I_{DQ} (I_{DQ} = I_D1+I_D2+I_D3). V_G1, V_G2 and V_G3 are nominally the same voltage.

Absolute Maximum Ratings[3,4,5]

Parameter	Rating
Input Power	18 dBm
Drain Voltage (V_D1,2,3)	7 V
Gate Voltage (V_G1,2,3)	-3 V
Drain to Gate Voltage (V_D-V_G)	10 V
Current (I_{DQ} = I_D1+I_D2+I_D3)	2800 mA
Detector Voltage (V_{DET})	6 V
Detector Reference (V_{REF})	6 V
Detector P_{OUT}	35 dBm
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq +175°C$ will ensure MTTF > 1 x 10^6 hours.

Maximum Operating Ratings[6,7]

Parameter	Rating
P_{DISS}	11.2 W
Input Power	15 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C

6. Channel temperature directly affects device MTTF. Chanel temperature should be kept as low as possible to maximize lifetime. Thermal resistance, Θjc, is 5.8°C/W.
7. For saturated performance, it is recommended that the sum of ($2V_{DD}$ + abs (V_{GG})) < 15 V.

Handling Procedures

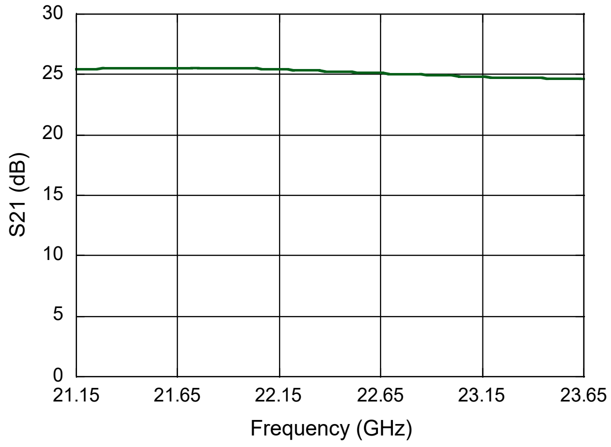
Please observe the following precautions to avoid damage:

Static Sensitivity

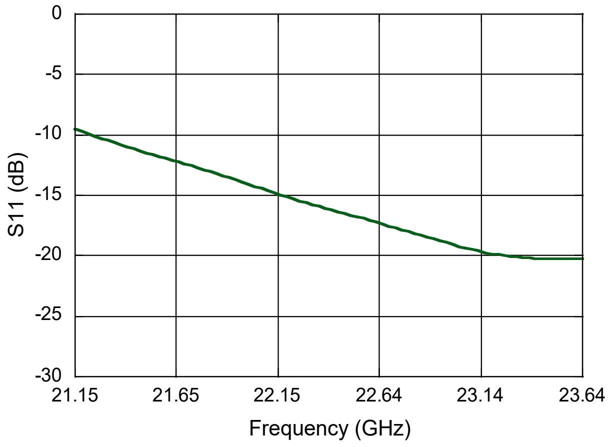
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these CDM class 2, HBM class 1B devices.

Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1330 mA

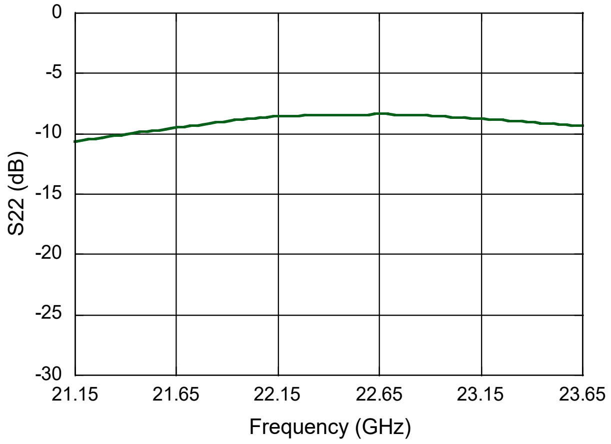
Small Signal Gain vs. Frequency



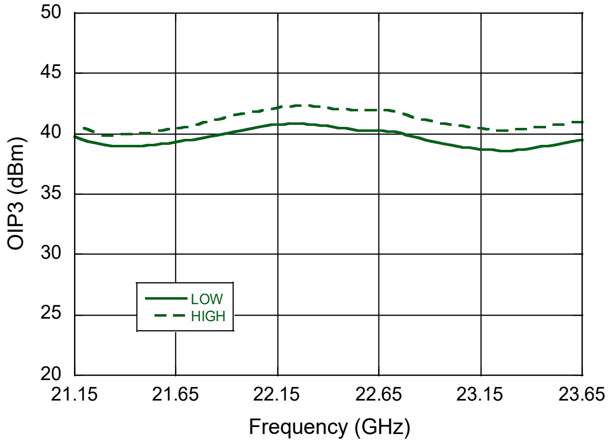
Input Return Loss vs. Frequency



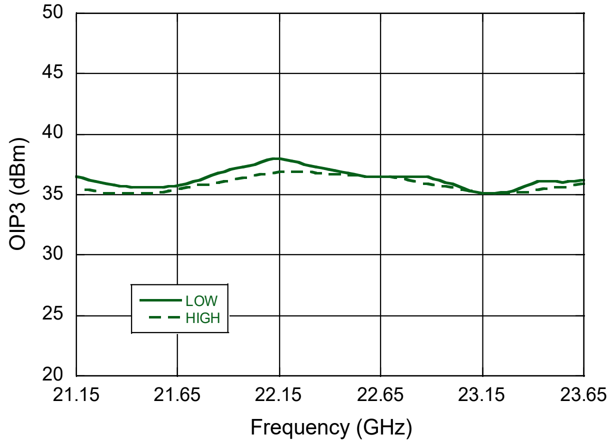
Output Return Loss vs. Frequency



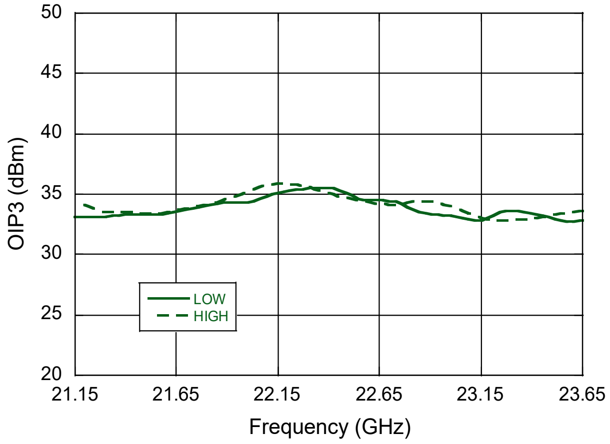
OIP3 @ -6 dBm RF_{IN} vs. Frequency



OIP5 @ -6 dBm RF_{IN} vs. Frequency

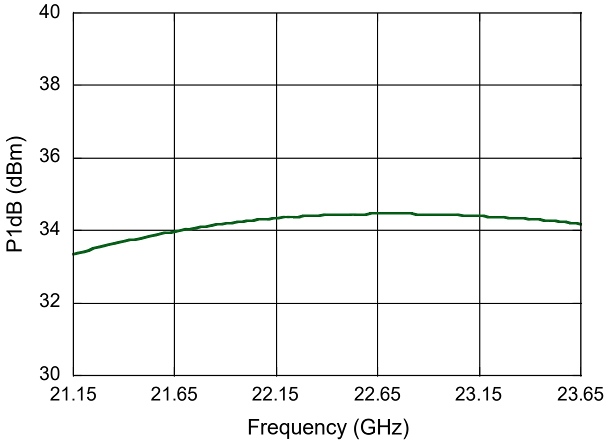


OIP7 @ -6 dBm RF_{IN} vs. Frequency

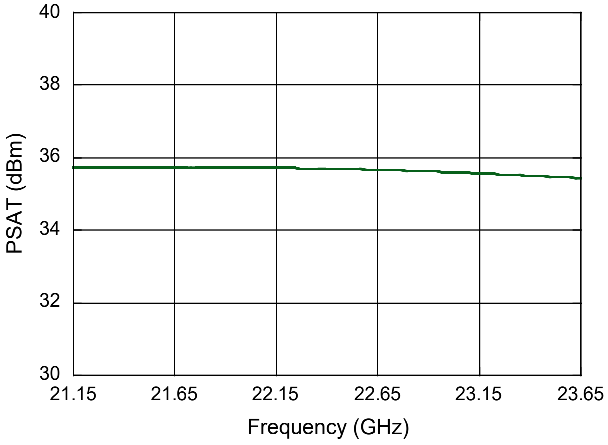


Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1330 mA

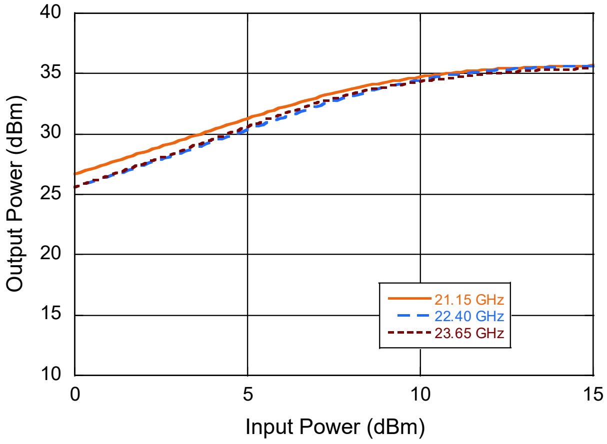
P1dB vs. Frequency



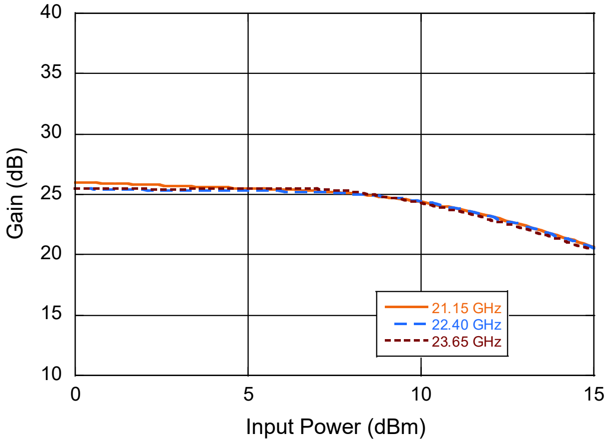
PSAT vs. Frequency



Pout vs. Input Power



Gain vs. Input Power



Biasing -

All gates should be pinched-off (V_G < -2 V) before applying drain voltage (V_D = 6 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is V_D = 6 V, I_D1 = 190 mA, I_D2 = 380 mA and I_D3 = 762 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

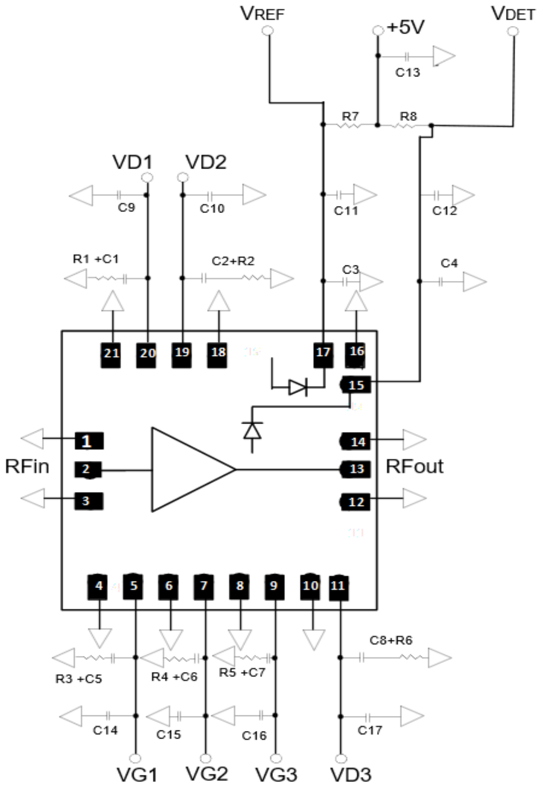
Bias Arrangement -

Recommended to use RC network on V_D1,2,3 and V_G1,2,3 close to the die pins. A 10 nF capacitor is also fitted at the drain and gate supply rails.

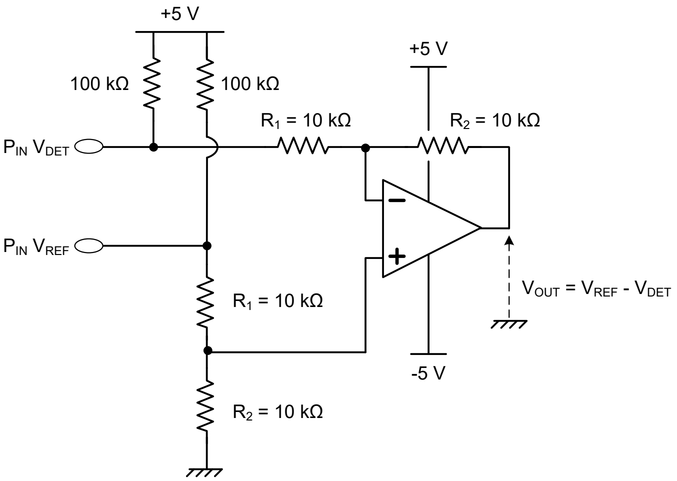
Power Detector -

As shown in the schematic below, the power detector is implemented by providing +5 V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

MMIC Schematic



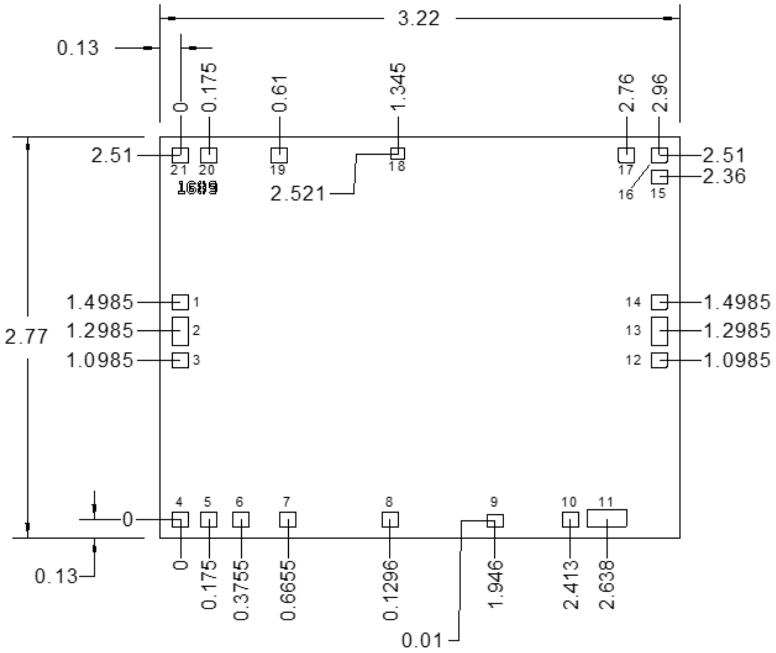
Power Detector Application Schematic



MMIC Parts List

Part	Value	Case Style
C1 - C8	120 pF	0402
C9 - C17	10 nF	0603
R1 - R6	10 Ω	0402
R7 - R8	100 kΩ	0402

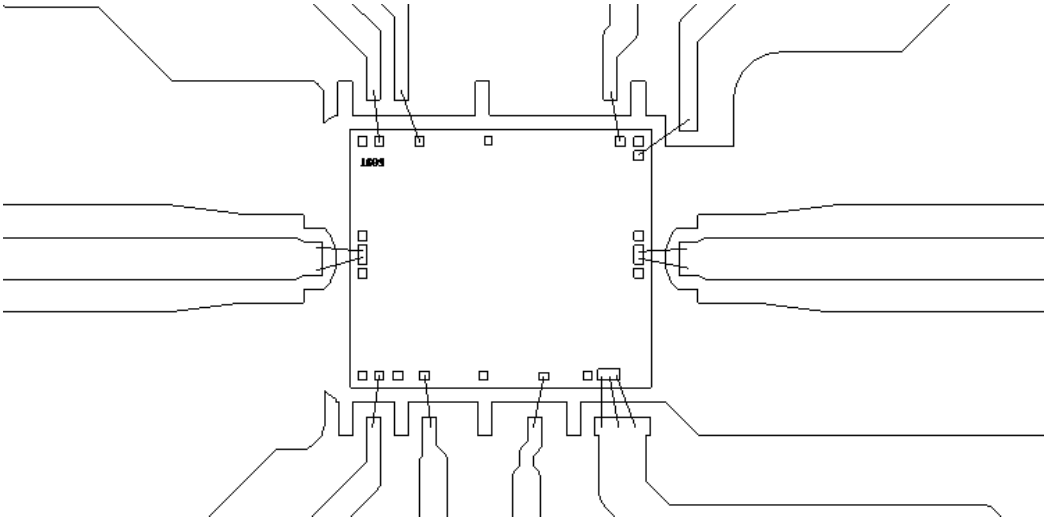
MMIC Die Layout



MMIC Die Dimensions (µm)

Bond Pad #	Bond Pad Name	Size X	Size Y
1,3,4,6,8,10, 12,14,16,21	GND	100	100
2	RFIN	100	200
5	VG1	100	100
7	VG2	100	100
9	VG3	100	80
11	VD3	240	120
13	RFOUT	100	200
15	VDET	100	100
17	VREF	100	100
18	GND	80	78
19	VD2	100	100
20	VD1	100	100

Recommended Bonding Diagram and PCB Details



Top/Bottom Layer: 1 oz. Copper, 44 µm +/-10 µm thickness
Dielectric Layer: Rogers RO4350B 254 µm thickness
ENEPIG Finish: 0.05 - 0.15 µm Au over 0.05 - 0.15 µm palladium over 3 - 6 µm nickel over copper.

Die Attach

Backside of die must be connected to RF, DC and thermal ground. Recommended high thermal and electrical performance epoxy is used for die attach.

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