MAAP-010517

Power Amplifier, 3 W
14.4 - 15.4 GHz

Rev. V4

Features

- 24 dB Small Signal Gain
- 42 dBm Third Order Intercept Point (OIP3)
- >3 W Output P1dB
- Integrated Power Detector
- Bias 1200 mA @ 6 V
- Lead-Free 5 mm 24-lead QFN Package
- RoHS* Compliant and 260°C Reflow Compatible

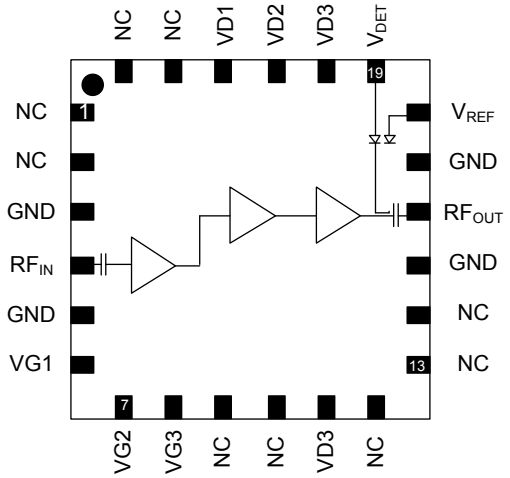
Description

The MAAP-010517 is a packaged linear power amplifier that operates from 14.4 - 15.4 GHz. The device provides 24 dB gain and 42 dBm Output Third Order Intercept Point (OIP3) with 34.5 dBm output P1dB.

The packaged amplifier comes in an industry standard, fully molded 5 mm QFN package and is comprised of a three stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part.

The device is specifically designed for use in 15 GHz point-to-point radios for cellular backhaul applications.

Functional Schematic



Pin Configuration [2]

Pin #	Function	Pin #	Function
1,2	No Connection	15	Ground
3	Ground	16	RF Output
4	RF Input	17	Ground
5	Ground	18	Pwr Det Ref
6	Gate 1 Bias	19	Pwr Det
7	Gate 2 Bias	20[2]	Drain 3 Bias
8	Gate 3 Bias	21	Drain 2 Bias
9,10	No Connection	22	Drain 1 Bias
11[2]	Drain 3 Bias	23,24	No Connection
12,13,14	No Connection	25[3]	Paddle

2. Drain 3 Bias can be connected from either pins 11 or 20
3. The exposed pad centered on the package bottom must be connected to RF and DC ground.

Ordering Information[1]

Part Number	Package
MAAP-010517-TR0500	500 piece reel
MAAP-010517-001SMB	evaluation module

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications[4]:

Freq. = 14.4 - 15.4 GHz, I_{DQ}[5] = 1200 mA, V_{DET} Bias = 5 V[6], V_D = 6 V, T_A = +25°C

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	21	24	—
Input Return Loss	dB	—	11	—
Output Return Loss	dB	—	11	—
Noise Figure	dB	—	7	—
P1dB	dBm	—	34.5	—
P_{SAT}	dBm	34.0	35.5	—
Output IP3, 20 dBm SCL	dBm	39	42	—

4. It is recommended to use active bias on gate voltages to keep the drain currents constant in order to maintain the best performance over temperature.
5. Adjust V_G1,V_G2 and V_G3 between -1.2 and -0.1 V to achieve specified I_{DQ} (I_{DQ}=I_D1+I_D2+I_D3). V_G1,V_G2 and V_G3 should be the same voltage.
6. See page 3 for schematic on how to connect V_{DET} and V_{REF} pins.

Maximum Operating Ratings[7,8,9]

Parameter	Absolute Maximum
Input Power	18 dBm
Drain Supply Voltage	7 V
Junction Temperature[10]	+160°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

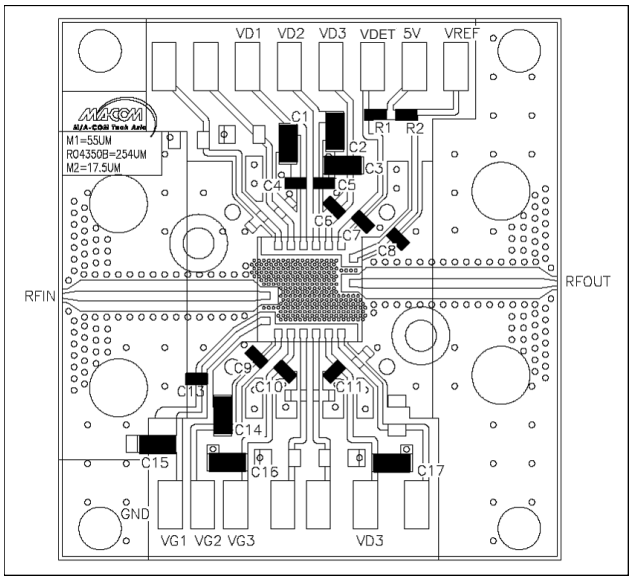
7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Operating at nominal conditions with $T_J \leq 160°C$ will ensure MTTF > 1 x 10^6 hours.
10. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
    Typical thermal resistance (Θ_{JC}) = 7.9°C/W
    a) For T_C = +25°C,
    T_J = 88°C @ 6 V, 1.8 A, P_{OUT} = 34.5 dBm, P_{IN} = 11.5 dBm
    b) For T_C = +85°C,
    T_J = 143°C @ 6 V, 1.7 A, P_{OUT} = 34.5 dBm, P_{IN} = 11.5 dBm

Absolute Maximum Ratings[11,12]

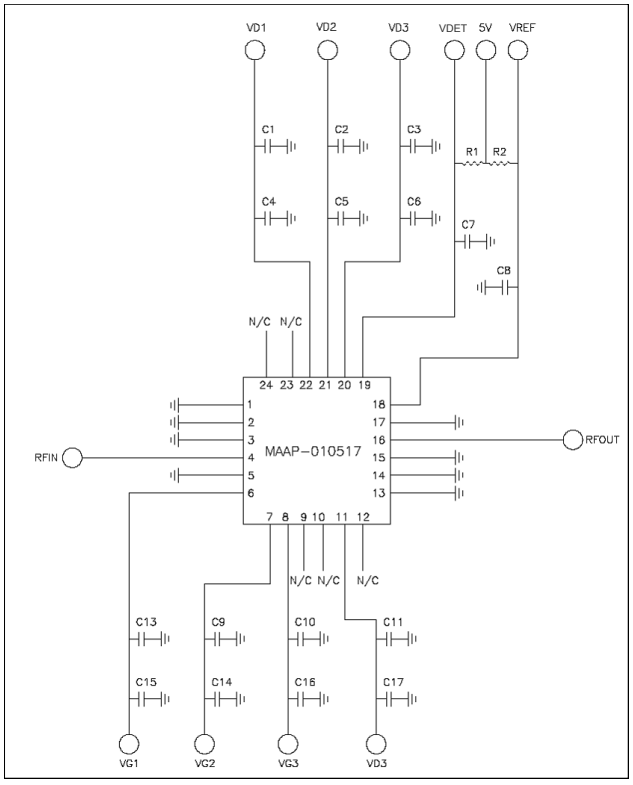
Parameter	Absolute Maximum
Supply Gate Voltage	-3 V
Supply Current	2200 mA
Drain to Gate Voltage	10 V
Continuous Power Dissipation @ +85ºC	11.3 W
Junction Temperature	+175ºC

11. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
12. For saturated performance it is recommended that the sum of (2*V_{DD} + abs(V_{GG})) <14 V.

Recommended PCB Layout



Schematic



Parts List

Component	Value	Package
C1,C2,C3,C14, C15,C16,C17	2.2 µF	0603
C4,C5,C6,C7,C8, C9,C10,C11,C13	1000 pF	0402
R1	100 KΩ	0402
R2	91 KΩ	0402

Handling Procedures

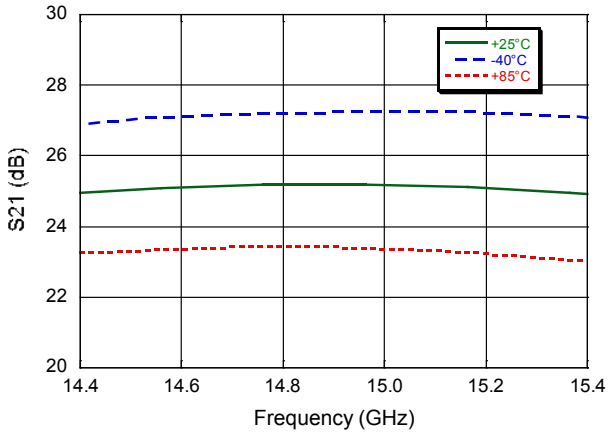
Please observe the following precautions to avoid damage:

Static Sensitivity

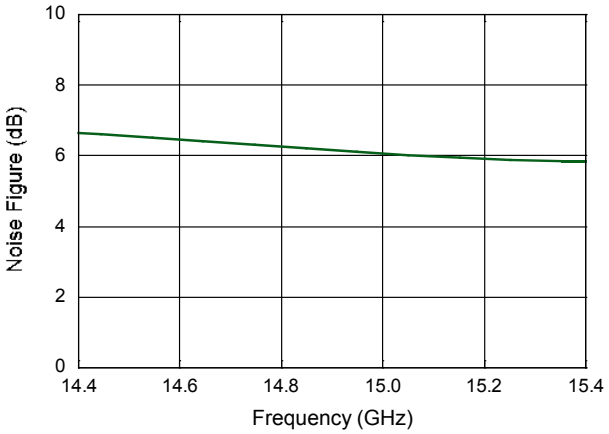
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A devices.

Typical Performance Curves

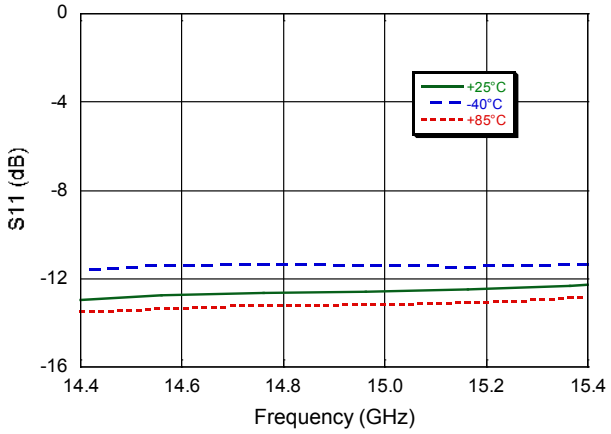
Gain



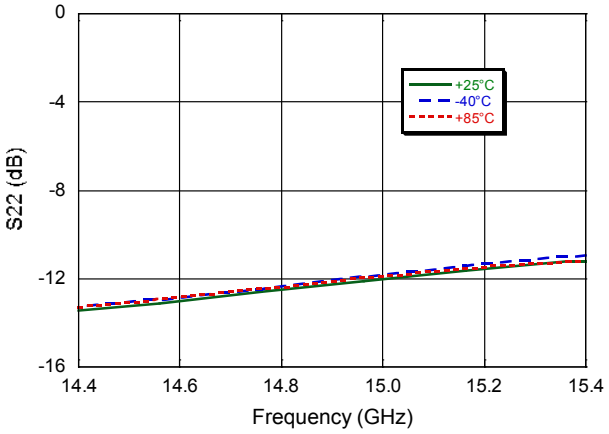
Noise Figure



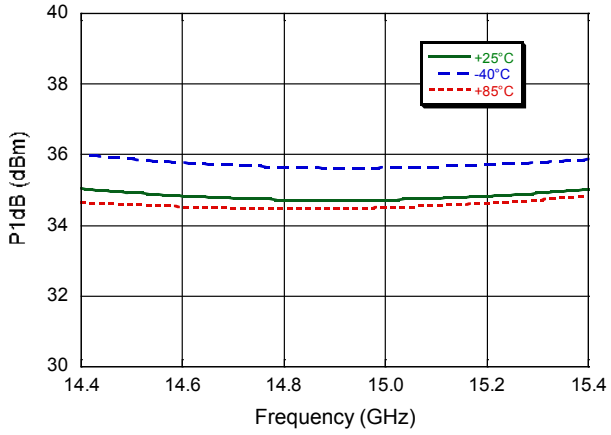
Input Return Loss



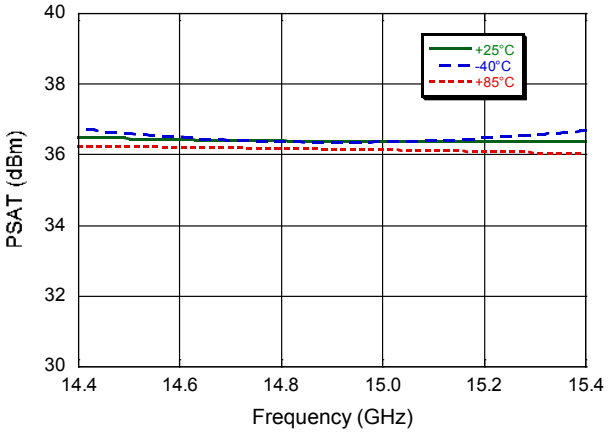
Output Return Loss



P1dB

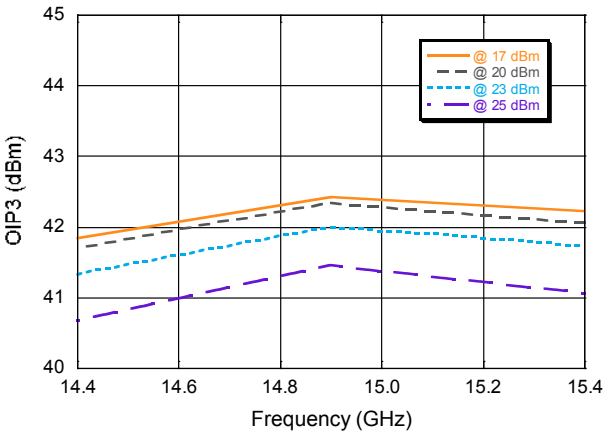


PSAT

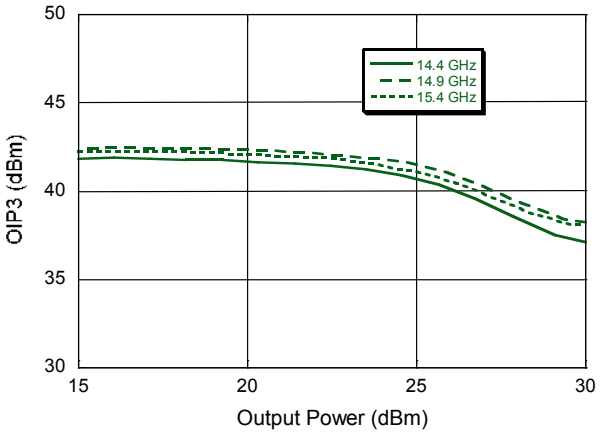


Typical Performance Curves

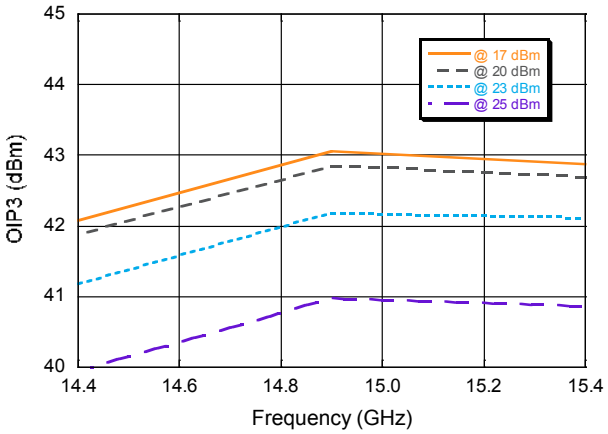
Output IP3 @ +25°C



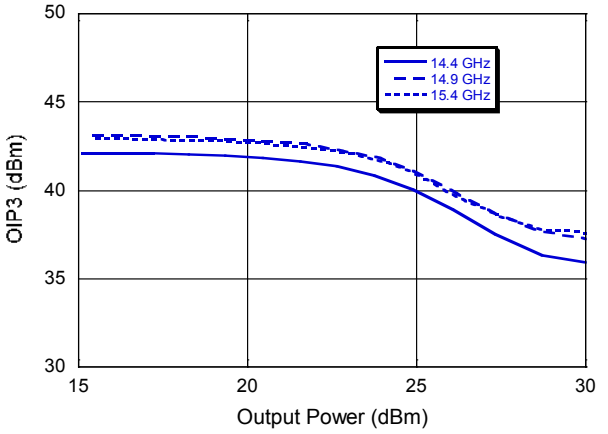
Output IP3 @ +25°C



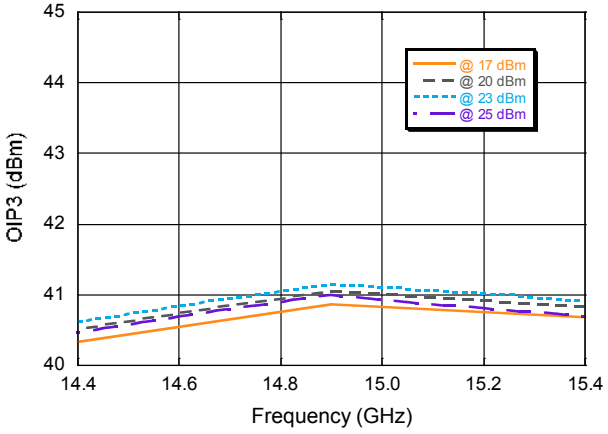
Output IP3 @ -40°C



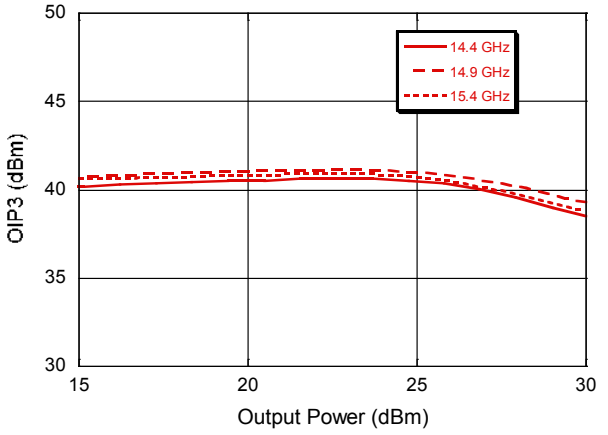
Output IP3 @ -40°C



Output IP3 @ +85°C

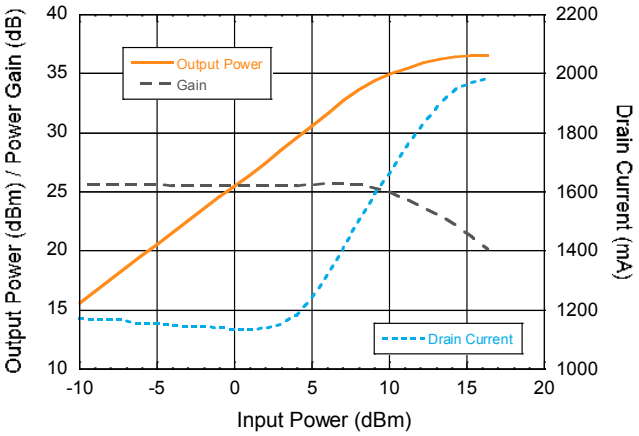


Output IP3 @ +85°C

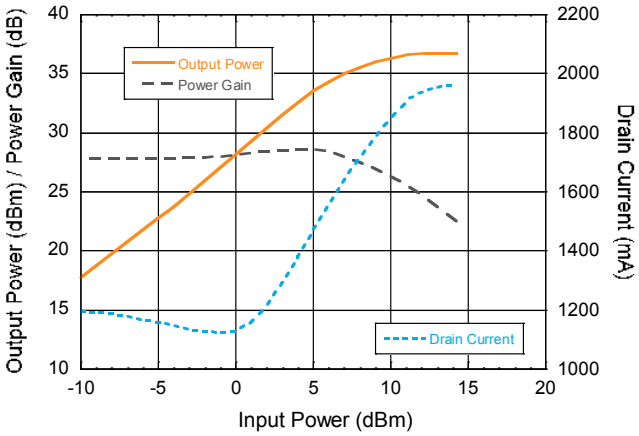


Typical Performance Curves

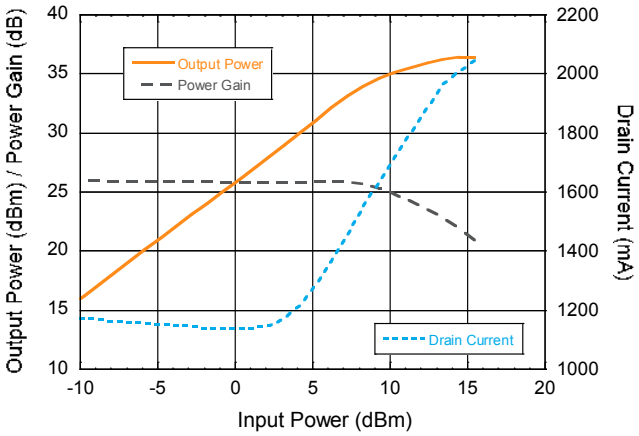
Power Data @ 14.4 GHz, +25°C



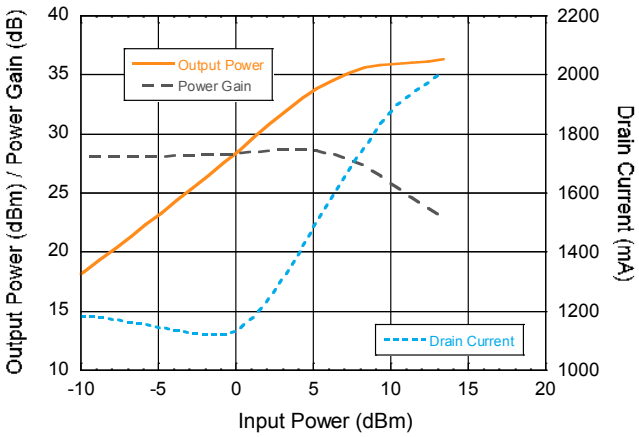
Power Data @ 14.4 GHz, -40°C



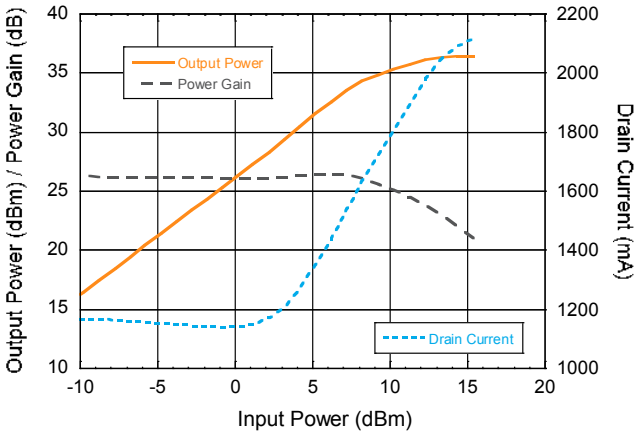
Power Data @ 14.9 GHz, +25°C



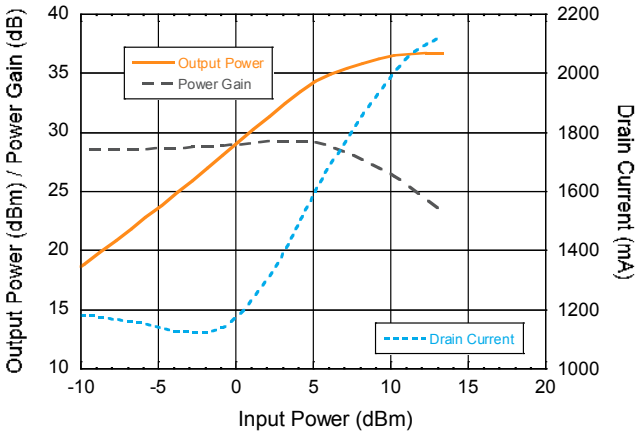
Power Data @ 14.9 GHz, -40°C



Power Data @ 15.4 GHz, +25°C

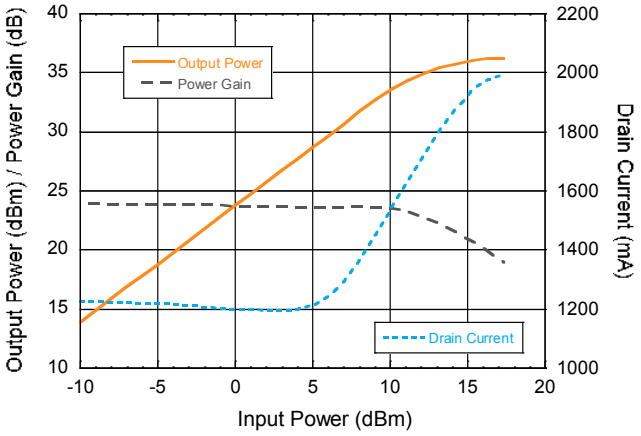


Power Data @ 15.4 GHz, -40°C

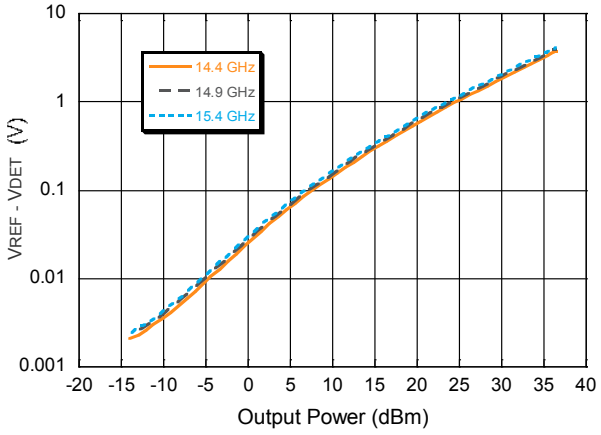


Typical Performance Curves

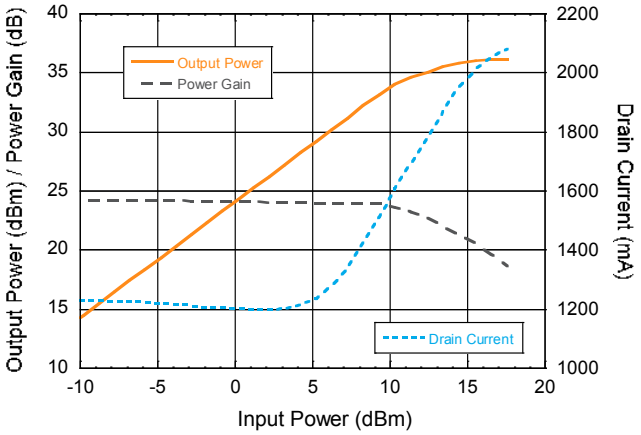
Power Data @ 14.4 GHz, +85°C



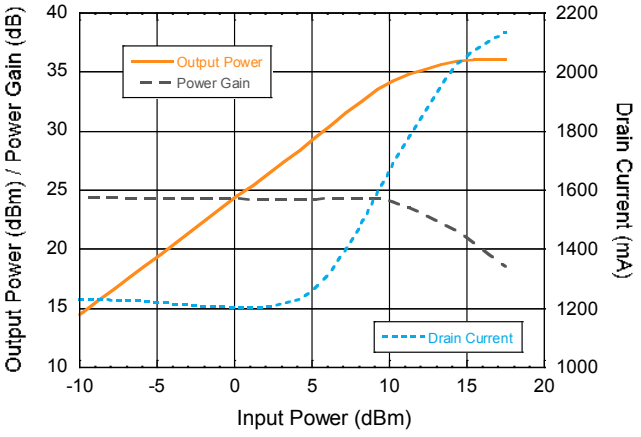
Detected Voltage (V_{REF} - V_{DET}) @ +25°C



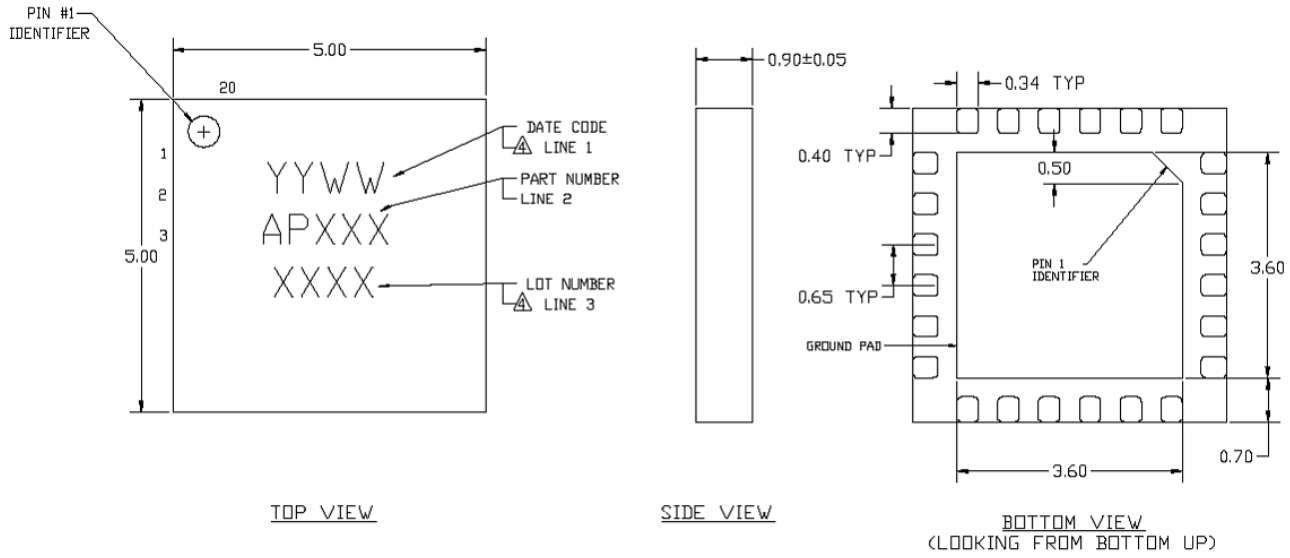
Power Data @ 14.9 GHz, +85°C



Power Data @ 15.4 GHz, +85°C



Lead-Free 5 mm 24-lead PQFN



(All Dimensions are in millimeters)

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is matte tin over Copper.