

Wideband Distributed Amplifier

100 kHz - 50 GHz



MAAM-011231-DIE

Rev. V1

Features

- Gain: 15 dB @ 6 V, 30 GHz
- P1dB: +17 dBm @ 6 V, 30 GHz
- P3dB: +18 dBm @ 6 V, 30 GHz
- Integrated Power Detector
- Gain Control with Only Positive Bias Voltages
- 50 Ω Input and Output Match
- Bias Voltage: $V_{DD} = +6 V$
- Bias Current: $I_{DSQ} = 165 mA$
- Die size: 2.1 x 1.05 x 0.1 mm
- RoHS* Compliant

Applications

- Instrumentation & Communication
- EW
- ECM
- Test and Measurement

Description

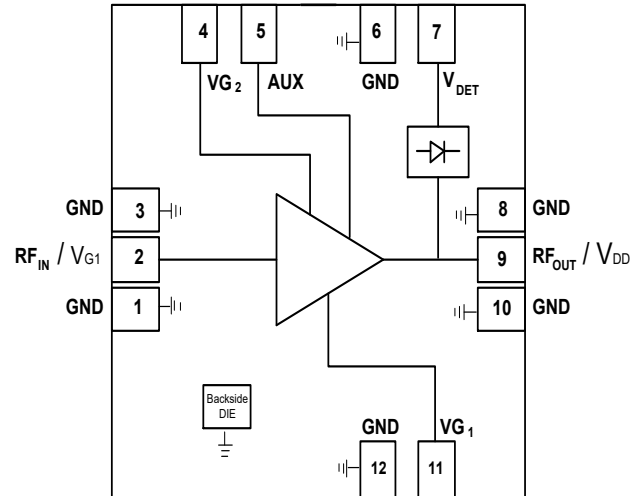
MAAM-011231-DIE is an easy-to-use, wideband amplifier that operates from 100 kHz to 50 GHz. The amplifier provides 15 dB gain, 4.5 dB noise figure and 20 dBm of P3dB output power @ 30 GHz. It is matched to 50 Ω with typical return loss better than 12 dB. The amplifier requires only positive bias voltages and would typically be operated at 6 V and 165 mA.

MAAM-011231-DIE is suitable for a wide range of applications in instrumentation and communication systems.

Ordering Information

Part Number	Package
MAAM-011231-DIE	Die in Gel Pak

Functional Schematic



Pad Configuration¹

Pin #	Pin Name	Description
1,3,6,8,10,12	GND	Ground
2	RF _{IN}	RF Input / Gate Voltage
4	V _{G2}	Gate Voltage 2
5	AUX	Auxiliary Drain Voltage
7	V _{DET}	Detector Voltage
9	RF _{OUT}	RF Output / Drain Voltage
11	V _{G1}	Gate Voltage 1
Backside	-	Note ¹

1. The backside of the die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: $T_C = +25^\circ\text{C}$, $V_D = 6\text{ V}$, $I_{DQ} = 175\text{ mA}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	0.0001 - 10 GHz	dB	13.5	15.0	—
	10 - 20 GHz		13.5	15.0	
	20 - 30 GHz		14.0	15.5	
	30 - 40 GHz		14.5	16.0	
	40 - 50 GHz		15.0	16.5	
Noise Figure	2.8 - 10 GHz	dB	—	5.0	—
	10 - 20 GHz			3.0	
	20 - 30 GHz			3.0	
	30 - 40 GHz			3.5	
	40 - 50 GHz			4.5	
Input Return Loss	0.0001 - 10 GHz	dB	—	17.0	—
	10 - 20 GHz			20.0	
	20 - 30 GHz			13.0	
	30 - 40 GHz			12.0	
	40 - 50 GHz			10.0	
Output Return Loss	0.0001 - 10 GHz	dB	—	17.0	—
	10 - 20 GHz			15.0	
	20 - 30 GHz			13.0	
	30 - 40 GHz			13.5	
	40 - 50 GHz			12.0	
P1dB	40 GHz	dBm	13.5	15.0	—
P3dB	0.0001 - 10 GHz	dBm	—	22.0	—
	10 - 20 GHz			21.0	
	20 - 30 GHz			18.0	
	30 - 40 GHz			17.5	
	40 - 50 GHz			15.0	
Output IP3	@ 11MHz tone spacing	dBm	—	29.0	—
	0.0001 - 10 GHz			30.0	
	10 - 20 GHz			29.0	
	20 - 30 GHz			28.0	
	30 - 40 GHz			24.0	

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Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	0.0001 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dB	—	15.0 15.0 16.0 17.0 17.5	—
Noise Figure	2.8 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dB	—	5.0 3.0 3.0 3.5 4.5	—
Input Return Loss	0.0001 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dB	—	17.0 17.0 17.0 15.0 12.0	—
Output Return Loss	0.0001 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dB	—	17.0 20.0 13.0 12.0 10.0	—
P1dB	40 GHz	dBm	—	15	—
P3dB	0.0001 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dBm	—	20.0 19.0 18.0 17.0 14.0	—
Output IP3	@ 11 MHz tone spacing 0.0001 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dBm	—	27.0 28.0 27.0 26.5 25.0	—

Operational Maximum Ratings

Parameter	Absolute Maximum
Input Power (CW)	+5 dBm
Drain Supply Voltage	7 V
Junction Temperature ^{3,4}	+150°C
Operating Temperature	-40°C to +85°C

- Operating at nominal conditions with $T_J \leq +150^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.
- Junction Temperature (T_J) = $T_A + \theta_{JC} * ((V * I) - (P_{OUT} - P_{IN}))$
 Typical thermal resistance (θ_{JC}) = 22 °C/W.
 For $T_A = +85^\circ\text{C}$,
 $T_J = +103^\circ\text{C}$ at $V = 6\text{ V}$, $I = 0.165\text{ A}$

Recommended Operating Conditions

It is recommended to operate at a typical drain voltage of +6 V ± 5 %. The maximum recommended operating drain current is fundamentally defined by the combination of the maximum operating junction temperature and the power dissipated. This can be calculated as shown in note 4.

Absolute Maximum Ratings^{5,6}

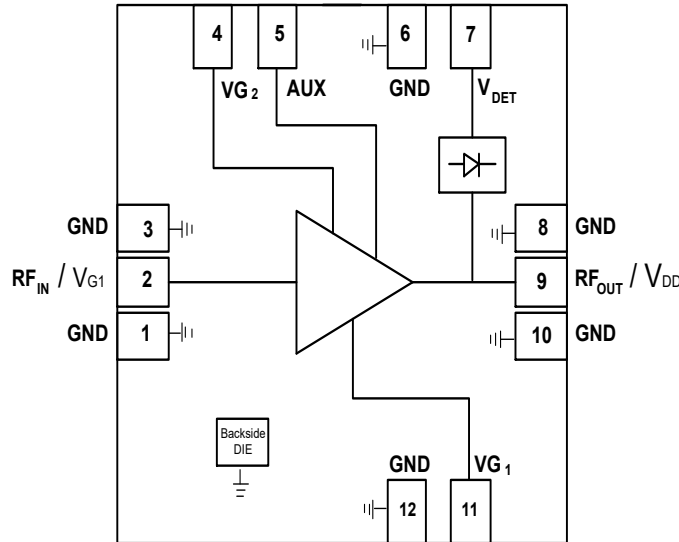
Parameter	Absolute Maximum
Input Power (CW)	+25 dBm
Drain Supply Voltage	8 V
Junction Temperature ^{5,6}	+175°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.

Electrostatic Sensitivity

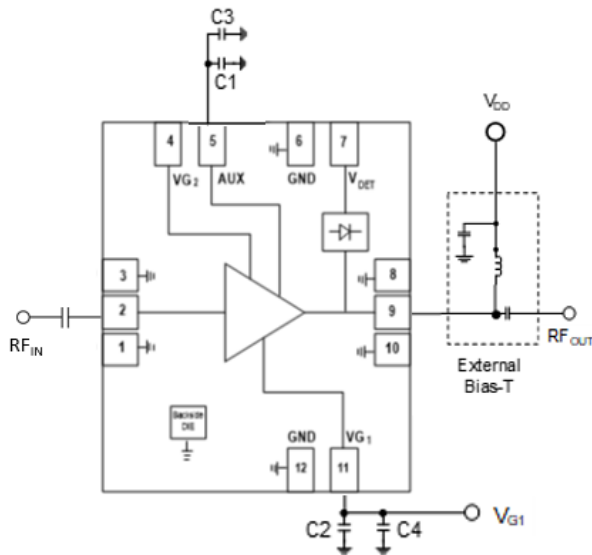
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 1B HBM and class C3 CDM devices.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1,3,6,8,10,12	GND	These pads are grounded on the MMIC
2	RF _{IN}	RF Signal Input / V _{G1} . This pad is matched to 50 Ω and is DC coupled to allows application of the gate voltage through this pad when a suitable bias tee is used. If the gate voltage is applied using pad 11, a suitable external DC blocking capacitor should be used on the RF input line as the applied gate voltage will be present on this pad.
4	V _{G2}	Gate Voltage 2. This pad allows the gain to be dynamically controlled when operating in the linear gain region through the application of 0 to 1.6 V to V _{G2} . For normal operation, this pad can be left unconnected.
5	AUX	Auxiliary drain connection. To improve the low frequency response 2 bypass capacitors of 1200 pF and 10 μF will improve the frequency of operation down to 100 kHz. These capacitors should be positioned as close to the device as possible.
7	V _{DET}	Temperature compensated power detector output voltage. This provides a voltage which is proportional to the output power of the amplifier.
9	RF _{OUT}	RF Signal Output / V _{DD} . This pad is matched to 50 Ω and is DC coupled to allow application of the drain bias through this pad when a suitable bias tee is used.
11	V _{G1}	Gate Voltage 1. Adjust V _G from 0 V to 1.6 V to achieve the desired quiescent current. External bypass capacitors and de-Q resistors are required as described in the applications section.
Backside	NC	The backside of the die must be connected to RF, DC and thermal ground. For recommended die attach materials see the applications section.

Application Schematic



Component List

Part	Value	Size	Part Number
C1, C2	1200 pF	25 mil	TECDIA SKT03C122V12A6
C3, C4	10 μ F	0603	any

Biasing Conditions

The typical biasing condition is $V_{DD} = 6$ V, $I_{DSQ} = 165$ mA (controlled with V_{G1}). The gate voltage can be applied in two ways: direct application to V_{G1} (pin 11), or alternatively through the RF input using a suitable bias tee on the RF input line. If a bias tee is not used on the RF input, a DC blocking capacitor is required on the RF input line to stop the gate voltage being imposed on the RF input line.

V_{DD} is applied at the RF_{OUT}/V_{DD} pad and requires the use of a suitable bias tee which can support both the bandwidth and drain current requirements of the MMIC. This configuration provides wide band performance of 40 MHz - 50 GHz (depending on the bandwidth of the bias tee).

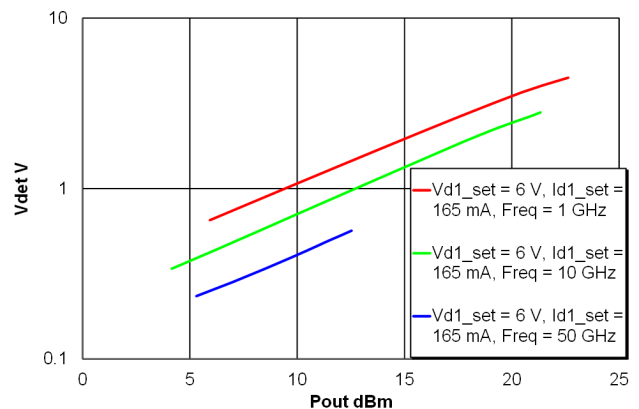
For low frequency operation below 40MHz the addition of 2 bypass capacitors on V_{G1} and AUX of 1200 pF and 10 μ F will improve the frequency response down to 100 kHz. These capacitors should be positioned as close to the device as possible.

Dynamic Gain Control

Dynamic gain control is available when operating in the linear gain region through the application of 0 to 1.6 V to V_{G2} . If not being used, this pad can be left unconnected.

Integrated Power Detector

The MAAM-011231-DIE has an integrated power detector. For ease of use and to minimize external componentry, the power detector output is internally temperature compensated. A typical response is shown below.



Operating the MAAM-011231-DIE

Turn-on

1. Apply V_{G1} to 0 V.
2. Apply V_{DD} to 6 V.
3. Set I_{DSQ} by adjusting V_{G1} more positive. (typically 0.65 V for $I_{DSQ} = 165$ mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_{G1} to 0 V.
3. Decrease V_{DD} to 0 V.

Handling the Die

This MMIC has a coating to protect the airbridges on its surface which allows the use of a vacuum collet. However, do not touch the surface of the chip with tweezers, or fingers.

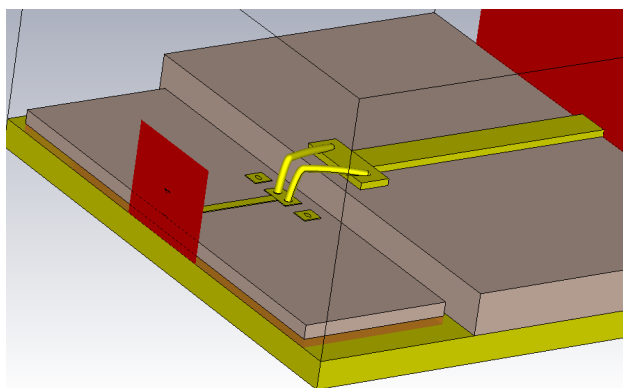
Die Attach

For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used. If using eutectic, an 80% Au / 20% Sn preform is recommended.

Wire Bonding

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25 μm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 μm . Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below.

Alternatively, a 3 mil bond ribbon could be used.



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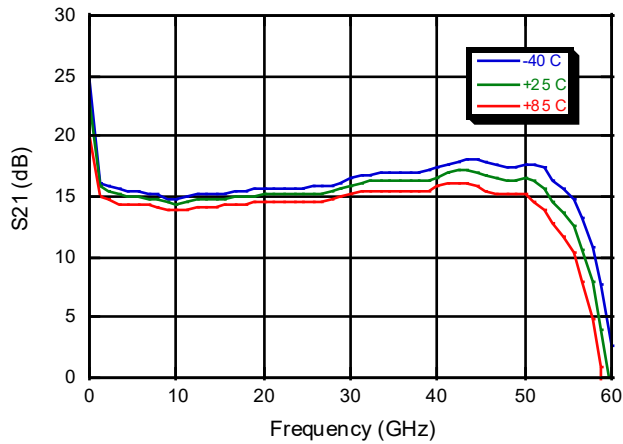


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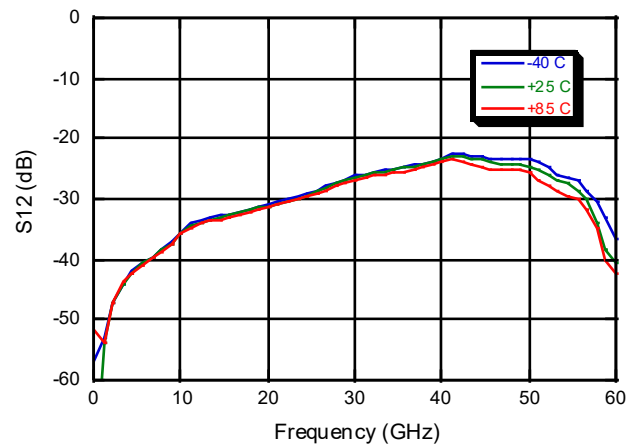
Rev. V1

Typical Performance at $V_D = 6\text{ V}$, $I_D = 175\text{ mA}$

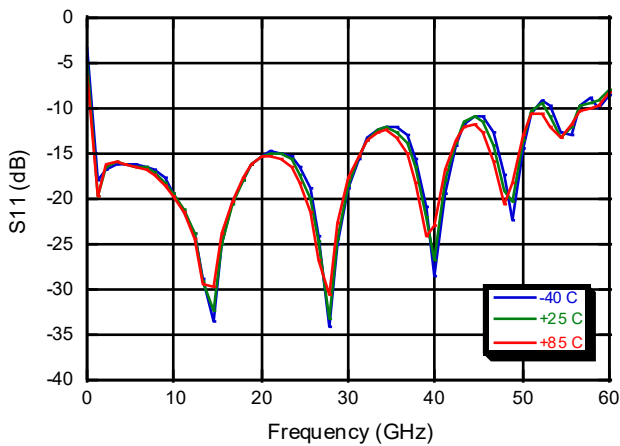
Gain



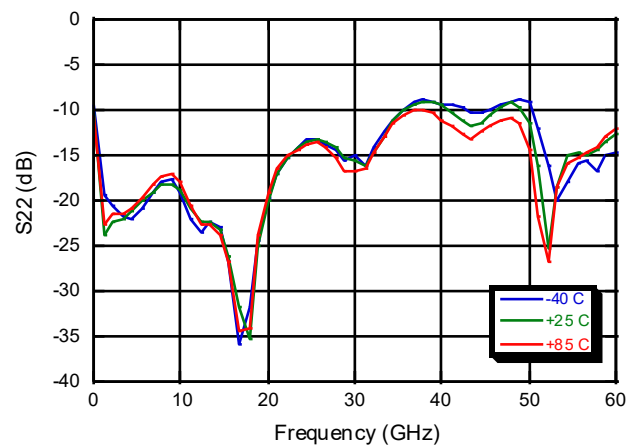
Reverse Isolation



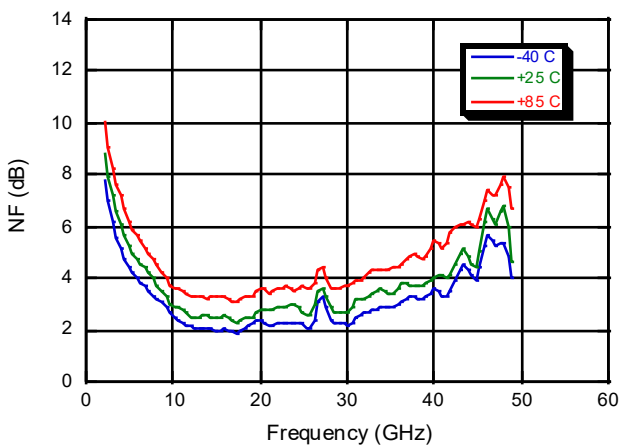
Input Return Loss



Output Return Loss



Noise Figure



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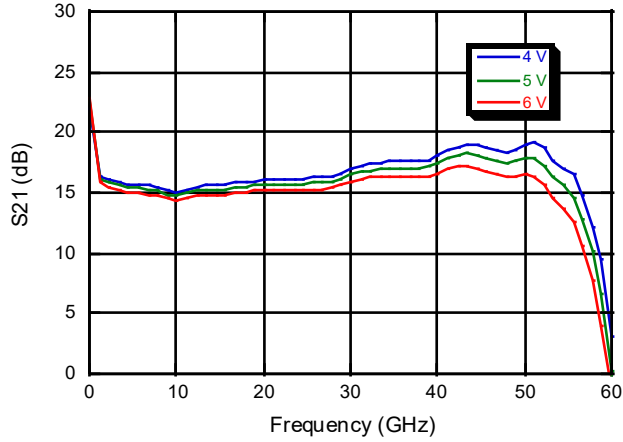


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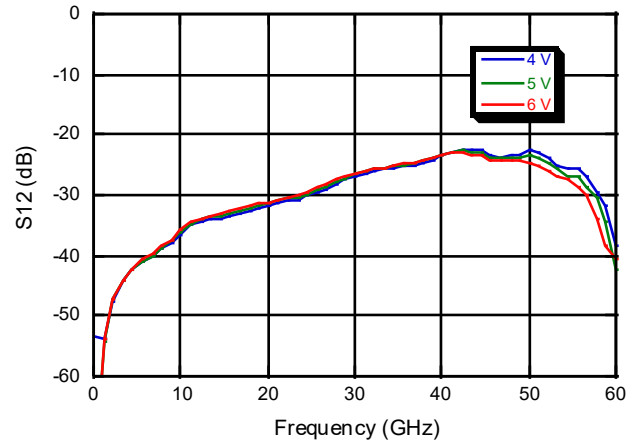
Rev. V1

Typical Performance at $I_D = 175 \text{ mA}$, $T_A = 25^\circ\text{C}$

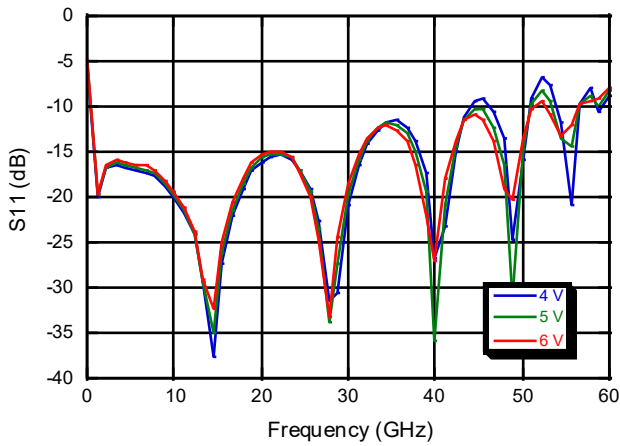
Gain



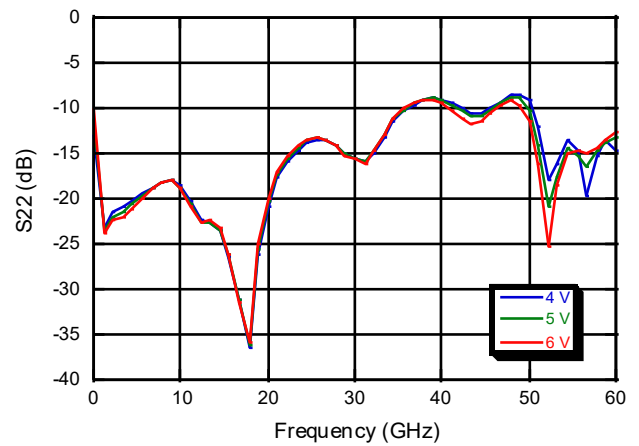
Reverse Isolation



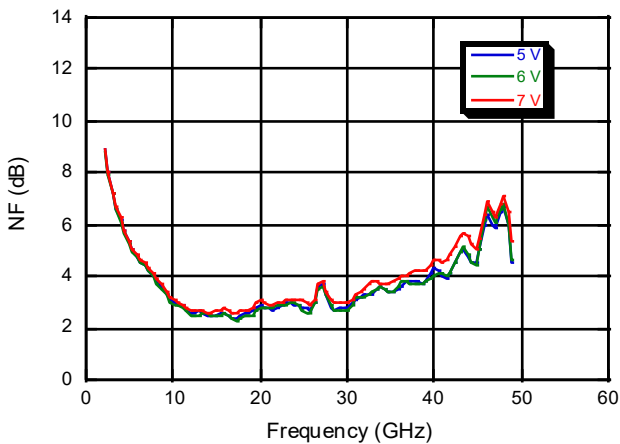
Input Return Loss



Output Return Loss



Noise Figure



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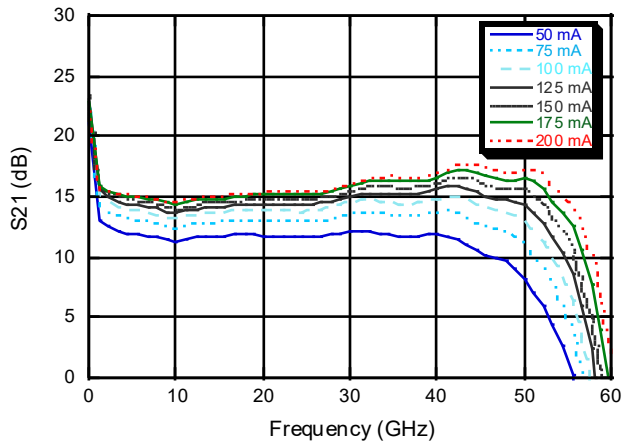


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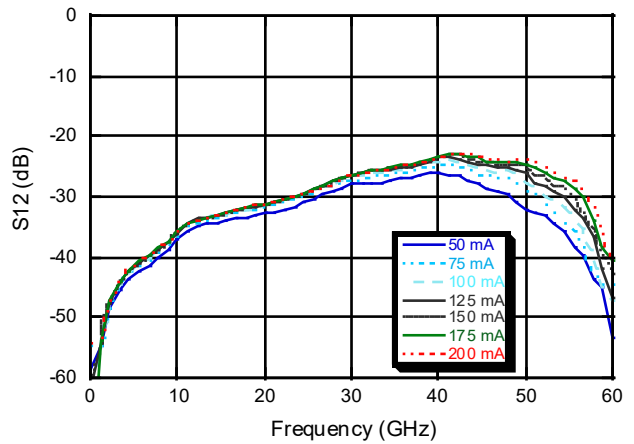
Rev. V1

Typical Performance at $V_D = 6\text{ V}$, $T_{AMB} = 25^\circ\text{C}$ ($I_D = 50, 75, 100, 125, 150, 175, 200\text{ mA}$)

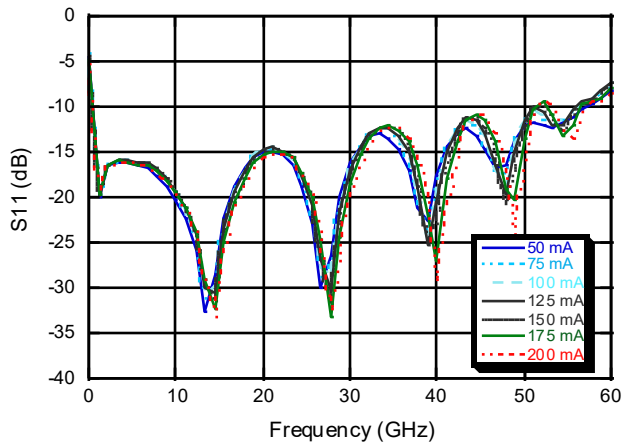
Gain



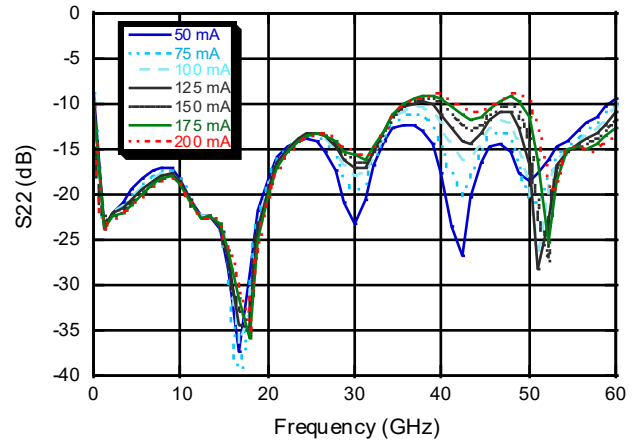
Reverse Isolation



Input Return Loss



Output Return Loss



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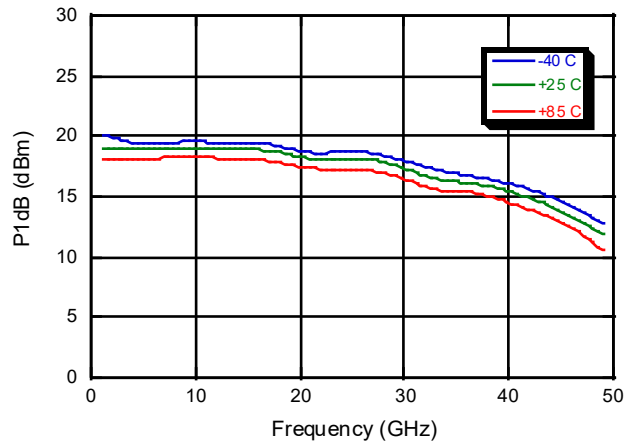


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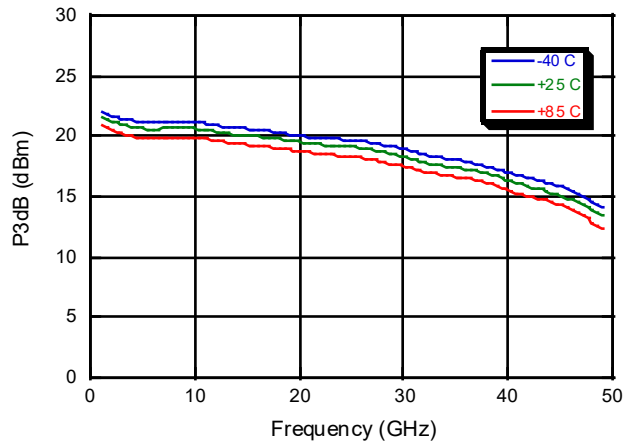
Rev. V1

Typical Performance at $V_D = 6\text{ V}$, $I_D = 165\text{ mA}$, $T_A = 25^\circ\text{C}$

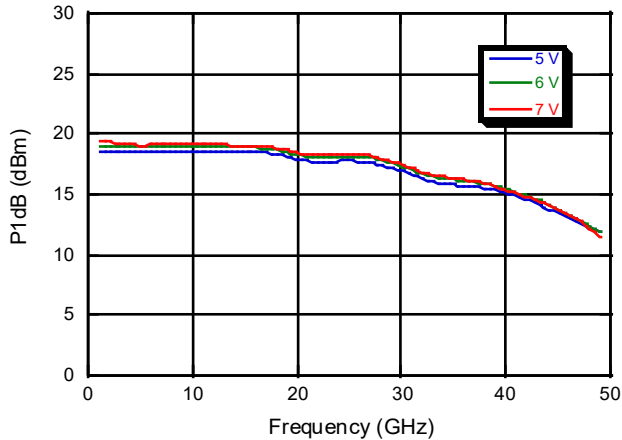
P1dB



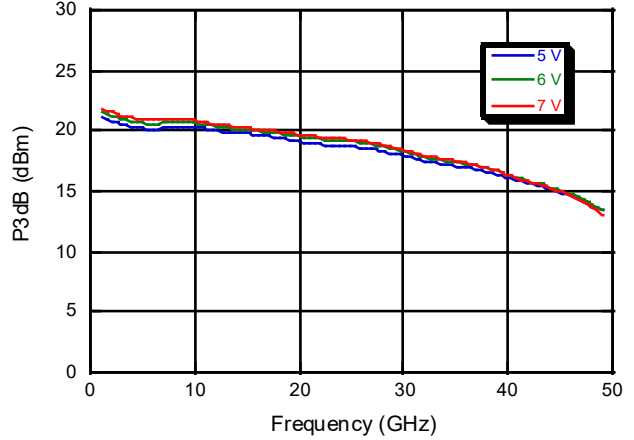
P3dB



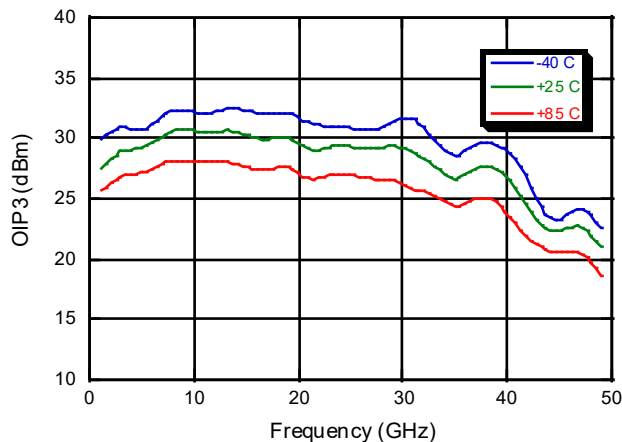
P1dB



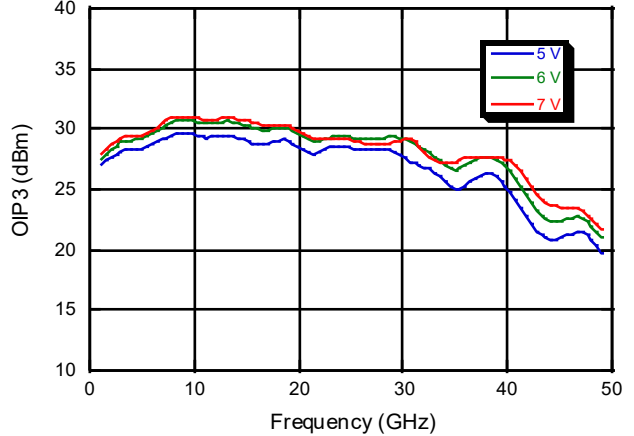
P3dB



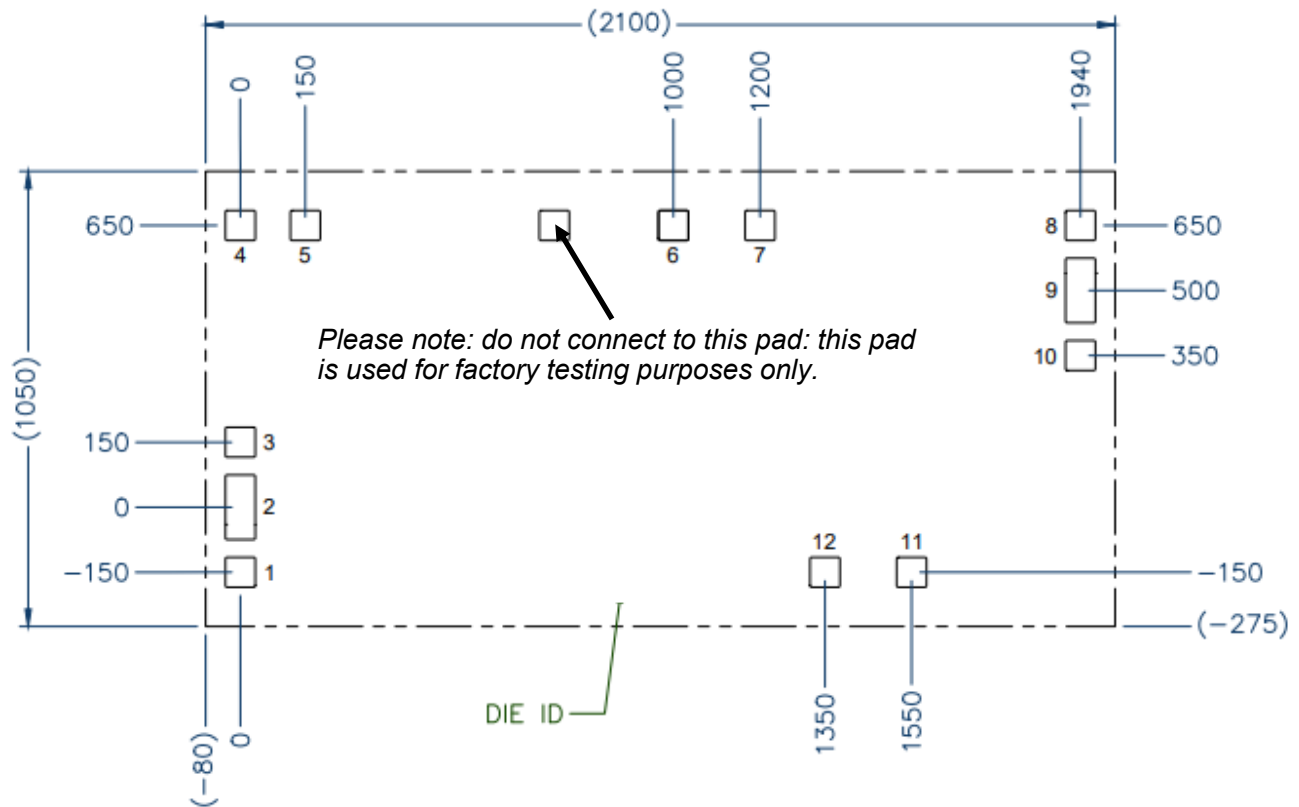
OIP3



OIP3



Die Dimensions



BOND PAD DIM. (μm)			
PAD	X	Y	PIN LABEL
1	69	69	GND
2	69	149	RF _{IN}
3	69	69	GND
4	69	69	VG2
5	69	69	AUX
6	69	69	GND
7	69	69	DET _{OUT}
8	69	69	GND
9	69	149	RF _{OUT}
10	69	69	GND
11	69	69	VG1
12	69	69	GND

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS SHOWN ARE μm WITH A TOLERANCE OF ±5μm.
2. DIE THICKNESS IS 100 ±10μm
3. BOND/PAD BACKSIDE METALLIZATION: GOLD
4. DIE SIZE REFLECTS UN-CUT DIMENSIONS. LASER KERF REDUCES DIE SIZE BY ~25μm EACH DIMENSION.

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