MAAM-011167

Medium Power Amplifier
71 - 86 GHz

Rev. V2

Features

- 4 Stage Driver Amplifier for E Band
- 18 dB Gain
- 10 dB Input and Output Match
- 24 dBm Saturated Output Power
- 27 dBm OIP3
- Variable Gain with Adjustable Bias
- Integrated Detector
- Bare die
- RoHS* Compliant
- HBM ESD rating of 200 V
- Size: 3780 x 1500 x 50 µm

Description

The MAAM-011167 is a bare die power amplifier that operates from 71 - 86 GHz. The amplifier provides 18 dB small signal gain. The input and output are matched to 50 Ω with bond wires to external board.

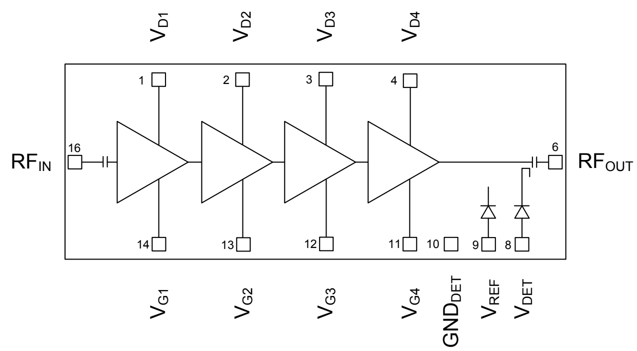
It is designed for use as a driver stage in transmit chains and is ideally suited for E band point to point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Ordering Information

Part Number	Package
MAAM-011167-DIE	Die in Vacuum release gel pack

Chip Device Layout



Pad Configuration

Pad No.	Function	Pad No.	Function
1	V_D1	9	V_{REF}
2	V_D2	10	GND_{DET}
3	V_D3	11	V_G4
4	V_D4	12	V_G3
5	GND	13	V_G2
6	RF_{OUT}	14	V_G1
7	GND	15	GND
8	V_{DET}	16	RF_{IN}
		17	GND

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications[1,2]: Freq. = 71 - 86 GHz, V_D = 4 V, I_D = 360 mA, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Gain	dB	16	18	-
Input Return Loss	dB	-	10	-
Output Return Loss	dB	-	10	-
P1dB	dB	-	21	-
P_{OUT} with P_{IN} = 10 dBm	dBm	20	24	-
P_{SAT} (P3dB)	dBm	-	24	-
OIP3 (worst tone)	dBm	-	27	-
IIP3 (worst tone) for Gain = 20 turned-down to -5 dB	dBm	-	10	-

1. Minimum limits are the on-wafer minimum test limits.
2. Quiescent DC Bias: I_D1= 30 mA, I_D2 = 60 mA, I_D3 = 120 mA, I_D4 = 150 mA. Total DC Power = 1.44 W.

Absolute Maximum Ratings [3,4,5]

Parameter	Absolute Max.
Drain Voltage	4.3 V
Drain Current	460 mA
Gate Bias Voltage (V_G1,2,3,4)	-1.5 V < V_G < +0.3 V
Input Power	13 dBm
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Junction Temperature	150°C
Thermal Resistance	16.15°C/W

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq 150$°C will ensure MTTF > 1 x 10^6 hours.

Handling Procedures

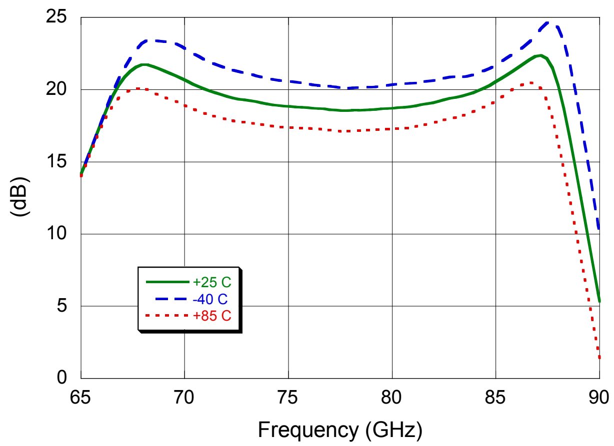
Please observe the following precautions to avoid damage:

Static Sensitivity

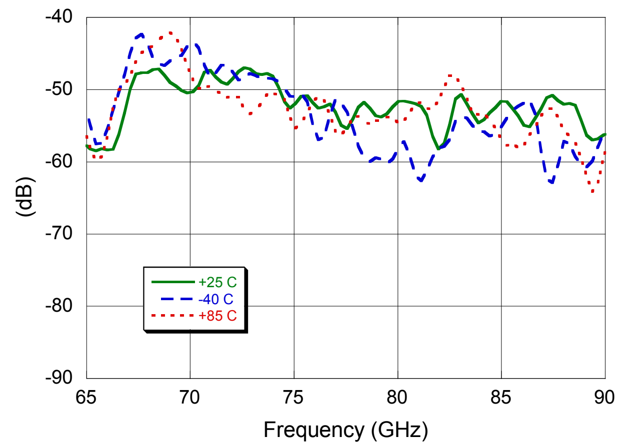
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 0 static sensitive devices.

Typical Performance Curves

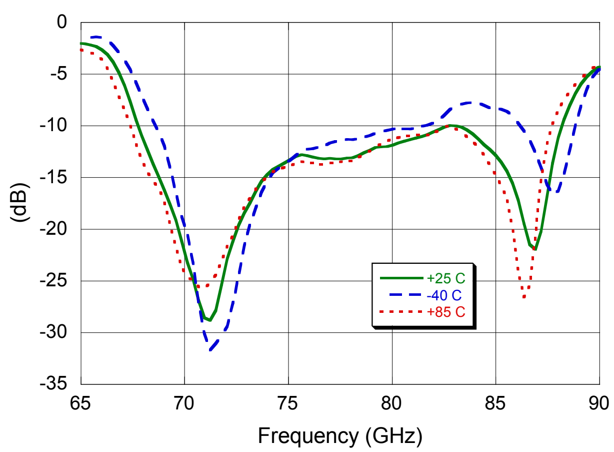
Gain @ VD = 4 V, I_{DQ} = 360 mA



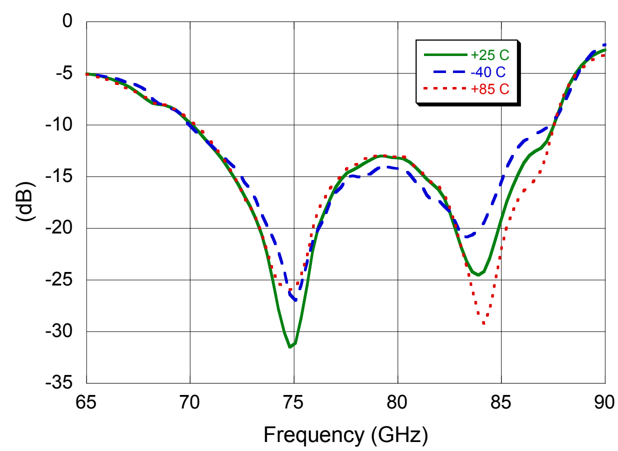
Reverse Isolation @ VD = 4 V, I_{DQ} = 360 mA



Input Return Loss @ VD = 4 V, I_{DQ} = 360 mA

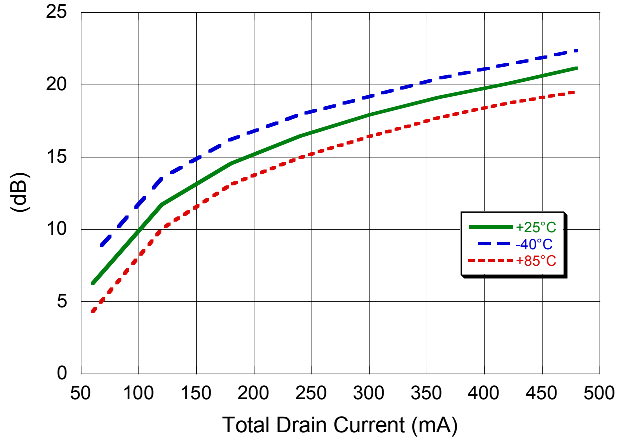


Output Return Loss @ VD = 4 V, I_{DQ} = 360 mA

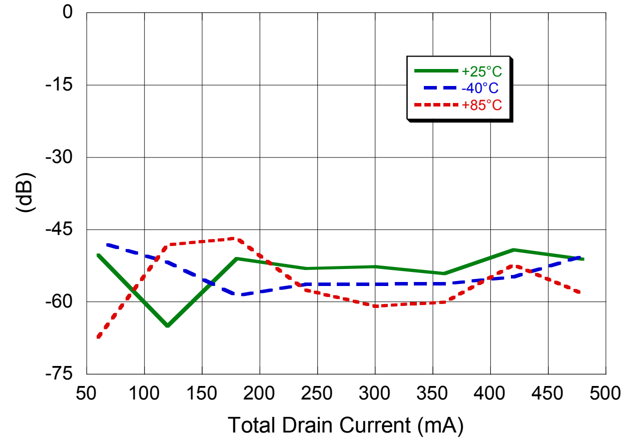


Typical Performance Curves

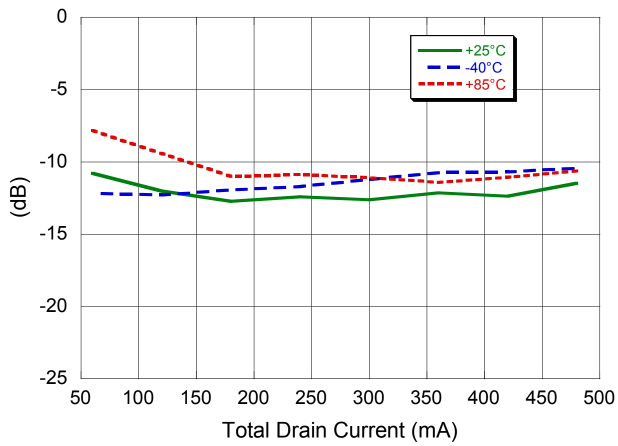
Gain, @ VD = 4 V, Frequency = 80 GHz



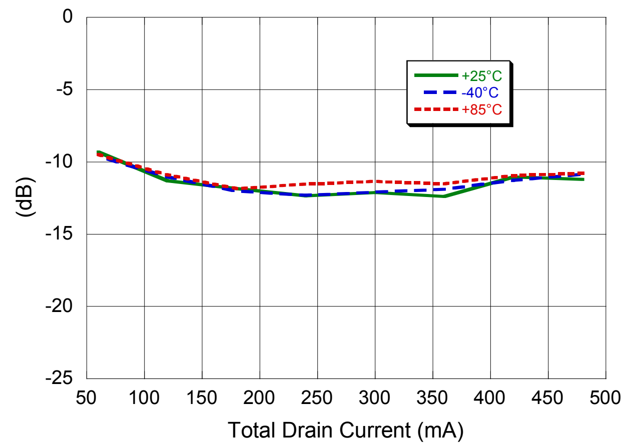
Reverse Isolation @ VD = 4 V, Frequency = 80 GHz



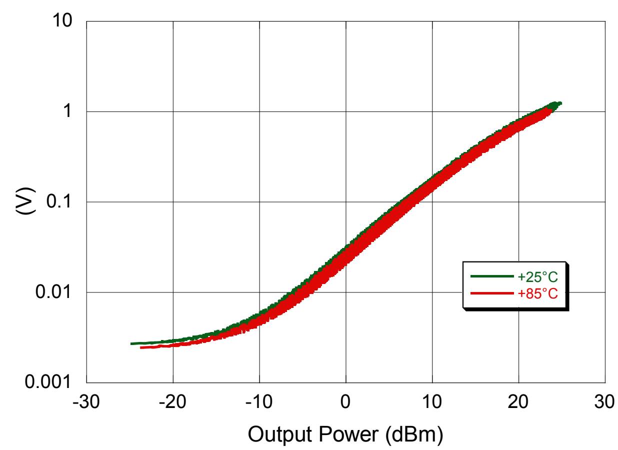
Input Return Loss @ VD = 4 V, Frequency = 80 GHz



Output Return Loss @ VD = 4 V, Frequency = 80 GHz

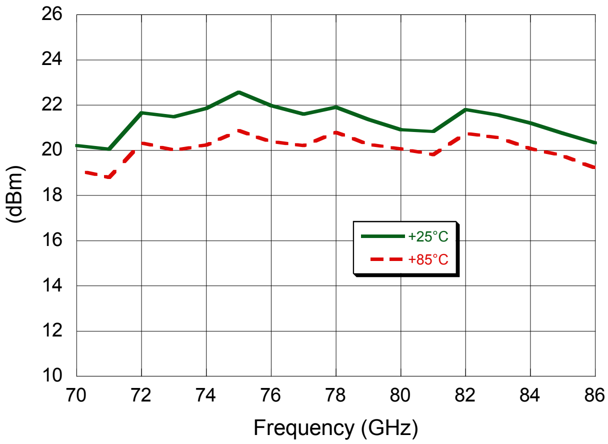


Detector Delta Voltage @ VD = 4 V

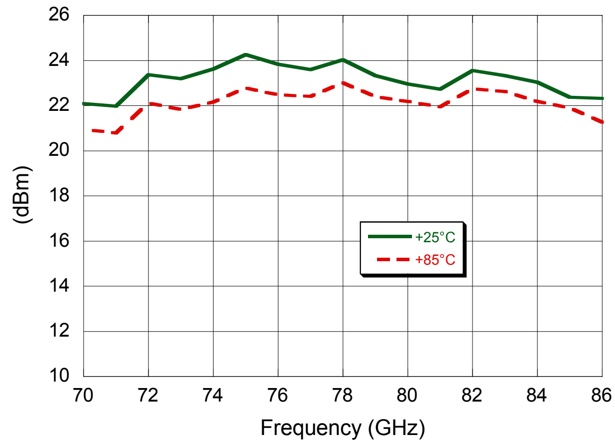


Typical Performance Curves

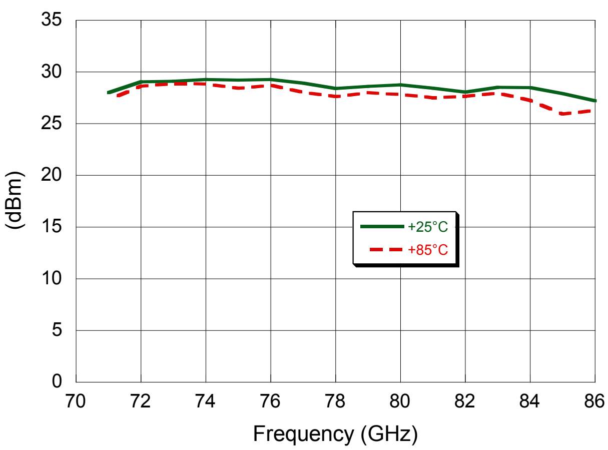
P1dB vs. Frequency @ VD = 4 V, I_{DQ} = 360 mA



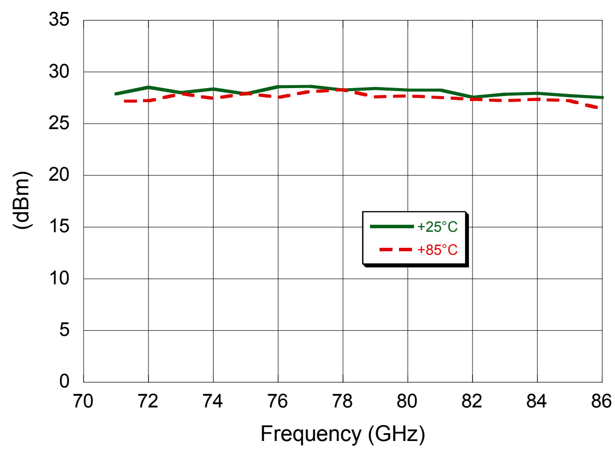
P3dB vs. Frequency @ VD = 4 V, I_{DQ} = 360 mA



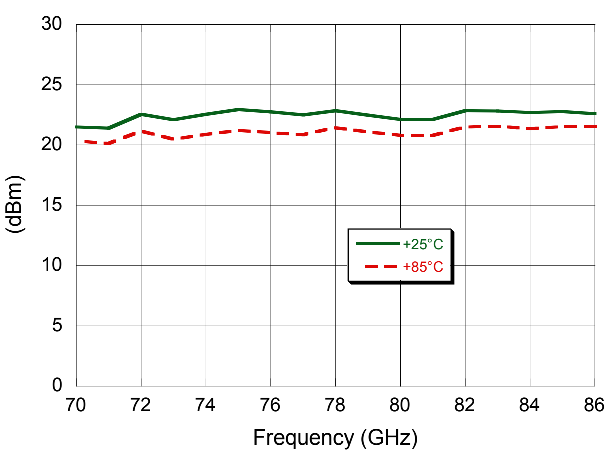
Output IP3 vs. Frequency @ VD = 4 V, I_{DQ} = 250 mA



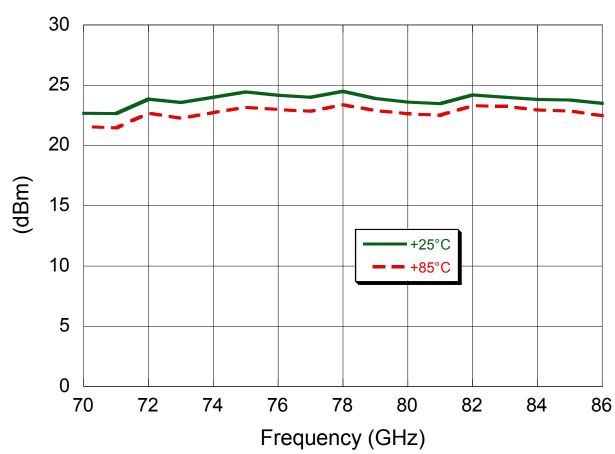
Output IP3 vs. Frequency @ VD = 4 V, I_{DQ} = 360 mA



P_{OUT}, P_{IN} = 10 dBm @ VD = 4 V, I_{DQ} = 250 mA

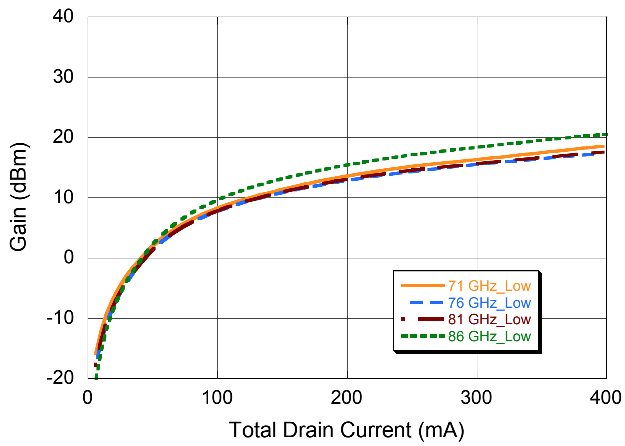


P_{OUT}, P_{IN} = 10 dBm @ VD = 4 V, I_{DQ} = 360 mA

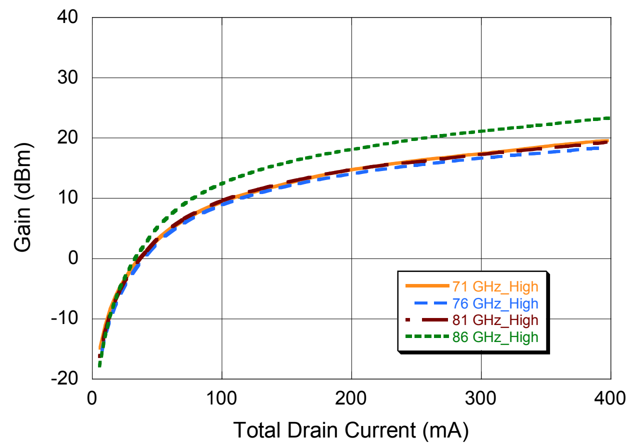


Typical Performance Curves

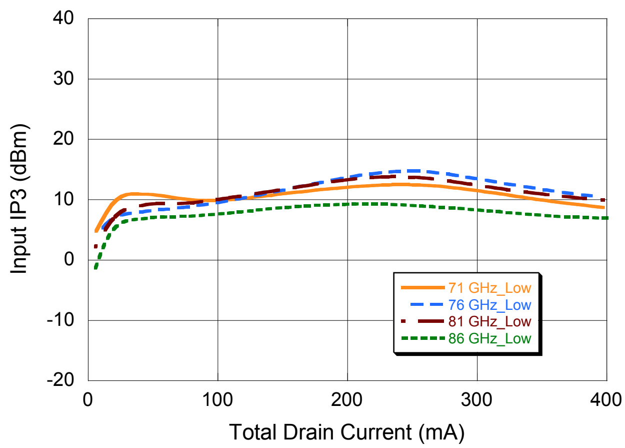
Lower Tone Gain vs. Total Current @ VD = 4 V



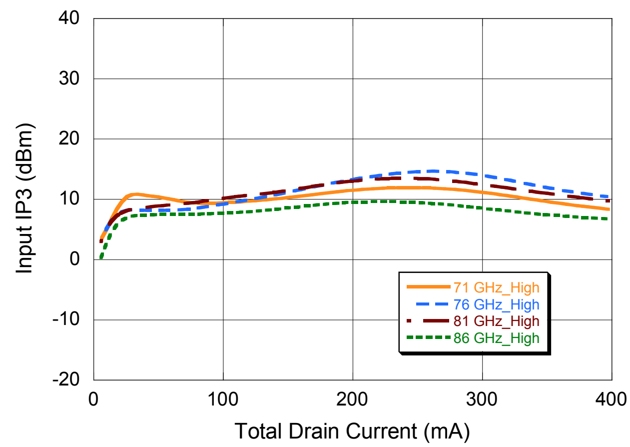
Upper Tone Gain vs. Total Current @ VD = 4 V



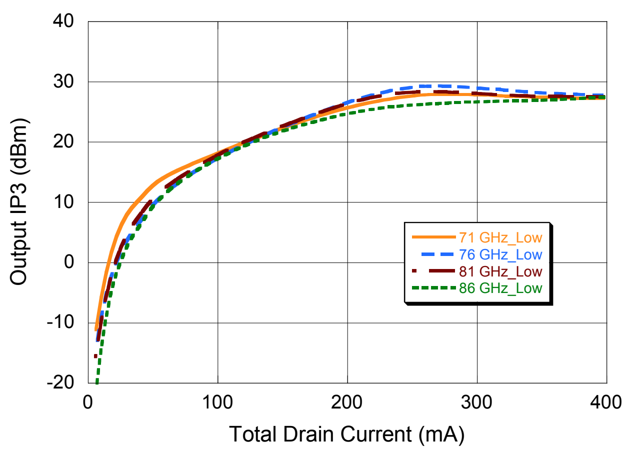
Lower Tone Input IP3 vs. Total Current @ VD = 4 V



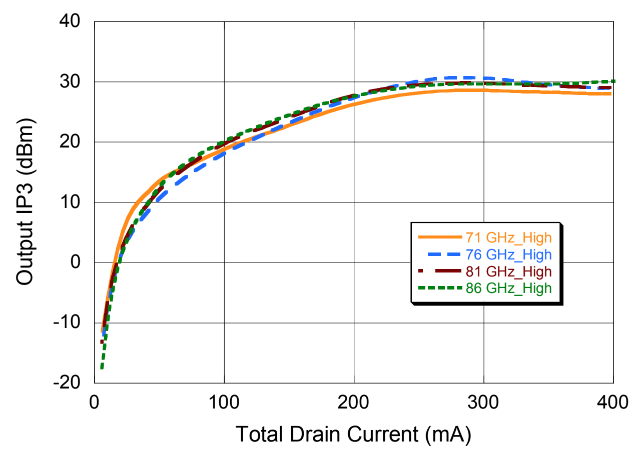
Upper Tone Input IP3 vs. Total Current @ VD = 4 V



Lower Tone Output IP3 vs. Total Current @ VD = 4 V

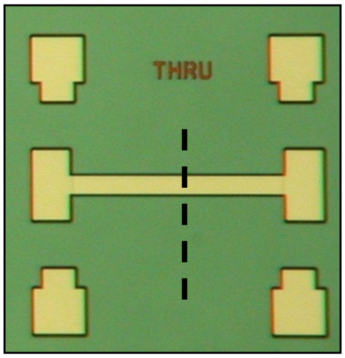


Upper Tone Output IP3 vs. Total Current @ VD = 4 V



Calibration Plane

All data was measured on die with 200 µm pitch probes. The calibration plane is at the middle of the through, 178.5 µm from the middle of the RF pad.



App Note [1] Biasing -

All gates should be pinched-off (V_G < -1 V) before applying drain voltage (V_D = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is V_D = 4 V, I_D1 = 30 mA, I_D2 = 60 mA, I_D3 = 120 mA and I_D4 = 150 mA. The performance in this datasheet has been measured with the gate bias set to the voltage that gives the stated value of the quiescent current. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -

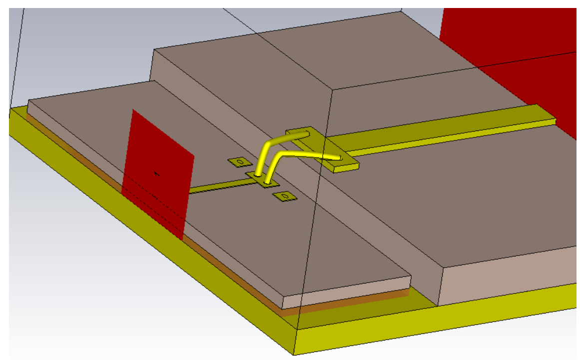
Each DC pin (V_D1,2,3,4 and V_G1,2,3,4) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.

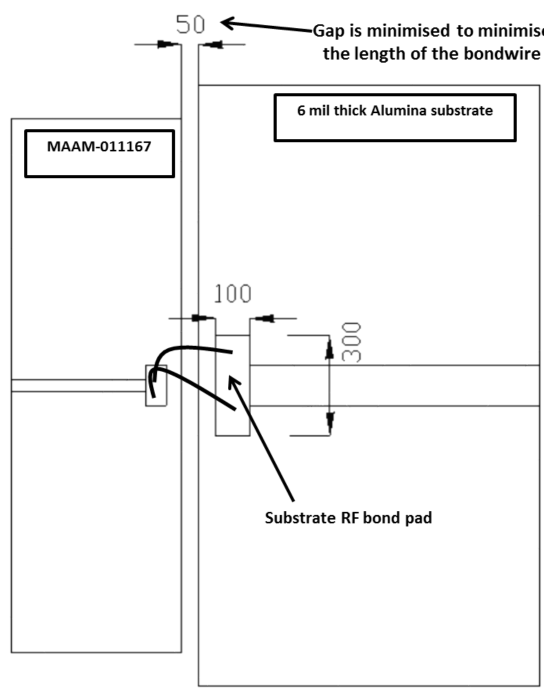
App Note [3] Wire Bonding -

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, Forward Loop bonding may result in a lower loop height.

V-shape RF bond with two wires (diameter = 25 µm) is recommended for optimum RF performance.

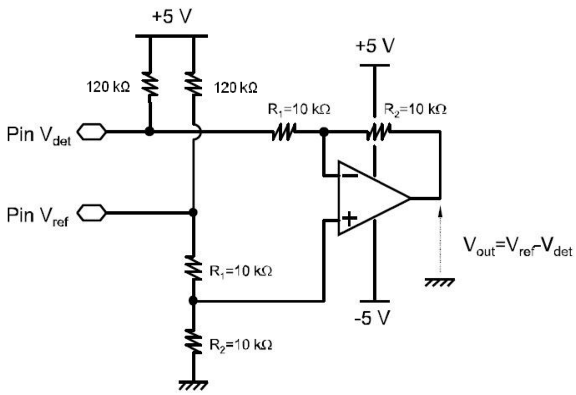
RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the Microstrip to MMIC bond transition as shown in the example below.



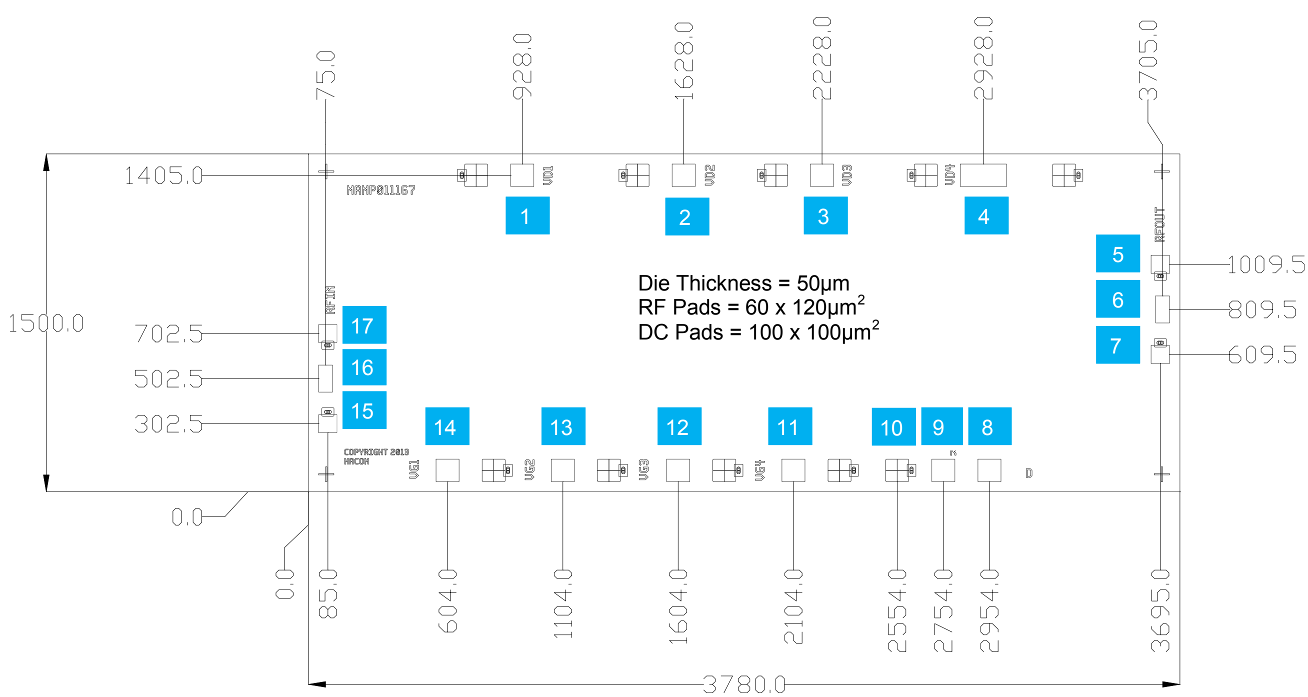


App Note [4] Detector biasing schematic -

As shown in the schematic below, the power detector is biased by matched 120 kΩ resistors to a 5 V bias. The difference voltage between V_{DET} and V_{REF} pins can be obtained using the op-amp differencing circuit shown below.



Layout Dimensions



Assembly Diagram