MAAM-011109-DIE

Wideband Amplifier
DC - 50 GHz

Rev. V3

Features

- 15 dB Gain
- 50 Ω Input / Output Match
- 20 dBm Output Power
- 5 V DC, 190 mA
- Die size: 1.97 x 1.30 x 0.1 mm
- Gold-Plated Contact Pads, Backside
- 100% On-Wafer DC & RF Tested
- RoHS* Compliant

Description

The MAAM-011109-DIE is an easy-to-use, wideband amplifier that operates from DC - 50 GHz. This device features 15 dB gain and +20 dBm of output power. Matching is 50 Ω with typical return loss better than 15 dB. This amplifier requires dual DC power supplies: 5V (190 mA) and a low current negative VG1 (< 1 mA).

Features include gate bias adjust to change current setting for power or temperature, gain trim control that allows 15 dB of gain control (0 to -1 V), and a temperature-compensated detector that provides a DC voltage in relation to the output power.

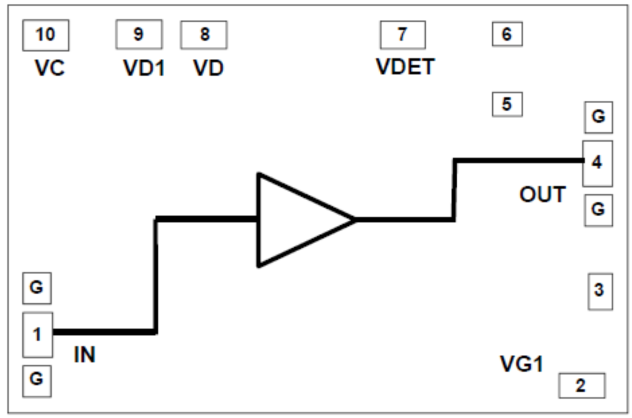
The MAAM-011109-DIE is ideally suited for any application that requires 50 Ω gain from DC to 50 GHz. It is useful in circuits where the incoming signal varies over a broad bandwidth such as laboratory, instrumentation, and defense applications.

Ordering Information[1]

Part Number	Package
MAAM-011109-DIE	Die in Gel Pack

1. Die quantity varies.

Functional Schematic



Pad Configuration[2,3]

Pin #	Pin Name	Function
1	IN	RF Input (alternate gate bias)
2	VG1	Gate Voltage (negative)
3	VC2	Gain Control (alternate)
4	OUT	RF Output (drain bias)
5, 6	N/C	Do Not Use
7	VDET	Power Detector
8	VD	Bypass (alternate drain bias)
9	VD1	Alternate Bypass
10	VC	Gain Control
G	Ground	

2. See Application Information for biasing details.
3. The backside of the die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[4]:
T_A = +25°C, +5 V (applied to OUT), VG1 = -0.4 V, VC = Open, Z_{IN} = Z_{OUT} = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	10 KHz - 2 GHz 2 - 40 GHz 50 GHz	dB	— 14.0 —	15.5 15.5 12	—
Isolation	DC - 50 GHz	dB	—	22	—
Input Return Loss	DC - 50 GHz	dB	—	15	—
Output Return Loss	DC - 20 GHz 20 - 50 GHz	dB	—	15 9	—
Noise Figure	DC - 40 GHz	dB	—	3.5	—
P1dB	0.1 GHz 10 GHz 40 GHz	dBm	—	21 21 15	—
Output IP3	0.1 GHz 10 GHz 40 GHz	dBm	—	29 29 19	—
Bias Current	—	mA	—	190	—

4. See Application Information for biasing details.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	17 dBm
Drain Voltage	7.5 V
Drain Current	240 mA
Control Voltage	-1 V ≤ VC ≤ 1.2 V
Junction Temperature[7,8]	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
8. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 17.8°C/W.
   a) For T_C = 25°C,
      T_J = 47°C @ 6.5V, 190mA
   b) For T_C = 85°C,
      T_J = 107°C @ 6.5V, 190mA

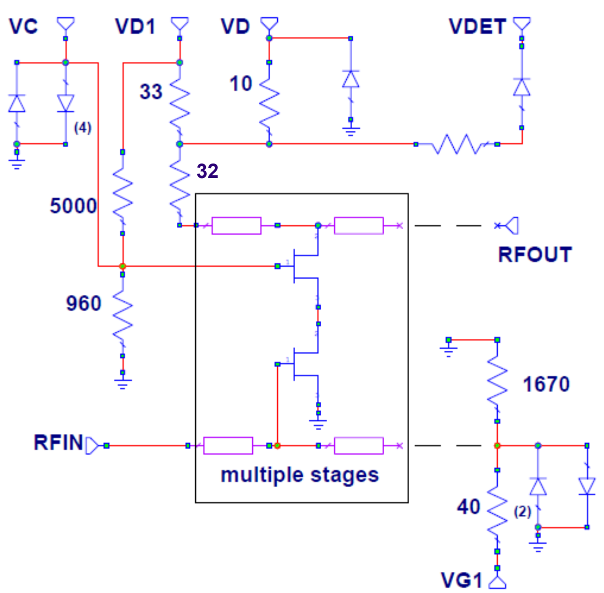
Handling Procedures

Please observe the following precautions to avoid damage:

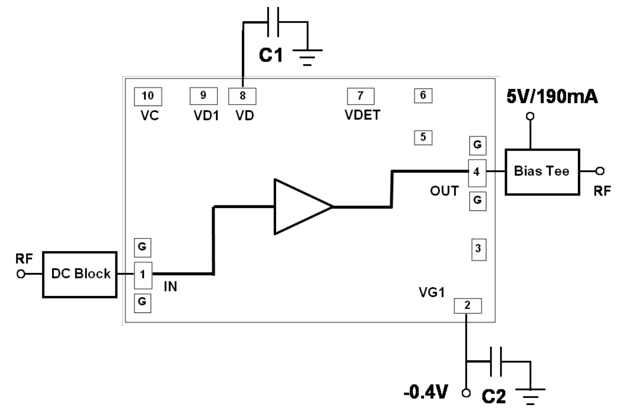
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A devices.

Biasing Schematic



Application Schematic (recommended biasing)



Parts List

Part	Value	Case Style
C1, C2	> 150 pF	0201 or parallel plate

Application Information (DC & Pads)

For proper operation a DC voltage must be applied to the VG1 (typically -0.4 V) and OUT (typically +5 V) pads *in that order*. Note that the Biasing Schematic shows ESD diodes connected to the VC and VG1 pads (the notation (4) on the VC pad indicates there are four forward diodes in series and the (2) on the VG1 pad diode indicates there are two reverse diodes in series).

Adjusting VG1 from -1.0 to -0.2 V will increase the quiescent current. The actual operating voltage should be kept between 3.3 and 6.5 V for proper operation.

The VG1 and VD pads should be bypassed with 0.22 μF for flattest overall low end response. Best flatness for 1 GHz and above will be achieved by bypassing the VD1 pad, instead of the VD pad, with at least 150 pF and a total trace plus bondwire inductance of 2.5 nH, and the VG1 pad with at least 150 pF.

The VC pad is typically left unconnected unless gain control or output power limiting is desired. Please refer to the “Variable Gain/Limiting” section for detailed usage. The VDET pad is typically left unconnected unless a voltage indication of the output power is required. Please refer to the “Internal Detector” section for detailed usage.

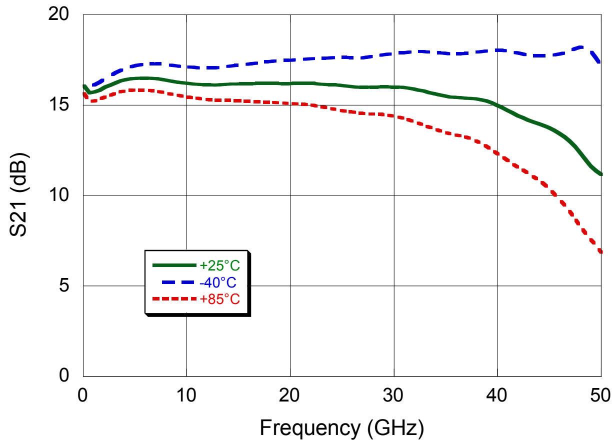
Bandwidth, Power, Noise and Linearity

Bias voltage and current affect both the bandwidth (response flatness), power available, noise figure, and linearity of the amplifier. Higher currents and lower bias voltage increase high frequency gain but reduce the P1dB and the OIP3 numbers. If the device is driven to P1dB and on into Psat the bias current will naturally reduce. The device will return to the quiescent current value once the input power is reduced. Finally, higher bias current values increase the device noise figure.

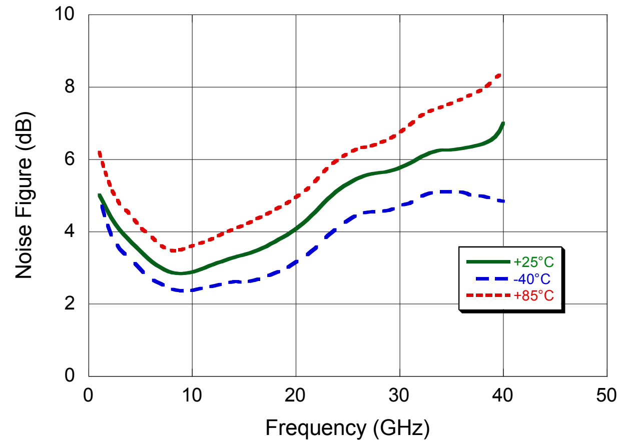
Temperature also affects the bandwidth, gain and noise figure of the device. Lower temperatures increase gain and bandwidth but reduce the noise figure. Temperature has little effect on power and linearity.

Typical Performance Curves over Temperature, 5 V / 190 mA

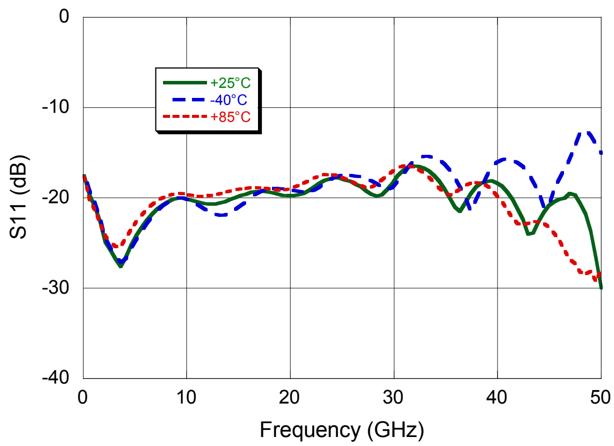
Gain



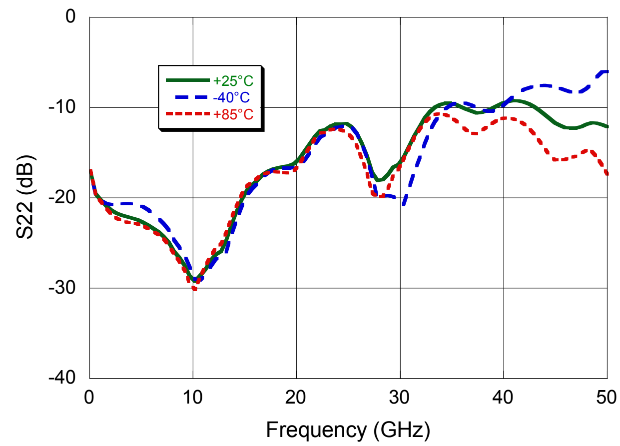
Noise Figure



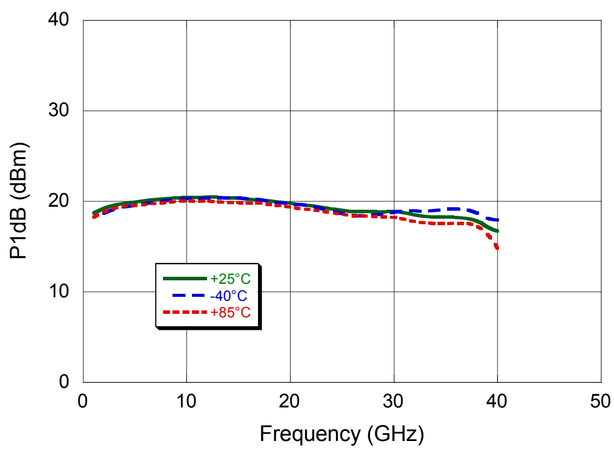
Input Return Loss



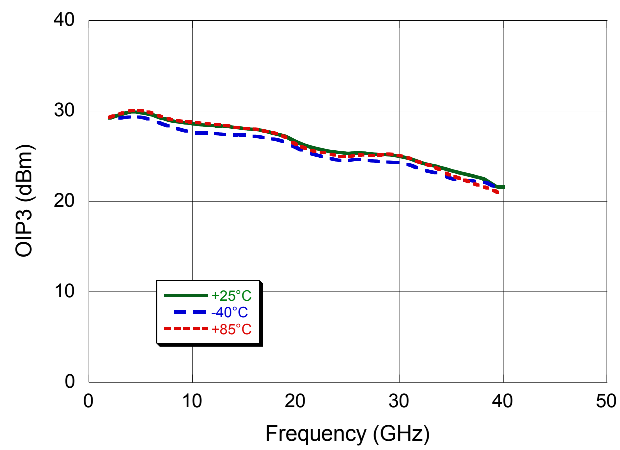
Output Return Loss



Output P1dB

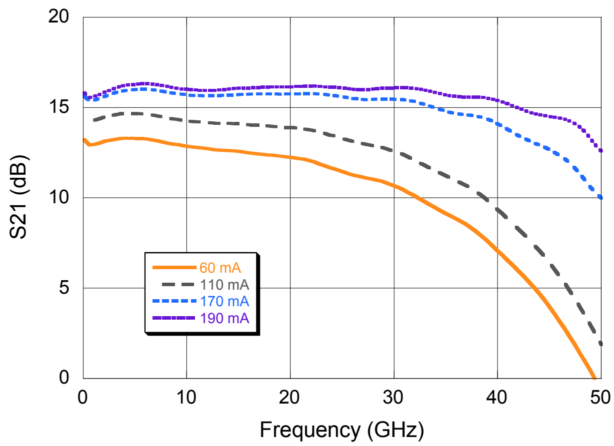


Output IP3

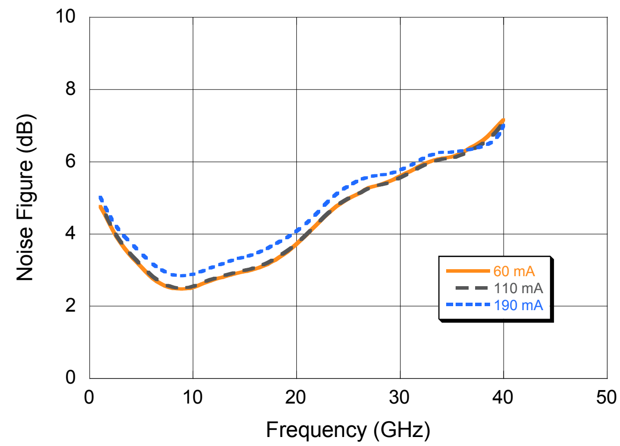


Typical Performance Curves over Current and Voltage (5 V unless otherwise noted)

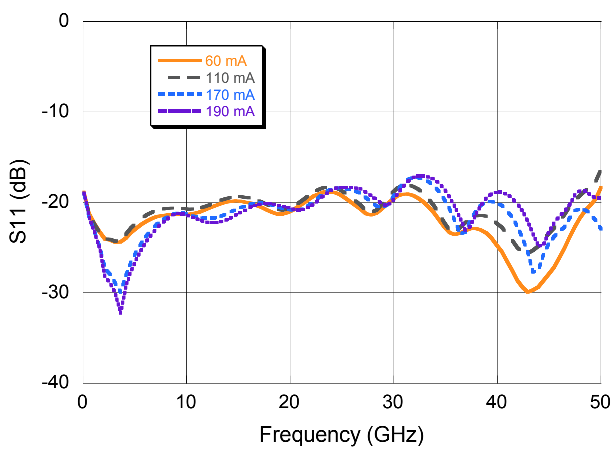
Gain over Current



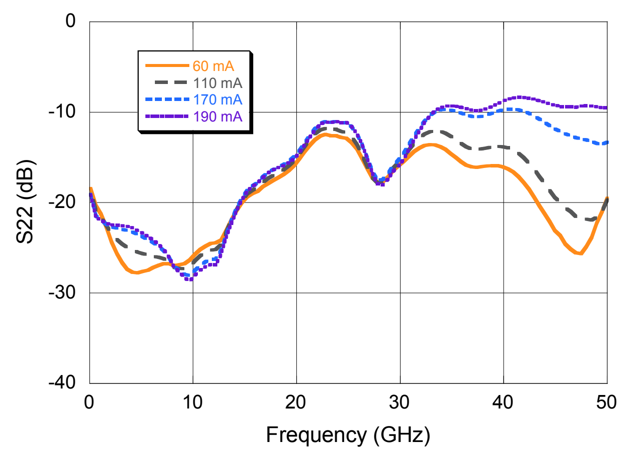
Noise Figure over Current



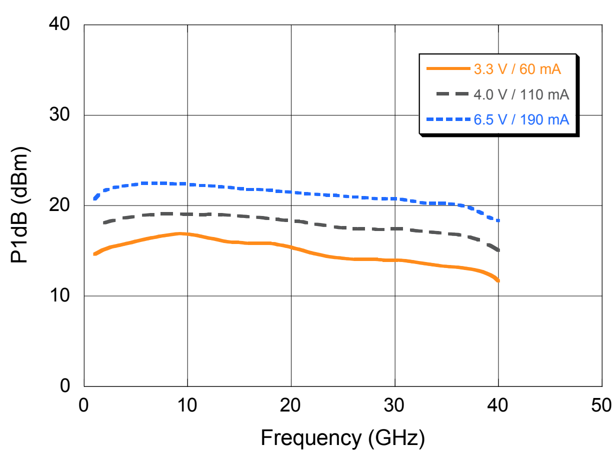
Input Return Loss over Current



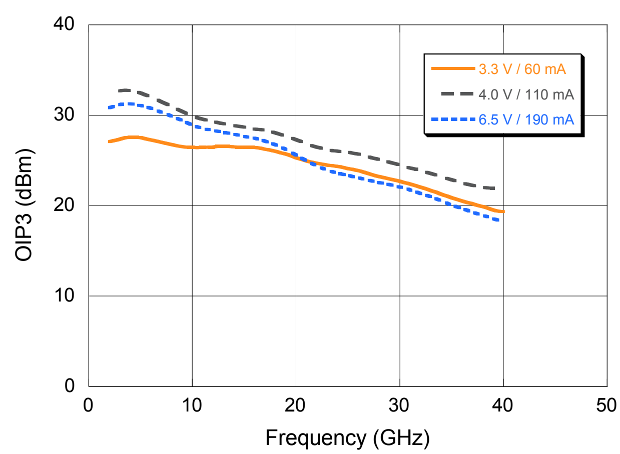
Output Return Loss over Current



Output P1dB over Voltage and Current

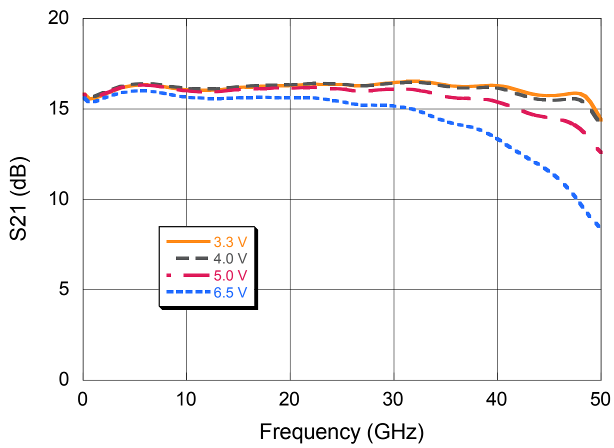


Output IP3 over Voltage and Current

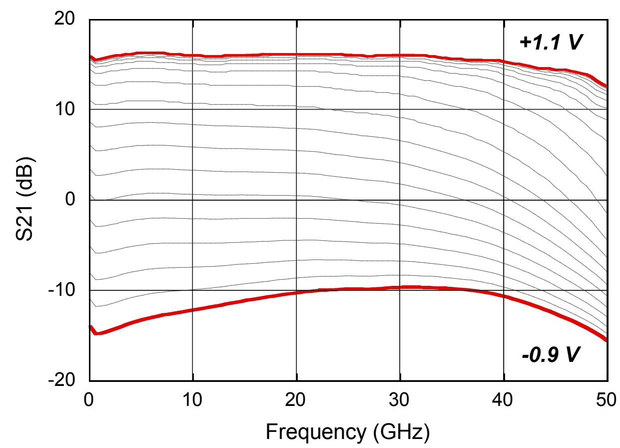


Typical Performance Curves, 5 V / 190 mA unless otherwise noted

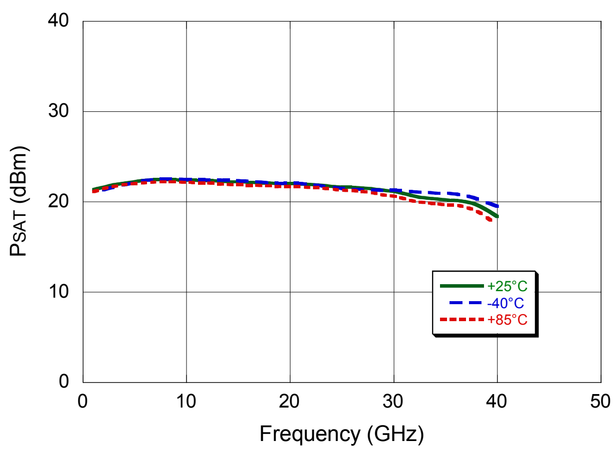
Gain vs. Frequency over voltage



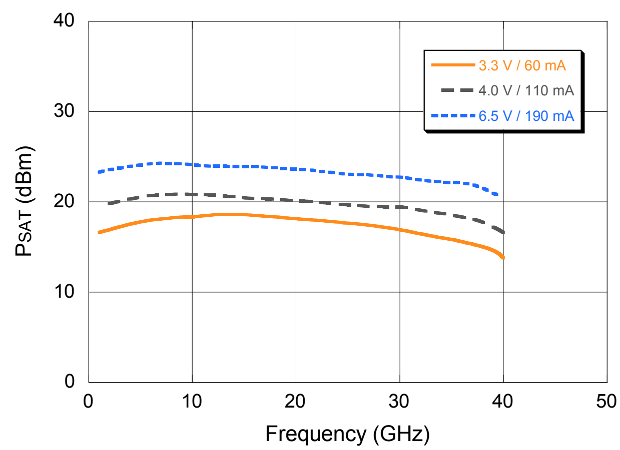
Gain vs. Frequency, VC from -0.9 to +1.1 V



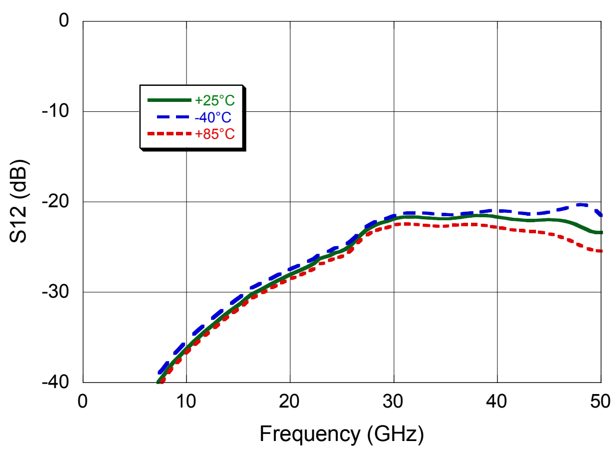
Output Saturated Power over Temperature



Output Saturated Power over Bias

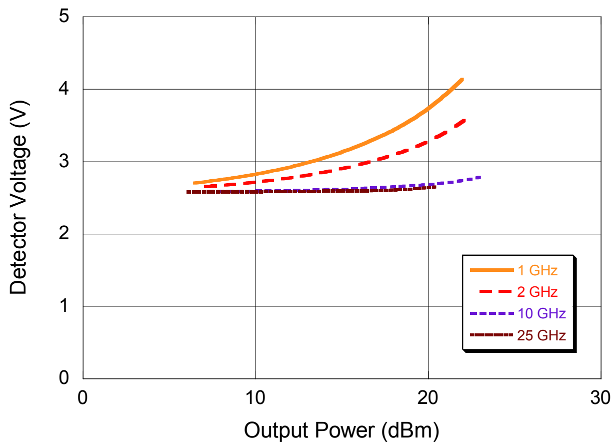


Isolation over Temperature

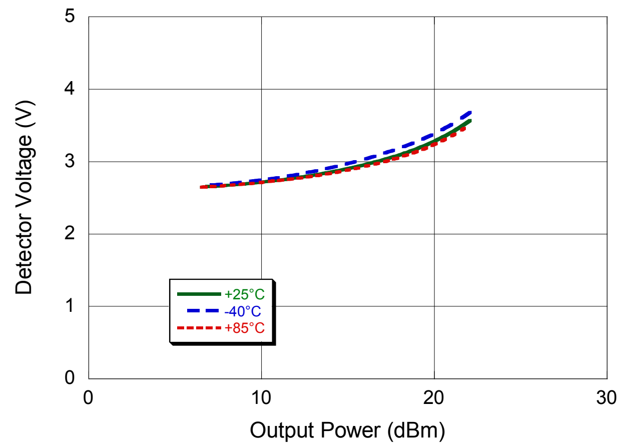


Typical Performance Curves, 5 V / 190 mA unless otherwise noted

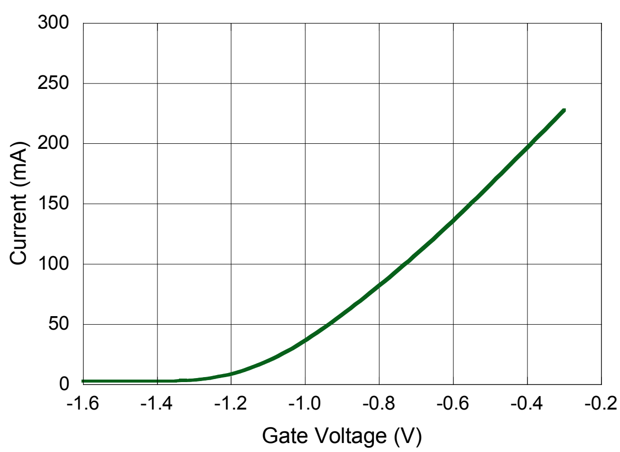
VDET vs. Output Power



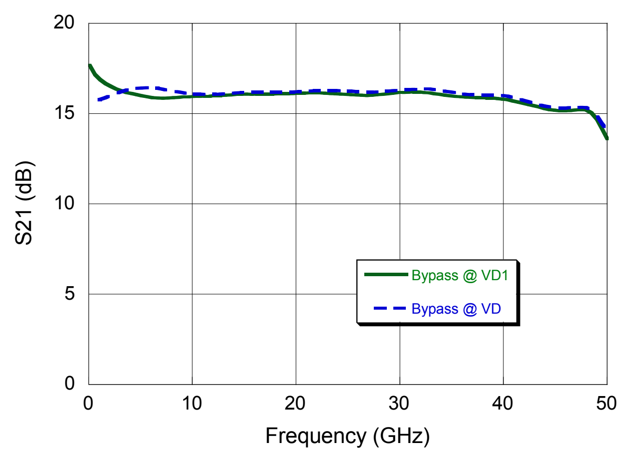
VDET vs. Output Power at 2 GHz over Temperature



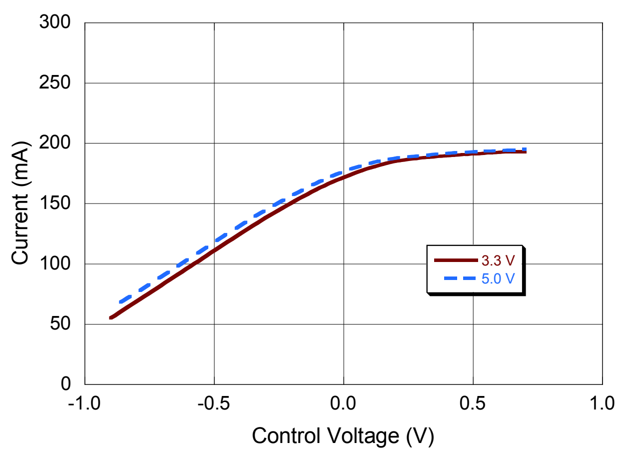
Current vs. VG1



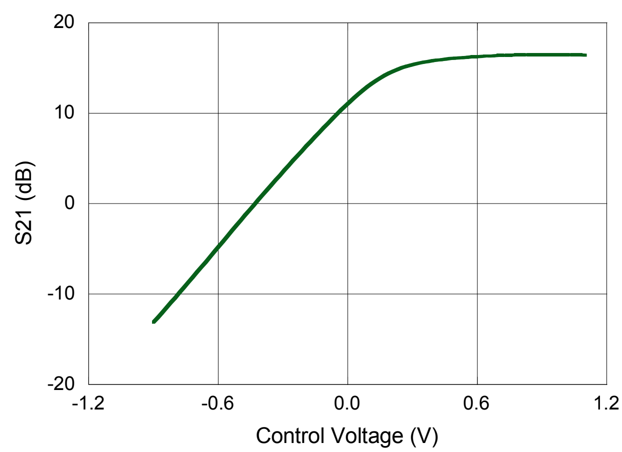
Gain vs. VD1 Bypass with 0.22 µF 0201 capacitors



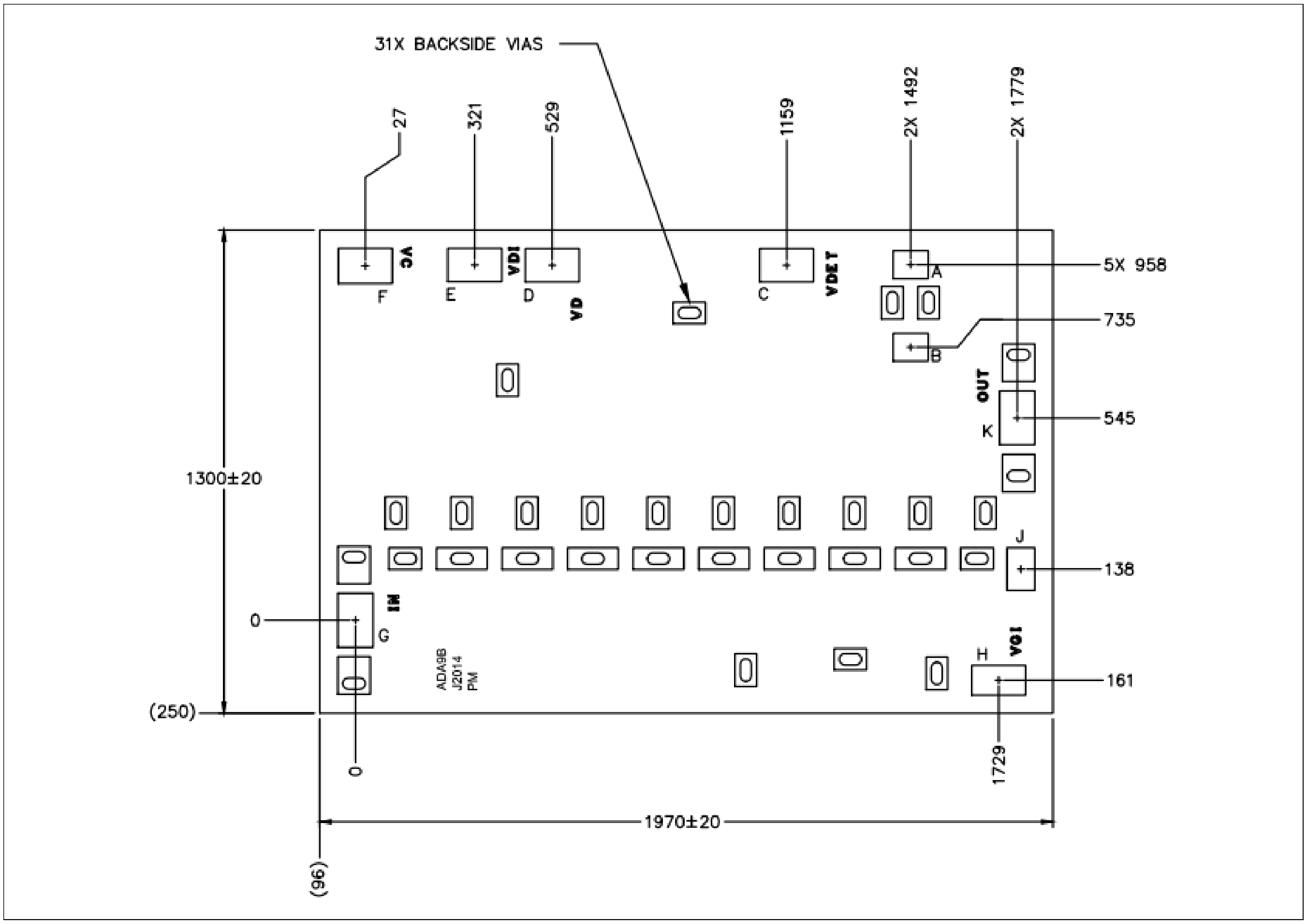
Current vs. VC



Gain at 5 GHz vs. VC



Outline Drawing



Bond Pad Detail in µm

Pad	Size (x)	Size (y)
A	85	65
B	85	65
C	135	80
D	135	80
E	135	80
F	135	85
G	85	135
H	135	70
J	65	105
K	85	135
GND	78	91

Notes:
1. All units are in µm, unless otherwise noted, with a tolerance of ±5 µm.
2. Die thickness is 100 ±10 µm.

Broadband Amplifier Applications

The MAAM-011109-DIE also has a low enough noise figure to be used in instrumentation front ends and buffer applications. It also has very flat response with low group delay distortion so it can be used in pulse applications. For higher gains multiple amplifiers may be cascaded. It also makes a very good low cost optical driver capable of delivering up to 8 V p-p into 50 ohms.

Variable Gain/Limiting Applications

The gain of the MAAM-011109-DIE can be easily controlled with the VC pin. The gain reduction is almost linear with VC between 0.1 V to -0.8 V. Below -0.7 V internal ESD protection diodes will draw increasing current (50 mA at -1.0 V). The VC pad should not be driven below -1 V or above 1.2 V. The nominal open circuit voltage at the VC pad is 0.8 V.

Reducing VC below 0.8 V will also reduce the bias current. Gain, P1dB, and PSAT will all be reduced as the voltage on VC is lowered. Limiting applications and zero crossing adjustment can be done by adjusting the VG1 and VC pads together.

Internal Detector

The VDET pad is connected to an internal diode detector. This pad should be connected to a high impedance (>50 kΩ) or left unconnected. The detector is internally connected so that it responds predominately to the power generated by the amplifier and is temperature compensated. The detector has a low pass characteristic which rolls off gradually above 1 GHz. Finally, even with zero output power the detector has a DC output voltage proportional to the bias voltage (nominally 2.8 V for 5 V at the OUT pad).