Low Noise Amplifier
17.0 - 21.5 GHz

MAAL-011265-DIE
Rev. V2

Features
- Gain: 29 dB
- Low Noise Figure: 1.4 dB
- P1dB: 10.5 dBm
- OIP3: 18 dBm
- Bias Voltage: V_{DD} = +2 V
- Bias Current: I_{DSQ} = 25 mA
- 50 Ω Matched Input and Output
- 0.92 x 0.93 x 0.1 mm die
- RoHS* Compliant

Applications
- Satellite Communications
- Low Earth Orbit Space Payloads
- GEO High Throughput Satellite
- Radar
- EW

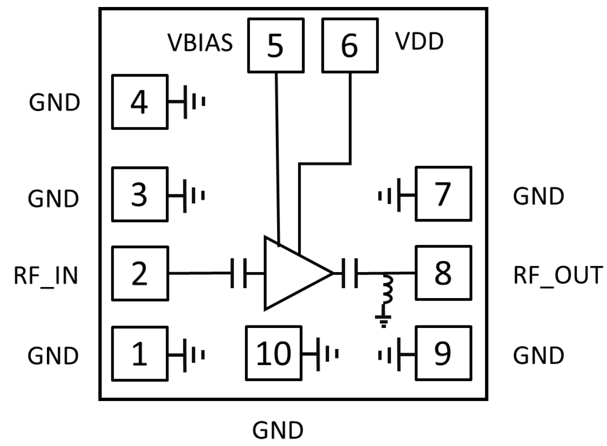
Description
The MAAL-011265-DIE is an easy to use low noise amplifier. It operates from 17 GHz to 21.5 GHz and provides 1.4 dB noise figure, 29 dB gain and a P1dB of 10.5 dBm. The input and output are fully matched to 50 Ω with typical return loss >12 dB.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

The MAAL-011265-DIE can be used as an ultra-low power dissipation low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Ka-band communication systems.

It is also available in a 2 mm DFN package under part number MAAL-011265.

Functional Schematic



Pin Configuration[1]

Pad #	Function	Description
1,3,4,7,9,10	GND	Ground
2	RF_IN	RF Input
5	VBIAS	Bias Voltage
6	VDD	Drain Voltage
8	RF_OUT	RF Output

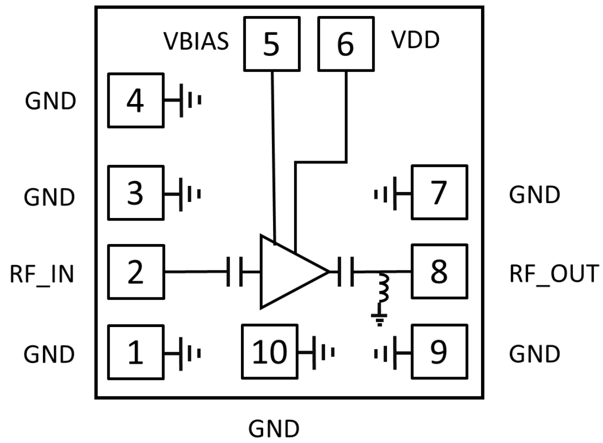
1. The backside of the die must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package
MAAL-011265-DIE	Bulk

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1,3,7,9	GND	These pins are grounded internally.
2	RF_IN	RF Signal Input. This pad is matched to 50 Ω and is AC coupled
4,10	GND	These pins are grounded internally and should not be bonded in the application
5	VBIAS	A voltage can be applied to this pin to set the required IDSQ as described in the application section
6	VDD	Drain bias for the amplifier. External bypass capacitors are required as described in the applications schematic.
8	RF_OUT	RF Signal Output. This pad is matched to 50 Ω and is AC coupled. There is a shunt inductor to ground providing a DC ground path.
Backside		RF, DC and thermal ground

Electrical Specifications: Freq. = 17.0 - 21.5 GHz, T_A = 25°C, V_D = +2 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	P_{IN} = -30 dBm 17.0 GHz 21.5 GHz	dB	24 22	29 27	—
Small Signal Gain Variation	over Temperature	dB/°C	—	0.06	—
Gain Flatness	—	dB	—	1	—
Noise Figure	—	dB	—	1.4	2
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	12	—
P1dB	17.0 GHz 21.5 GHz	dBm	8.0 8.5	10.5 11.0	—
Output 3rd Order Intercept	P_{IN} = -30 dBm/tone (10 MHz tone spacing)	dBm	—	18	—
Supply Current	—	mA	—	25	—

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Input Power	+18 dBm
Drain Voltage	4.5 V
Junction Temperature[4,5]	+165°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \le +150°C$ will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 100 °C/W.
   a) For T_C = +25°C,
      T_J = 27.4 °C @ 2 V, 25 mA
   b) For T_C = +85°C,
      T_J = 87.4 °C @ 2 V, 25 mA

Maximum Operating Conditions

Parameter	Maximum
TX Input Power	-22 dBm
Drain Voltage	3.5 V
Junction Temperature[4,5]	+150°C
Operating Temperature	-40°C to +85°C

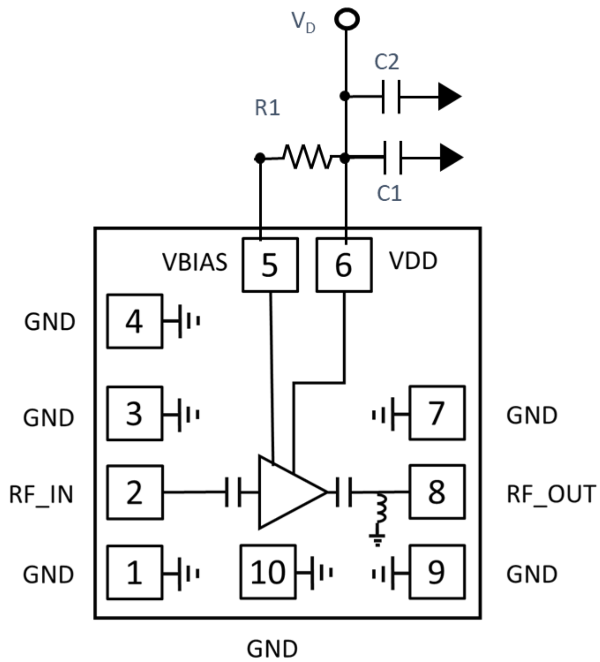
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A (250 V) devices.

Application Schematic



Parts List

Part	Value	Case Style
C1	100 pF	Chip Cap
C2	0.1 µF	0402
R1	-	0402

Operating the MAAL-011265-DIE

Turn-on

1. Apply V_D (+2 V)
2. Apply RF_{IN} signal

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_D to 0 V

Application Circuit and Operation

The basic application circuit is shown below. Place C1 capacitor as close to the MMIC as physically possible. The position of the C2 capacitor is not as critical but should also be placed as closely as practically possible.

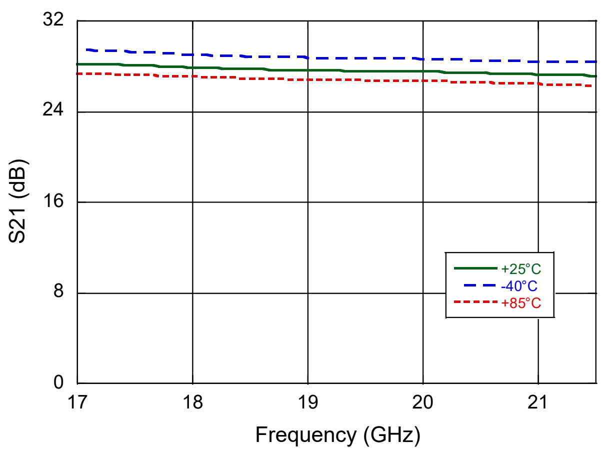
Set IDQ by adjusting R1

The value of R1 sets IDQ according to the table below:

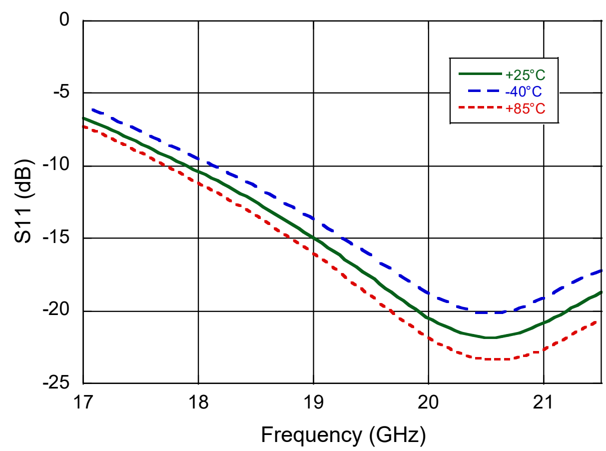
R1 (Ω)	IDQ (mA)
8K	10
4K	15
2.4K	20
1.7K	25
1.25K	30
950	35
780	40
640	45
540	50

Typical Performance Curves over Temperature @ V_D = 2 V, I_D = 25 mA, Z_0 = 50 Ω

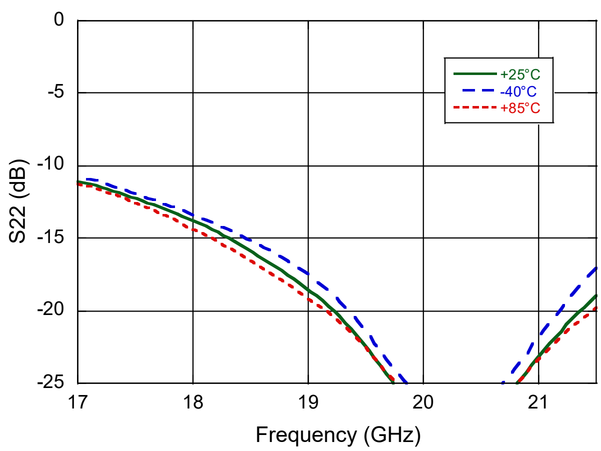
Gain



Input Return Loss

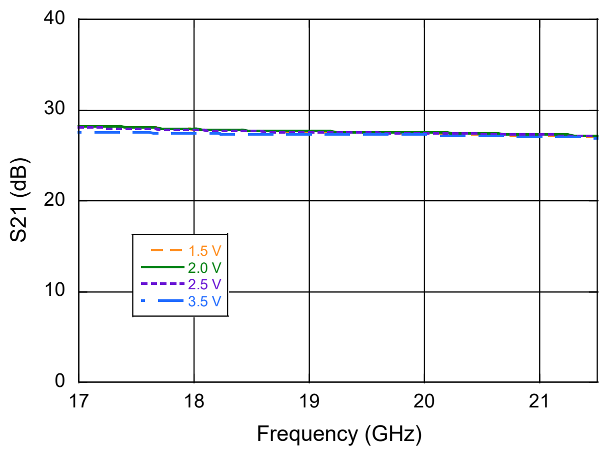


Output Return Loss

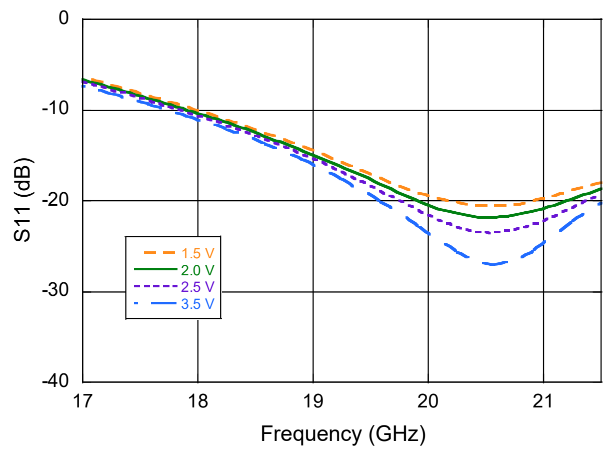


Typical Performance Curves @ I_D = 25 mA, Z_0 = 50 Ω

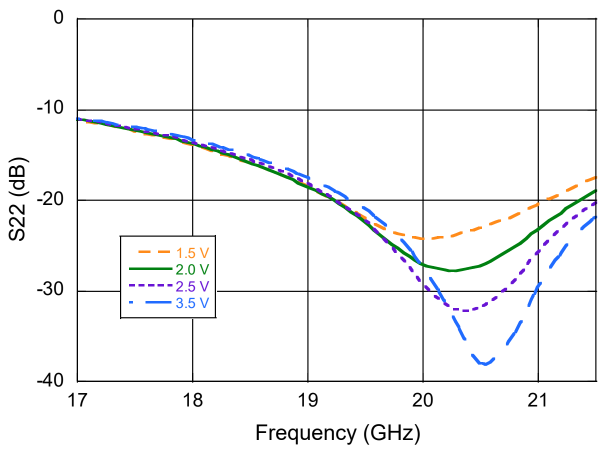
Gain



Input Return Loss

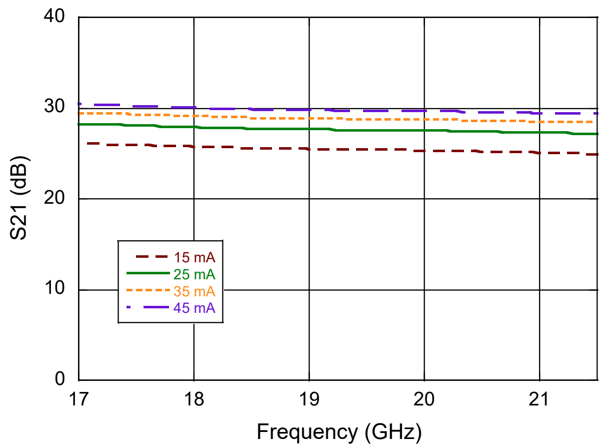


Output Return Loss

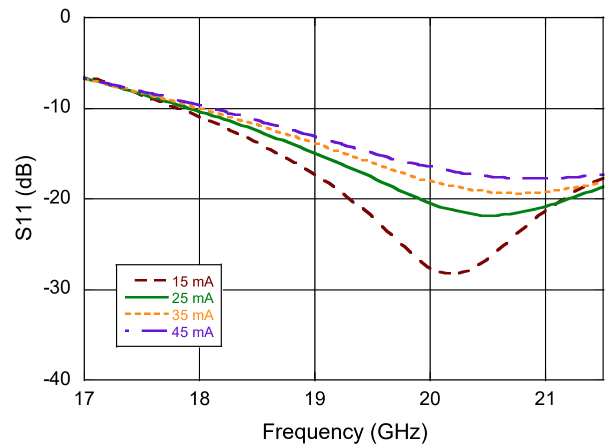


Typical Performance Curves @ V_D = 2 V, Z_0 = 50 Ω

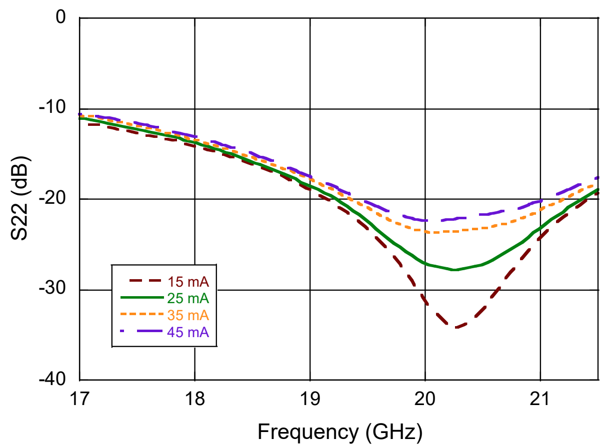
Gain



Input Return Loss

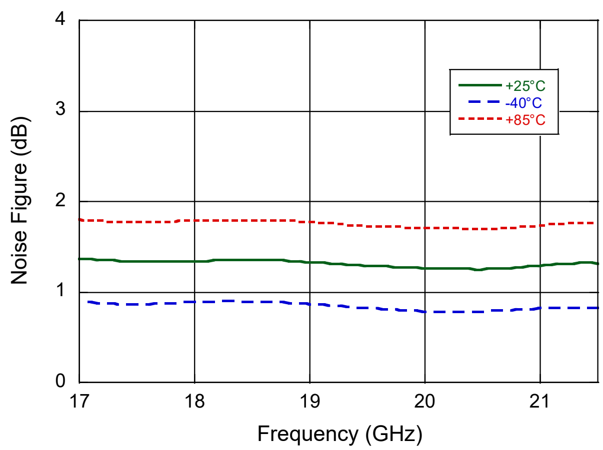


Output Return Loss

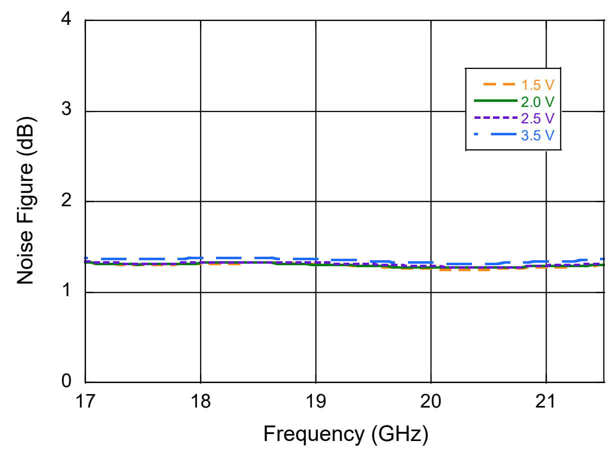


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, 25°C, Z_0 = 50 Ω

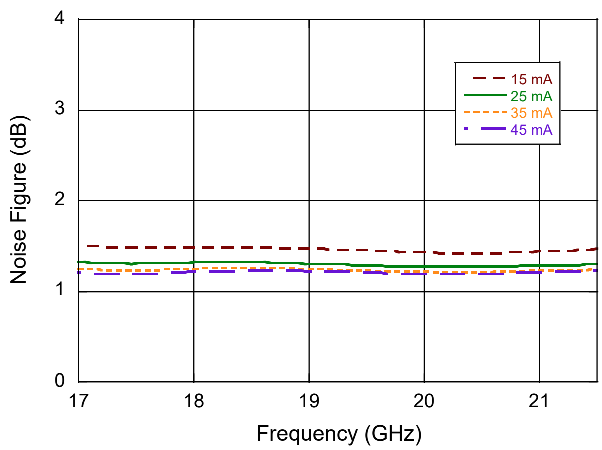
Noise Figure over Temperature



Noise Figure over Voltage

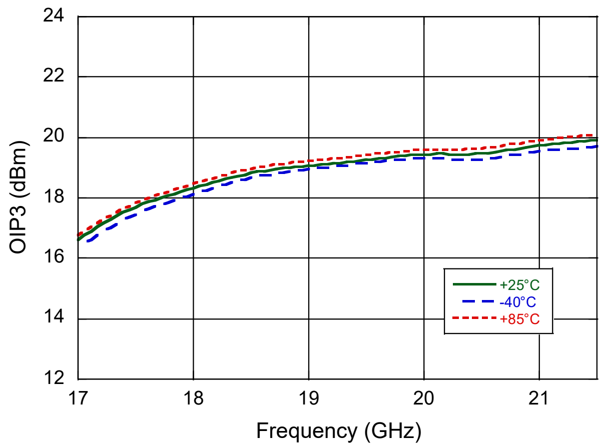


Noise Figure over Current

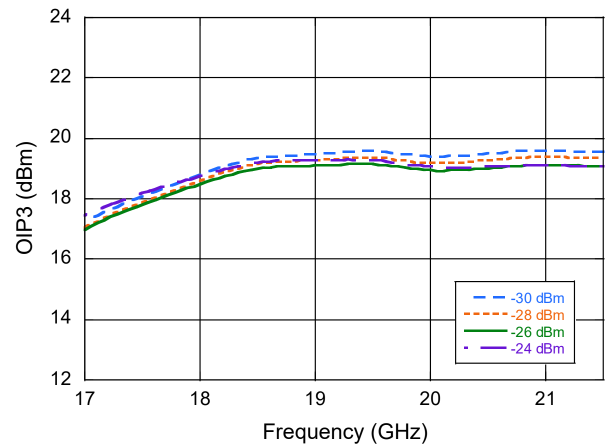


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, P_{IN} = -30 dBm, 25°C, Z_0 = 50 Ω

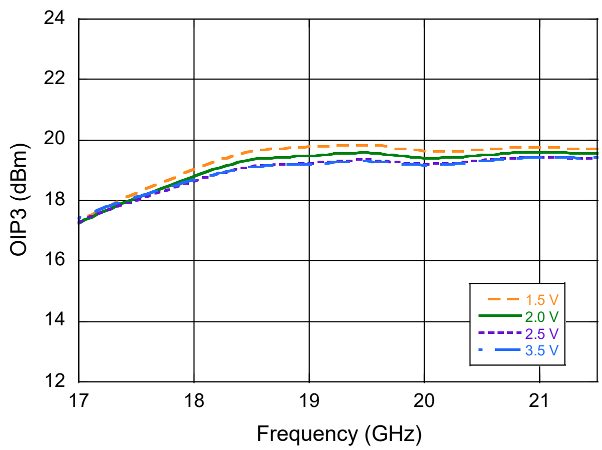
OIP3 vs Temperature



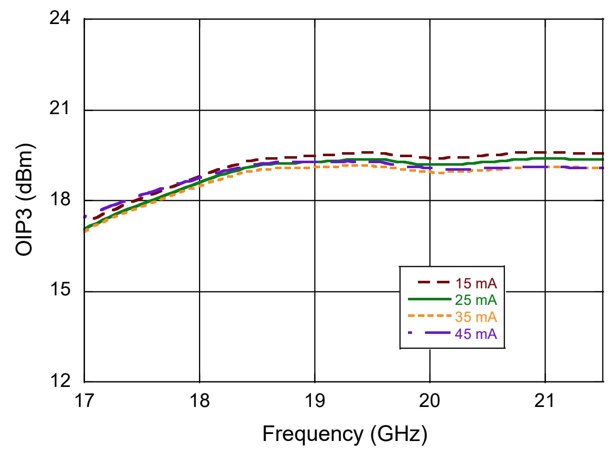
OIP3 vs Input Power



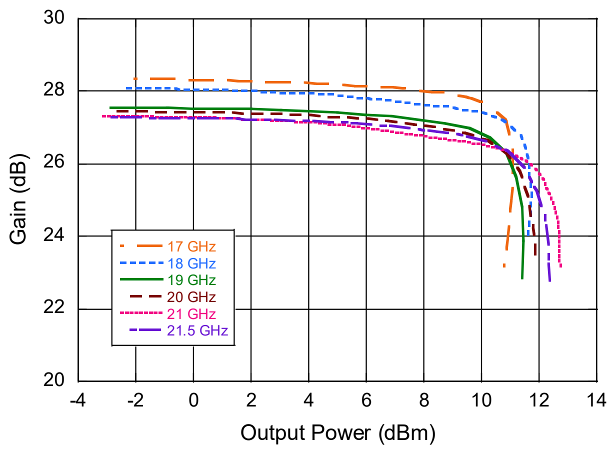
OIP3 vs Bias Voltage



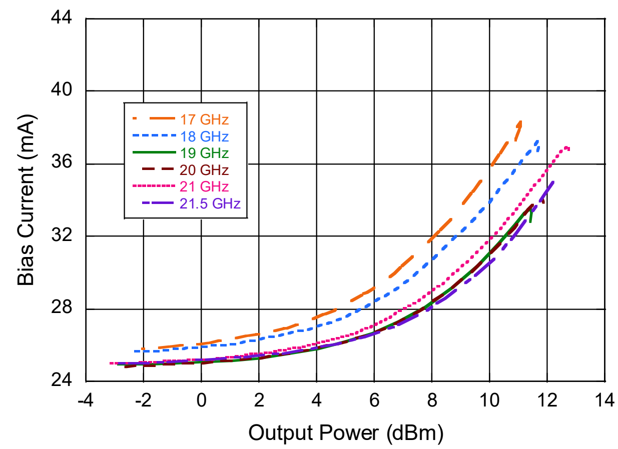
OIP3 vs Bias Current



Gain vs Output Power

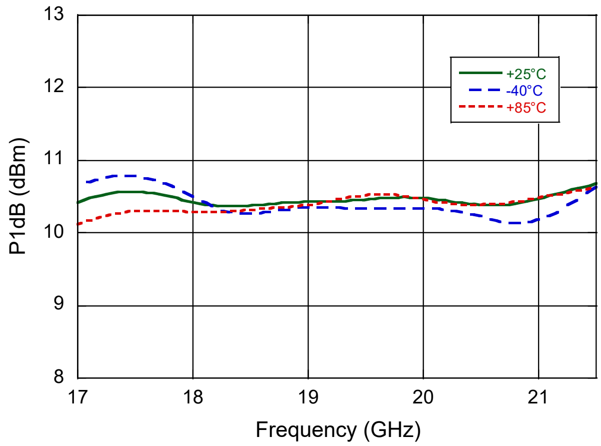


Bias Current vs Output Power

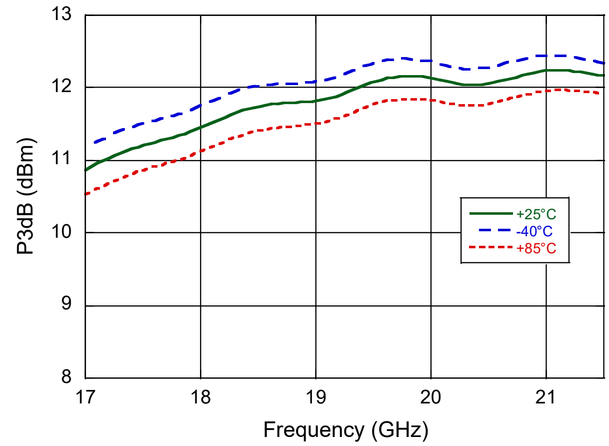


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, 25°C, Z_0 = 50 Ω

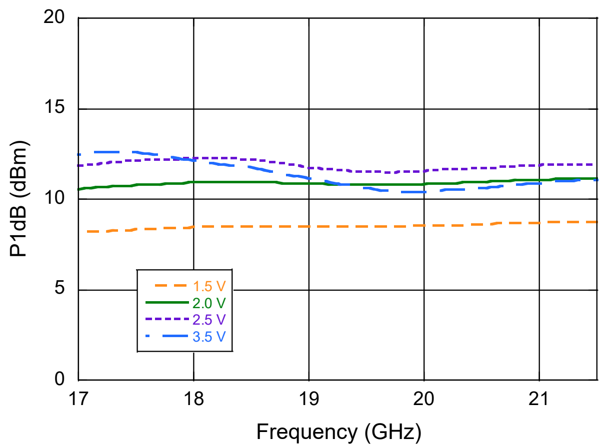
P1dB vs Temperature



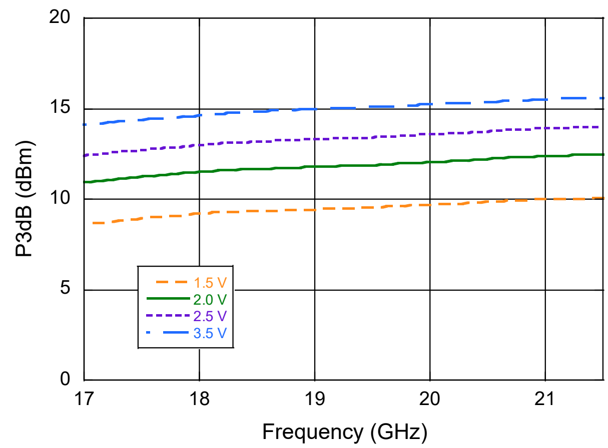
P3dB vs Temperature



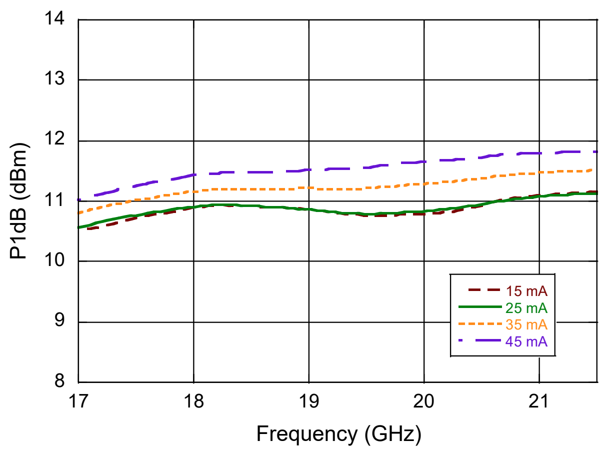
P1dB vs Bias Voltage



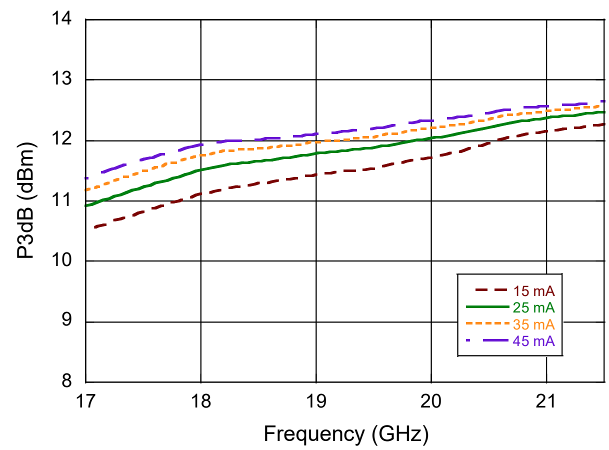
P3dB vs Bias Voltage



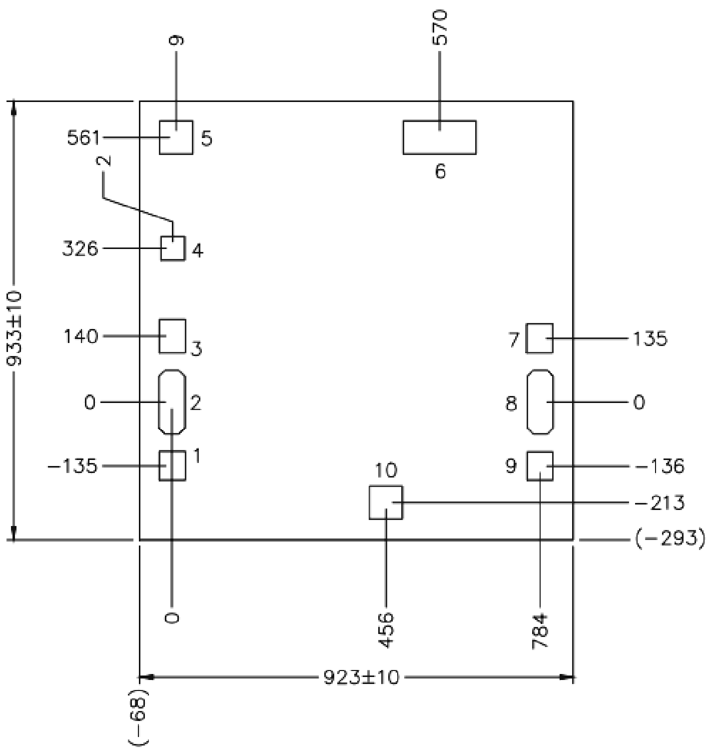
P1dB vs Bias Current



P3dB vs Bias Current



Chip Outline Drawing



BOND PAD DIM. (µm)			
PAD	X	Y	PIN LABEL
1,7,9	55	60	GND
2	55	135	RFIN
3	55	70	GND
4	50	50	GND
5	70	70	VBIAS
6	155	70	VDD
8	55	135	RFOUT
10	70	70	GND

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS SHOWN ARE µm WITH A TOLERANCE OF ±5µm.
2. DIE THICKNESS IS 100 ±10µm
3. BOND/PAD BACKSIDE METALLIZATION: GOLD
4. DIE SIZE REFLECTS FINAL DIMENSIONS.