Two-stage Low Noise Amplifier with Bypass 1.4 - 6.5 GHz

MAAL-011243
Rev. V1

Features

- Broadband 2-stage LNA
- Second LNA has Bypass Mode
- Gain at High Gain Mode:
  34 dB at 3.5 GHz, 32 dB at 5.9 GHz
- Gain at Low Gain Mode:
  20 dB at 3.5 GHz, 17 dB at 5.9 GHz
- Noise Figure:
  0.9 dB at 3.5 GHz, 1.6 dB at 5.9 GHz
- Output IP3:
  35 dBm at High Gain Mode
  30 dBm at Low Gain Mode
- Single 5 V Supply
- Power Down Pin with 1.8 V / 3.3 V Logic
- Low DC Current: 110 mA
- Lead-Free 4x4 mm 24 Lead QFN Package
- RoHS* Compliant

Applications

- 5G TDD and FDD Base Station
- Automotive V2X
- General Purpose Wireless

Description

The MAAL-011243 is a compact surface mount, highly integrated 2-stage low noise amplifier (LNA) module with Bypass function on the second stage. This module operates from 1.4 – 6.5 GHz and features low noise figure, high linearity and low power consumption. MAAL-011243 requires a single 5 V supply and the internal digital logic is 1.8 V and 3.3V CMOS compatible.
are used to achieve high power handling, low noise figure, and low power consumption. The module only needs a single +5 V supply. T/R switch, LNA enable, and bypass function can be controlled with 1.8 V or 3.3 V logic.

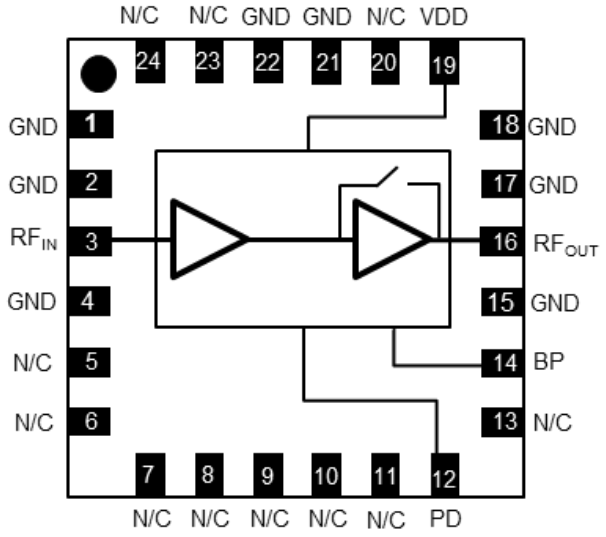
Ordering Information[1]

Part Number	Package
MAAL-011243-TR1000	1000 Piece Reel
MAAL-011243-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Functional Schematic



Pin function[2]

Pin #	Function
1, 2, 4, 15, 17, 18, 21, 22	Ground
3	RF Input
5-11,13, 20, 23, 24	N/C
12	Power Down Logic Control
14	Bypass Logic Control
16	RF Output
19	DC Supply Voltage
25	Paddle[3]

2. MACOM recommends connecting unused package pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Pin Description

Pin #	Name	Description
1, 2, 4, 15, 17, 18, 21, 22	GND	These pins are grounded internally.
3	RF_{IN}	RF Input Pin, external DC block required.
5-11,13, 20, 23, 24	N/C	Not connected internally. It is recommended to connect N/C pins to RF grounds of the PCB.
12	PD	Power down both stages of LNA.
14	BP	Bypass for second stage of the LNA.
16	RF_{OUT}	RF output pin, external DC block required.
19	VDD	5V Supply pin. Needs external decoupling capacitors.
25	Paddle	Exposed Pad. The exposed pad must be connected to RF, DC and thermal ground.

AC Electrical Specifications: Freq. = 3.5 GHz, T_C = 25°C, VDD = +5 V, Z_0 = 50 Ω, P_{IN}= -30 dBm (unless otherwise stated)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain at High Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	32.5 31.5 29.5 —	35 34 32 32	—
NF at High Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	—	0.8 0.9 1.3 1.7	—
Input RL at High Gain Mode		dB	—	10	—
Output RL at High Gain Mode		dB	—	12	—
Output IP3 at High Gain Mode	Tone Spacing = 10 MHz P_{OUT} / Tone = +10 dBm	dBm	—	36	—
Output P1dB at High Gain Mode		dBm	—	19.5	—
Gain at Low Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	17.5 17.5 16.5 —	20 20 19 17	—
NF at Low Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	—	0.7 0.9 1.3 1.6	—
Input RL at Low Gain Mode		dB	—	10	—
Output RL at Low Gain Mode		dB	—	13	—
Output IP3 at Low Gain Mode	Tone Spacing = 10 MHz P_{OUT} / Tone = +3 dBm	dBm	—	32	—
Output P1dB at Low Gain Mode		dBm	—	15	—
Power Consumption	High Gain Mode Low Gain Mode Off state	W	—	0.55 0.23 0.008	—
Reverse Isolation	High Gain Mode Low Gain Mode	dB	—	50 35	—
Off State Isolation	Off state	dB	—	55	—

DC Electrical Specifications: Freq. = 3.5 GHz, T_C = 25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	4.75	5.0	5.25
Supply Current (V_{DD}) per Channel	Rx High Gain Rx Low Gain Off Current	mA	—	110 45 1.3	—
Control Voltage	Logic High Logic Low	V	1.2 0	—	3.45 0.6
Logic Input Current	Logic High Logic Low	µA	-80	—	80
RF Switching Time	50% CTL to 10/90% RF	ns	—	120	—
High/Low Gain Mode Switching Time	50% CTL to 10/90% RF	ns	—	150	—

Control Truth Table

Mode	PD	BP	Note
High Gain Mode	Low or open	Low or Open	HGM[4]
Low Gain Mode	Low or open	High	LGM[5]
Power Down	High	High, Low, or Open	Power down

4. HGM: High Gain Mode.
5. LGM: Low Gain Mode.

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
DC Supply	V_{DD}	V	4.75	5.0	5.25
Logic Pins	BP, PD	V	0	—	3.45
Junction Temperature[6,7]	T_J	°C	—	—	150
Operating Temperature[8]	T_C	°C	-40	—	+105

Absolute Maximum Ratings[9,10]

Parameter	Symbol	Unit	Min.	Max.
RF Input Power	RF_{IN}	dBm	—	23 dBm LTE, 26 dBm CW
DC Voltages	RF_{IN}, RF_{OUT} VDD PD, BP	V	-0.3 -0.3 -0.3	+3.6 +5.5 +3.6
Functional Temperature[8]	T_C	°C	-40	+125
Storage Temperature		°C	-65	+150

6. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature $T_J = T_C + \Theta_{JC} * P_{DISS}$ where P_{DISS} is the total DC & RF dissipated power.
   Typical thermal resistance Θ_{JC} = 33.4 ºC/W.
   a) For T_C = +25°C, T_J = 43.4 °C @ 5 V, 110 mA
   b) For T_C = +105°C, T_J = 123.4 °C @ 5 V,110 mA
8. Tc is defined by exposed paddle temperature.
9. Exceeding any one or combination of these limits may cause permanent damage to this device.
10. MACOM does not recommend sustained operation near these survivability limits

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

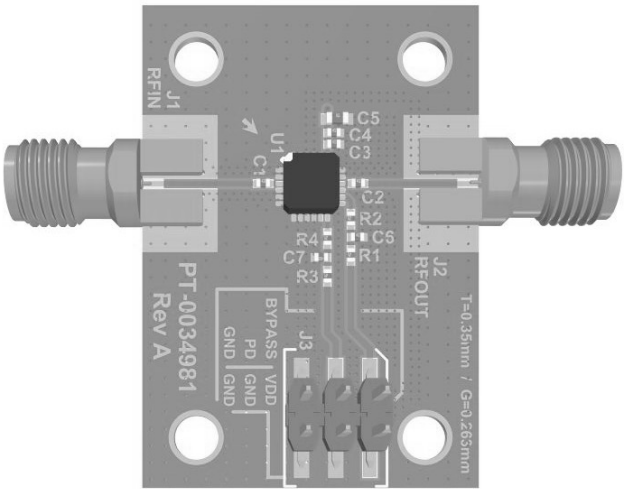
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Parameter	Rating	Standard
Human Body Model (HBM)	500 V Class 1B	ESDA/JEDEC JS-001
Charged Device Model (CDM)	500 V (Class C2a)	ESDA/JEDEC JS-002

Power Supplies

De-coupling capacitors should be placed at the V_{DD} supply pin to minimize noise and fast transients. Supply voltage change or transients should have a slew rate smaller than 1 V / 10 µs. In addition, all control pins should remain at 0 V (+/- 0.3 V) and no RF power should be applied while the supply voltage ramps or while it returns to zero.

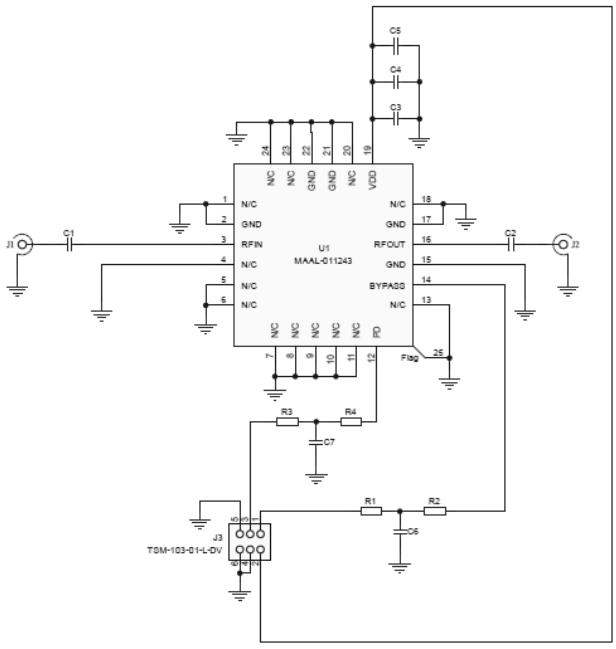
PCB Layout



Parts List

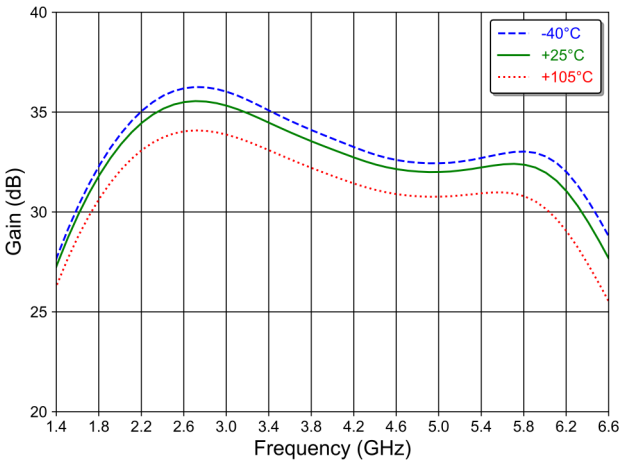
Part	Value	Case Style
C1, C2	20pF	0402
C3	470pF	0402
C4	10nF	0402
C5	1uF	0603
C6, C7	5pF	0402
R1, R3	1kΩ	0402
R2, R4	0Ω	0402

Application Schematic

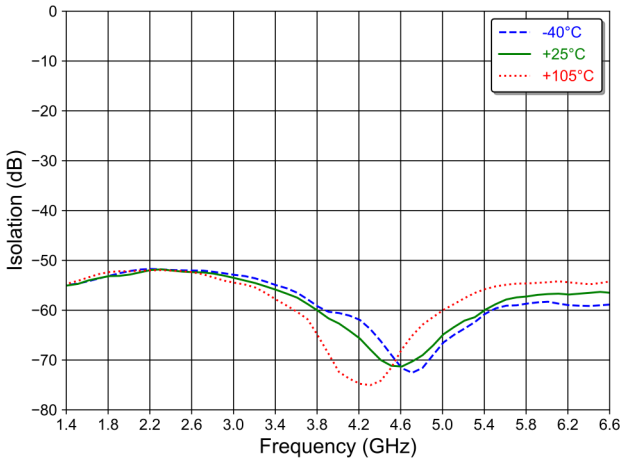


Typical Performance Curves - High Gain Mode:
P_{IN} = -30 dBm, VCC = +5 V, Z_0 = 50 Ω (unless otherwise stated)

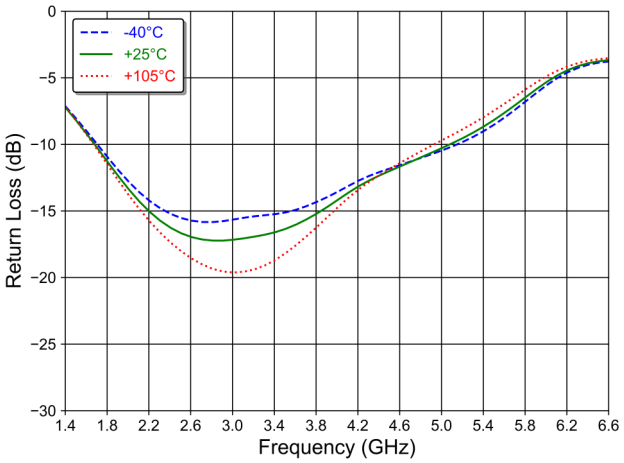
Gain[11]



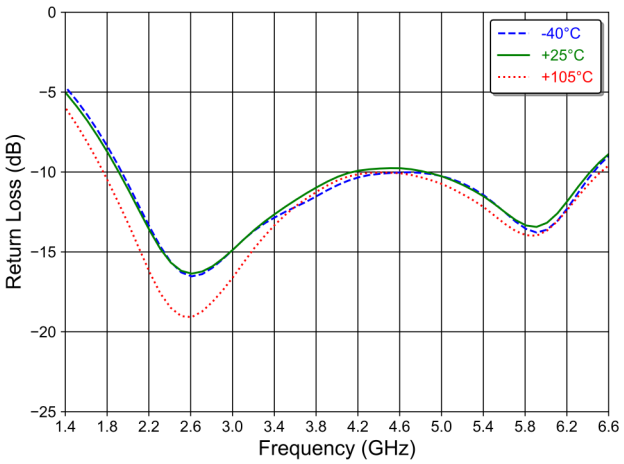
Reverse Isolation



Input Return Loss



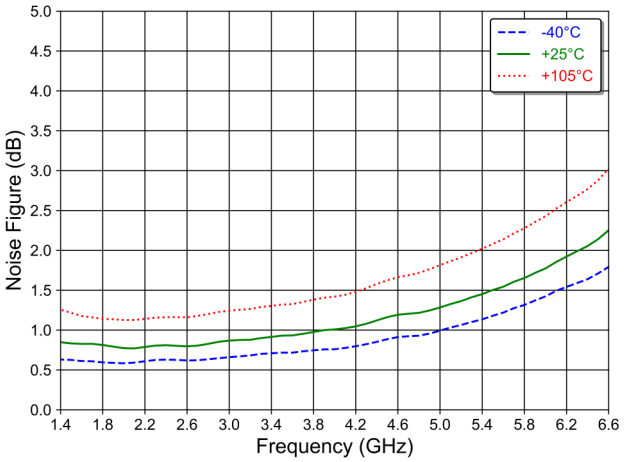
Output Return Loss



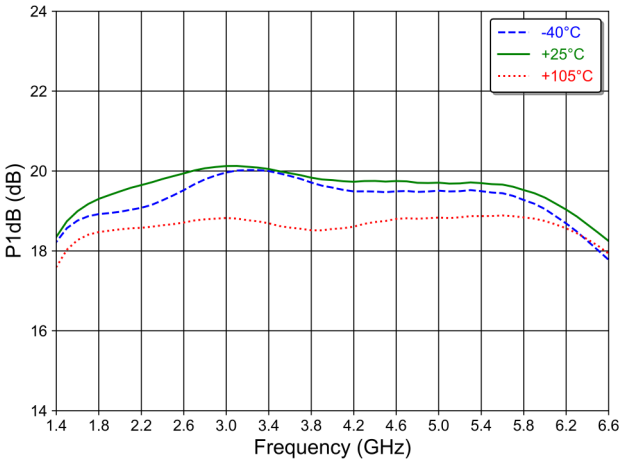
11. For Gain, Noise Figure and Gain Compression plots, RF trace and connector losses are de-embedded .

Typical Performance Curves - High Gain Mode:
P_{IN} = -30 dBm, VCC = +5 V, Z_0 = 50 Ω (unless otherwise stated)

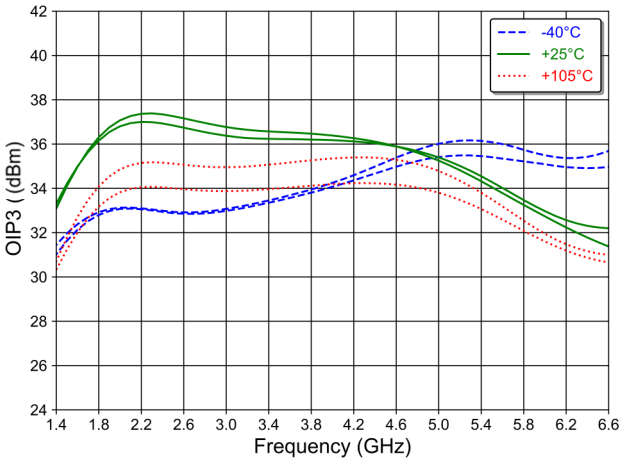
Noise Figure[11]



Gain Compression[11]

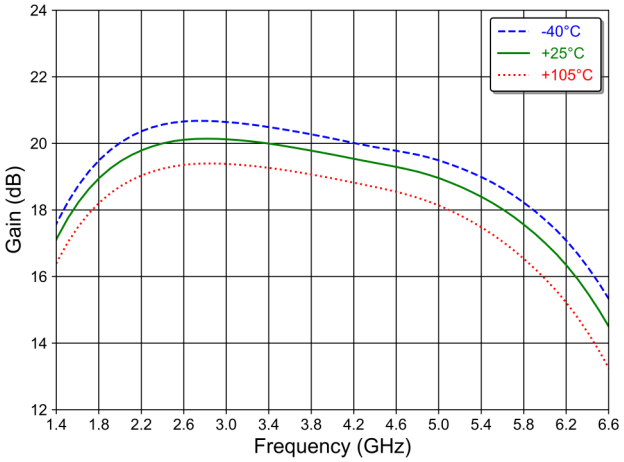


OIP3 (P_{OUT}/Tone = +10 dBm & 10 MHz tone spacing)

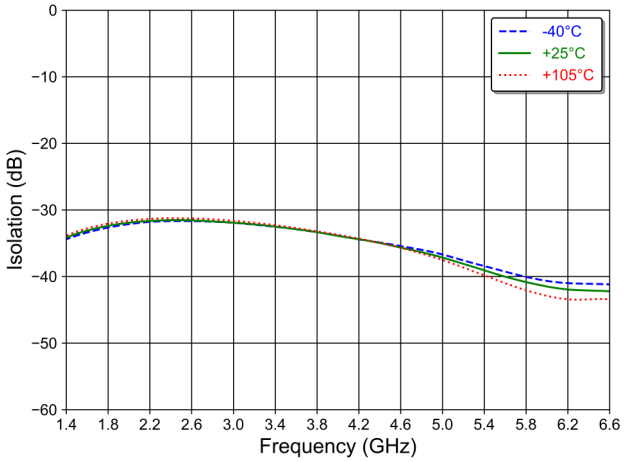


Typical Performance Curves - Low Gain Mode:
P_{IN} = -30 dBm, VCC = +5 V, Z_0 = 50 Ω (unless otherwise stated)

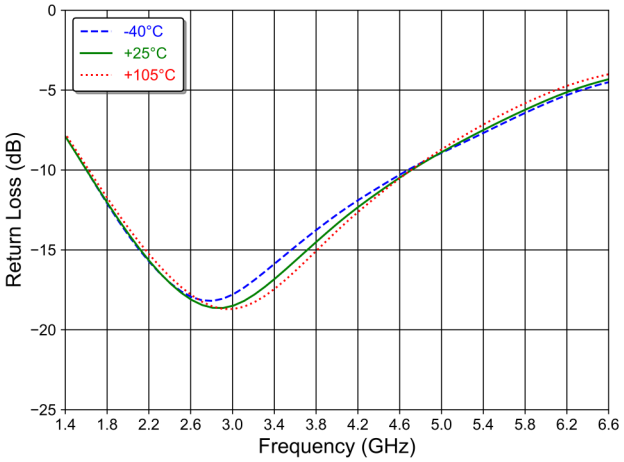
Gain[11]



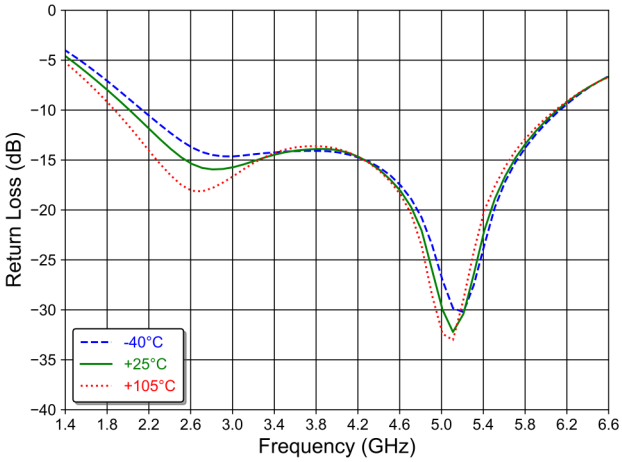
Reverse Isolation



Input Return Loss

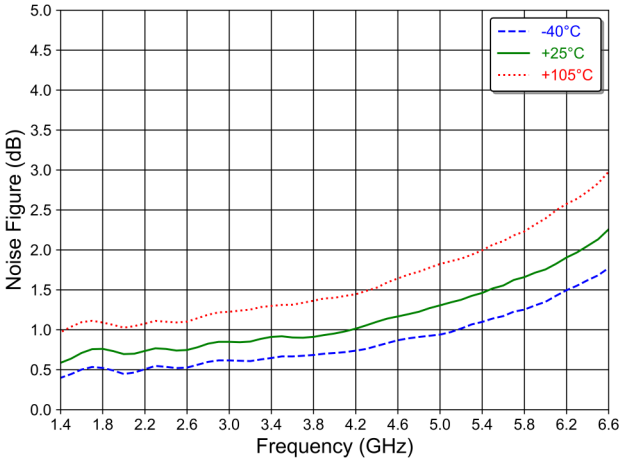


Output Return Loss

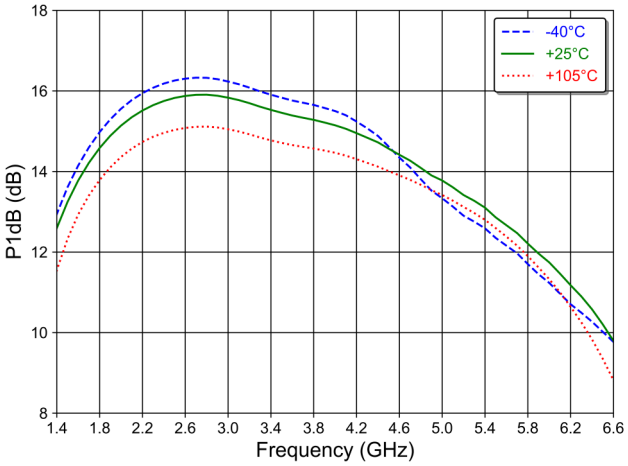


Typical Performance Curves - Low Gain Mode:
P_{IN} = -30 dBm, VCC = +5 V, Z_0 = 50 Ω (unless otherwise stated)

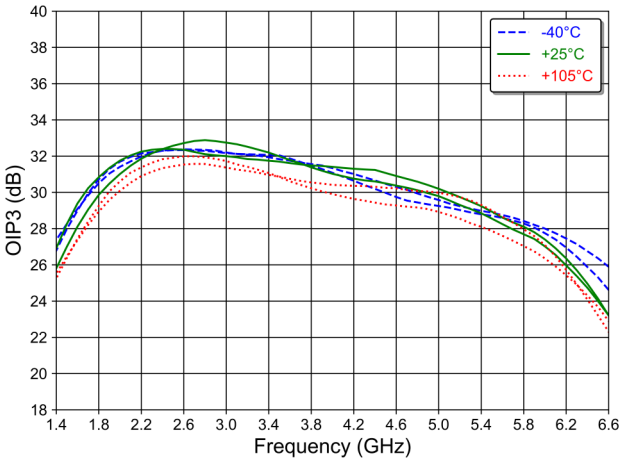
Noise Figure[11]



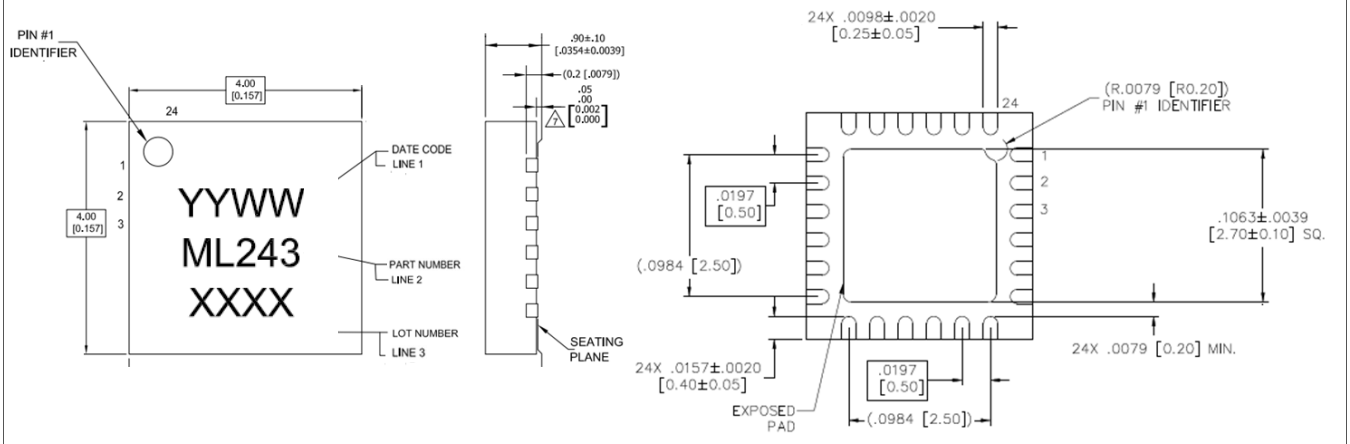
Gain Compression[11]



OIP3 (P_{OUT}/Tone = +3 dBm & 10 MHz tone spacing)



Lead-Free 4 mm 24-Lead PQFN†



Notes:
1. Dimensions are in mm [in]
2. Reference JEDEC MO-220 for additional dimensional and tolerance information

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level MSL-1 requirements.
Plating is NiPdAuAg

Revision History

Rev	Date	Change Description
V1	27/09/23	
V2		
V3		