Features

- Low Noise Figure: 1.5 dB
- Gain: 30 dB
- P1dB: +11 dBm
- Bias Voltage: V_{DD} = 2 V
- Bias Current: I_{DSQ} = 25 mA
- 50 Ω Matched Input and Output
- 2 mm DFN 8-Lead Package
- RoHS* Compliant

Applications

- Satellite Communications
- Low Earth Orbit Space Payloads
- GEO High Throughput Satellite
- Radar
- EW

Description

The MAAL-011238 is an easy to use low noise amplifier. It operates from 27 GHz to 31.5 GHz and provides 1.5 dB noise figure, 30 dB gain and a P1dB of 11 dBm. The input and output are fully matched to 50 Ω with typical return loss >10 dB. This part is a packaged in a 2 mm DFN 8-Lead Package.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

The MAAL-011238 can be used as a low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Ka-band satellite communication systems.

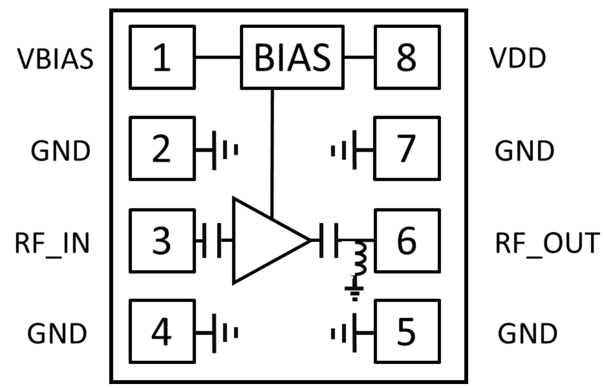
The MAAL-011238 is also available in die form under MAAL-011238-DIE part number.

Ordering Information

Part Number	Package
MAAL-011238-TR3000	Bulk
MAAL-011238-SB1	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



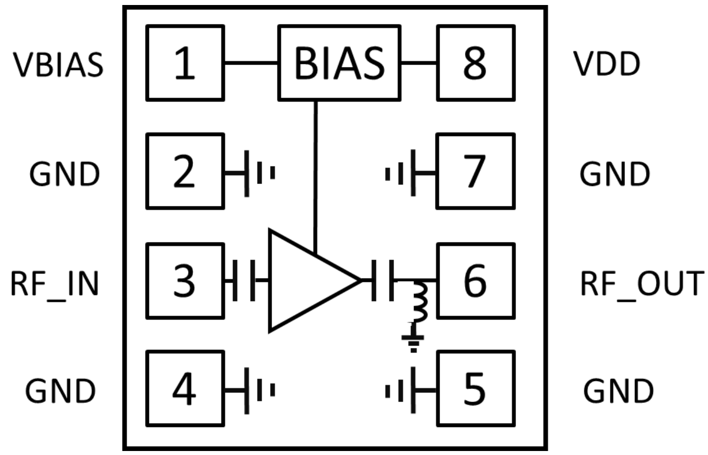
Pin Configuration

Pin #	Function	Description
1	VBIAS	Bias Voltage
2, 4, 5, 7	GND	Ground
3	RF_{IN}	RF Input
6	RF_{OUT}	RF Output
8	VDD	Drain Supply
Paddle	GND[2]	Ground

2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1	VBIAS	A voltage can be applied to this pin to set the required IDSQ as described in the application section
2,4,5,7	GND	These pins are grounded internally. It is recommended these are grounded on the application PCB.
3	RF_IN	RF Signal Input. This pad is matched to 50 Ω and is AC coupled
6	RF_OUT	RF Signal Output. This pad is matched to 50 Ω and is AC coupled. There is a shunt inductor to ground providing a DC ground path.
8	VDD	Drain bias for the amplifier. External bypass capacitors are required as described in the applications schematic.
Paddle		RF, DC and thermal ground

Electrical Specifications: Freq. = 27.0 - 31.5 GHz, T_A = 25°C, V_D = 2 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	P_{IN} = -30 dBm 27.0 GHz 31.5 GHz	dB	 27.5 26.0	 30.5 29.0	—
Small Signal Gain Variation over Temperature	—	dB/°C	—	0.02	—
Gain Flatness	—	dB	—	0.5	—
Noise Figure	—	dB	—	1.5	—
Input Return Loss	—	dB	—	10	—
Output Return Loss	—	dB	—	10	—
P1dB	27.0 GHz 31.5 GHz	dBm	8.5 10.0	10.5 12.0	—
Output 3rd Order Intercept	P_{IN} = -26 dBm/tone, 10 MHz spacing	dBm	—	20	—
Supply Current	—	mA	—	25	—

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Input Power	18 dBm
Drain Voltage	4 V
Junction Temperature[5,6]	+160°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1×10^6 hours.
6. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 93 °C/W.
   a) For T_C = +25°C,
      T_J = 30 °C @ 2 V, 25 mA
   b) For T_C = +85°C,
      T_J = 90 °C @ 2 V, 25mA

Maximum Operating Conditions

Parameter	Maximum
TX Input Power	-14 dBm
V_{DD}	3.5 V
Junction Temperature[5,6]	+150°C
Operating Temperature	-40°C to +85°C

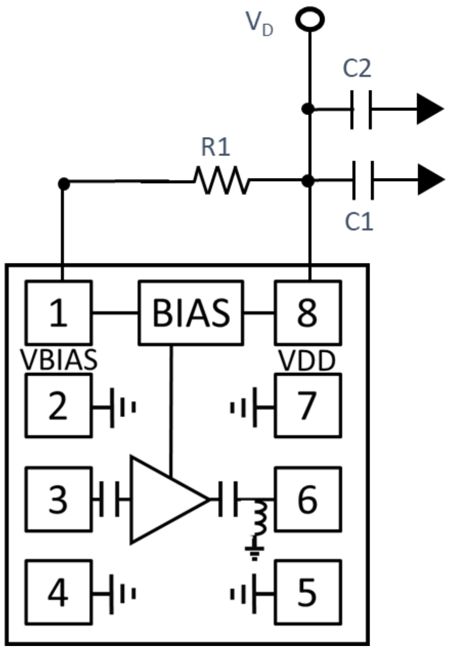
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A (250 V), class C2a (500 V) CDM devices.

Application Schematic



Parts List

Part	Value	Case Style
C1	100 pF	0402
C2	0.1 µF	0402
R1	-	0402

Operating the MAAL-011238

Turn-on

1. Apply V_D (+2 V)
2. Apply RF_{IN} signal

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_D to 0 V

Application Circuit and Operation

The basic application circuit is shown below. Place C1 capacitor as close to the package as physically possible. The position of the C2 capacitor is not as critical but should also be placed as closely as practically possible.

To ensure proper grounding the number of ground vias under the device should be maximized (within practical limits imposed by the PCB vendor).

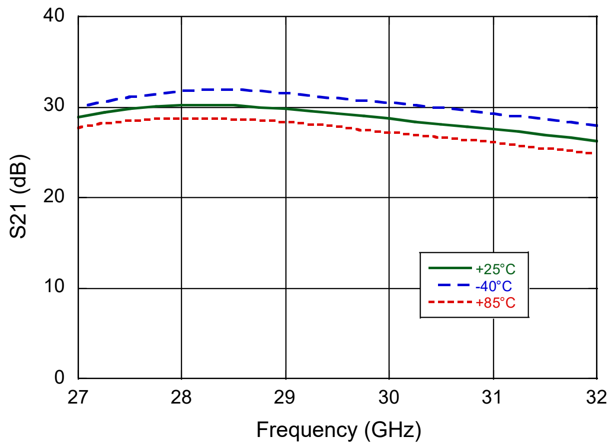
Set IDQ by adjusting R1

The value of R1 sets IDQ according to the table below:

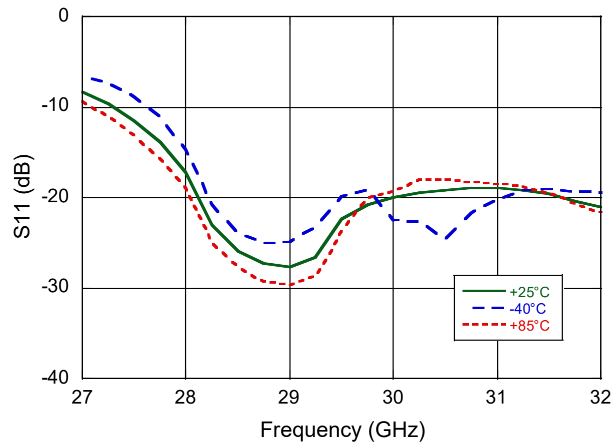
R1 (Ω)	IDQ (mA)
100	74
200	46
300	35
400	28
500	24
600	21
700	19
800	17
900	15.5

Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, Z_0 = 50 Ω

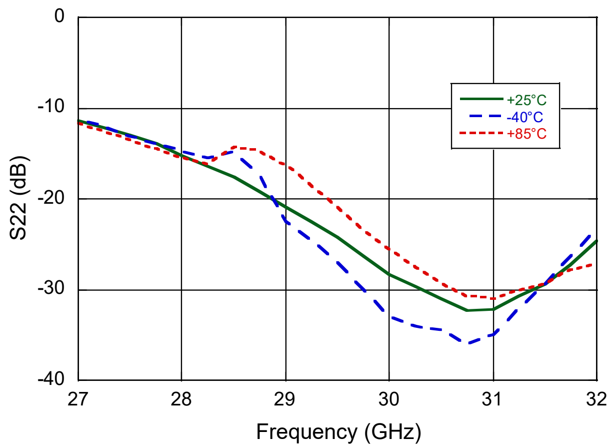
Gain



Input Return Loss

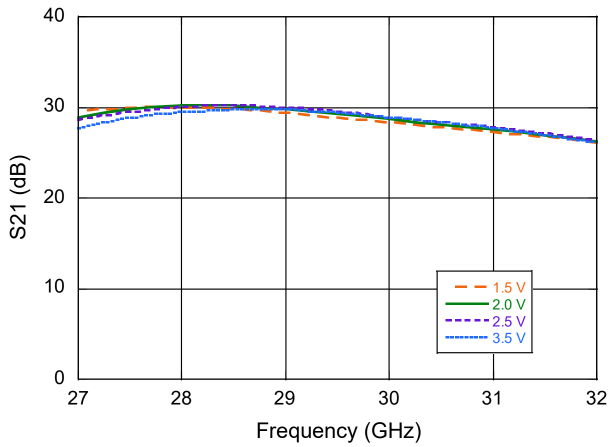


Output Return Loss

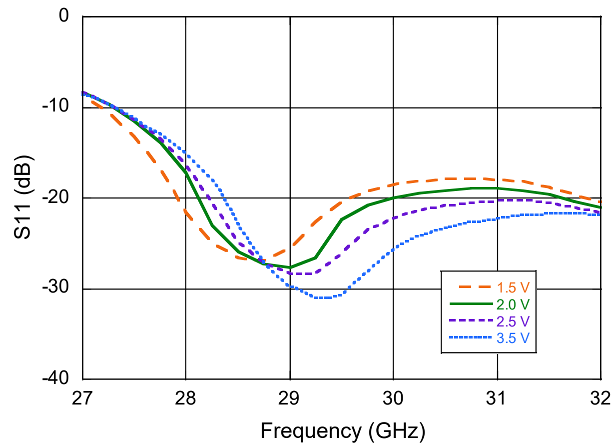


Typical Performance Curves @ I_D = 25 mA, Z_0 = 50 Ω

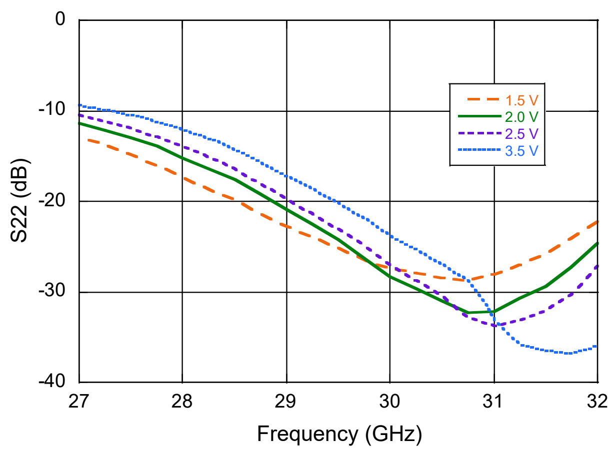
Gain



Input Return Loss

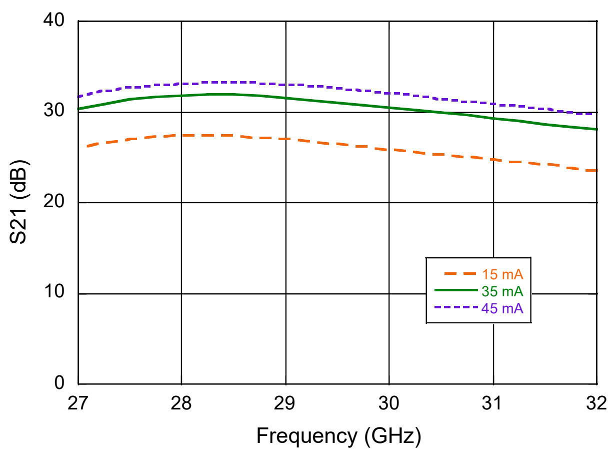


Output Return Loss

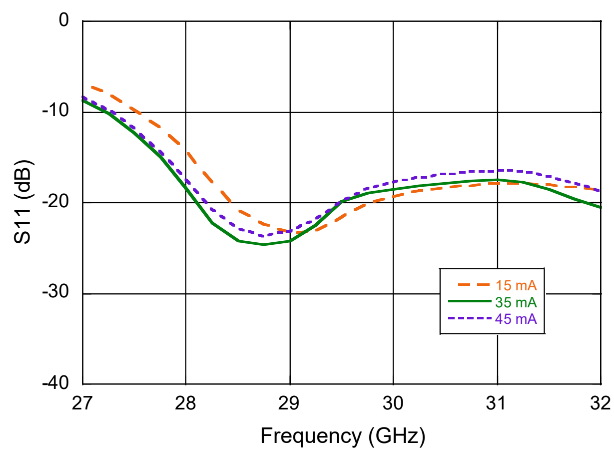


Typical Performance Curves @ V_D = 2 V, Z_0 = 50 Ω

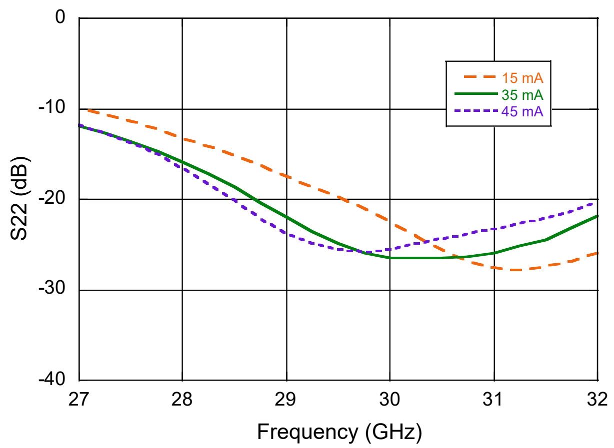
Gain



Input Return Loss

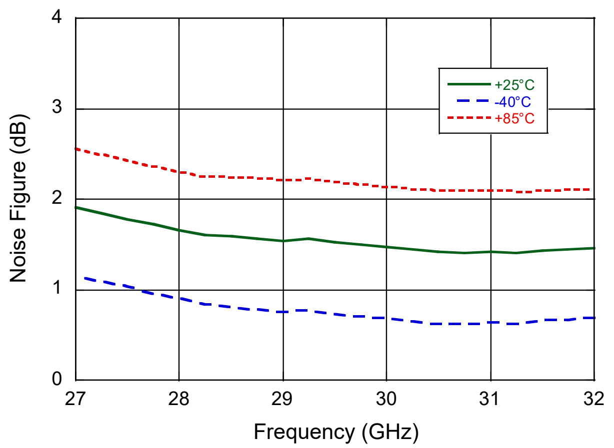


Output Return Loss

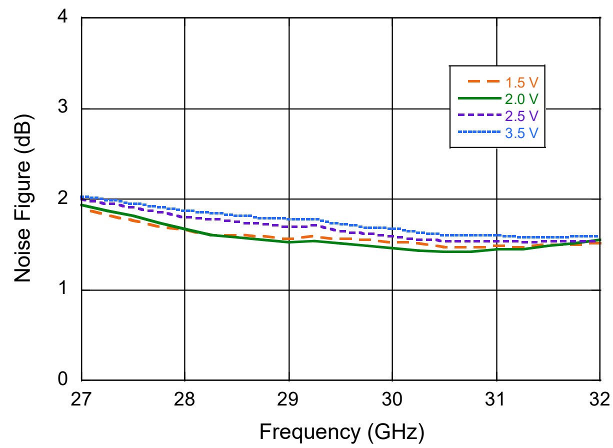


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, 25°C, Z_0 = 50 Ω

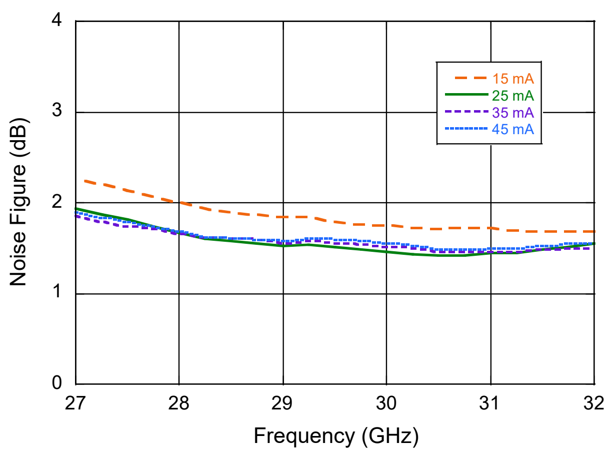
Noise Figure over Temperature



Noise Figure over Voltage

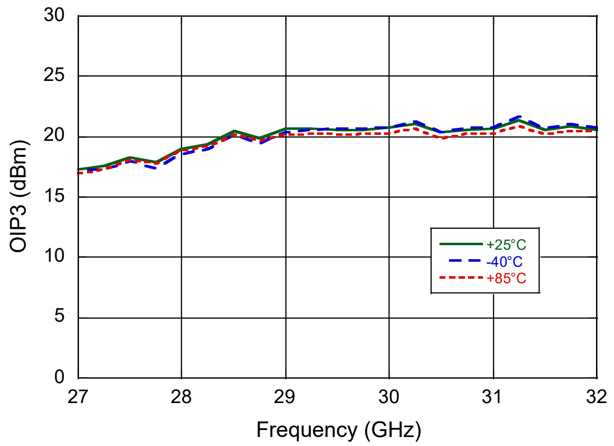


Noise Figure over Current

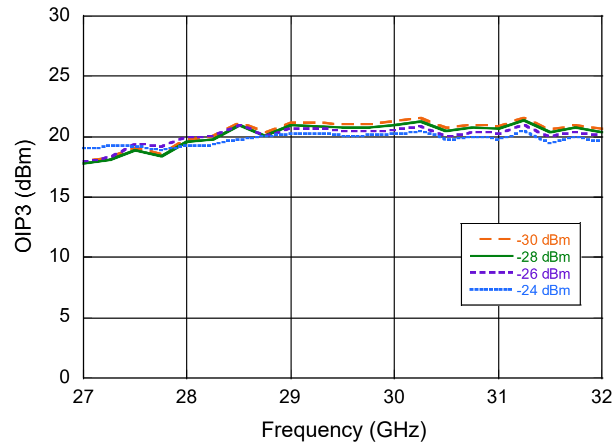


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, P_{IN} = -30 dBm, 25°C, Z_0 = 50 Ω

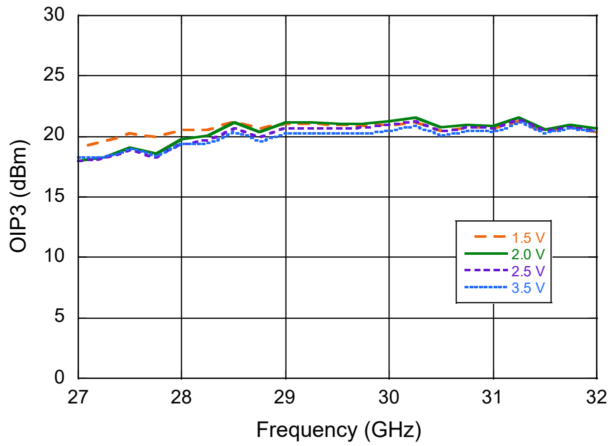
OIP3 over Temperature



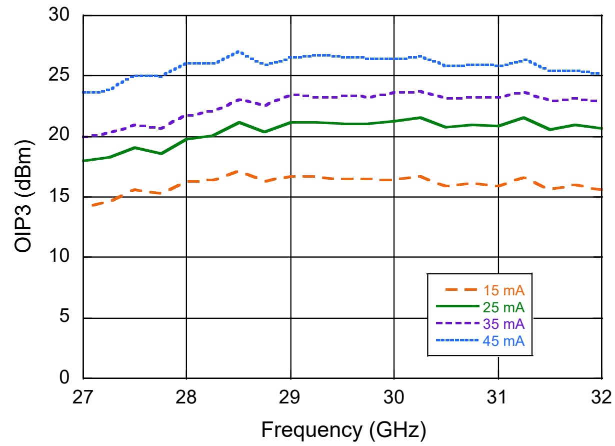
OIP3 over Input Power



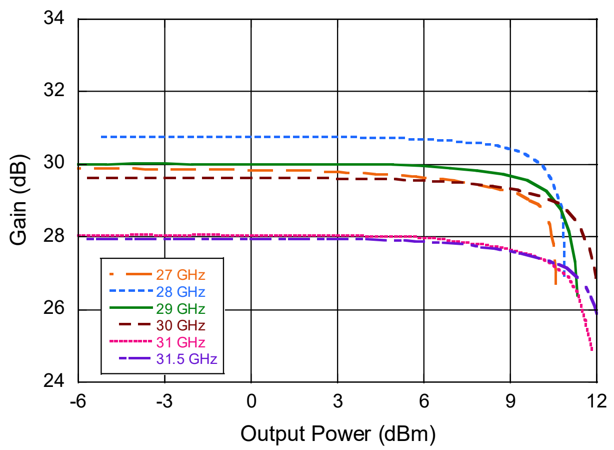
OIP3 over Bias Voltage



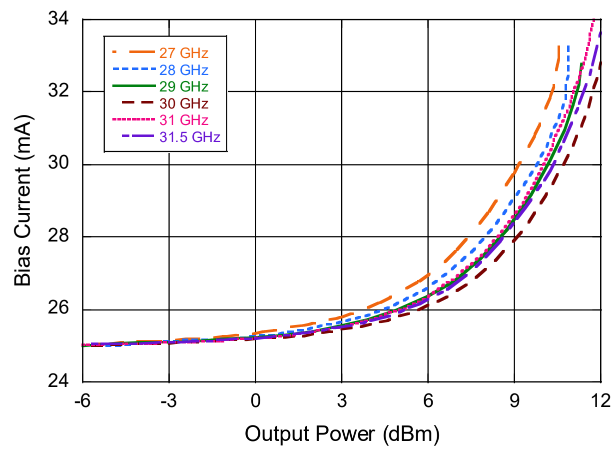
OIP3 over Bias Current



Gain vs Output Power over Frequency

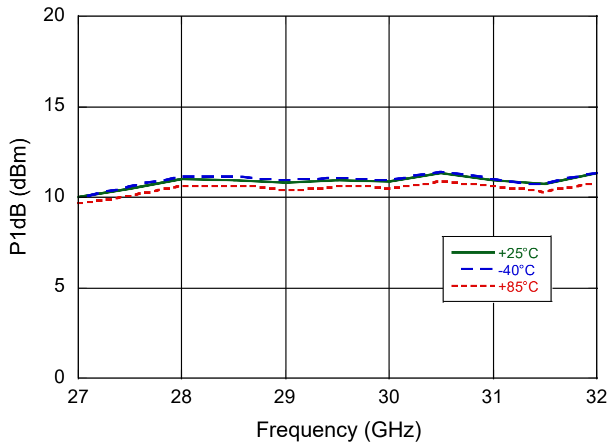


Bias Current vs Output Power over Frequency

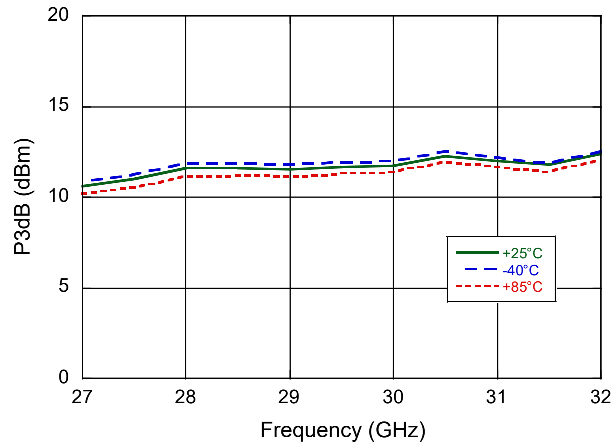


Typical Performance Curves @ V_D = 2 V, I_D = 25 mA, 25°C, Z_0 = 50 Ω

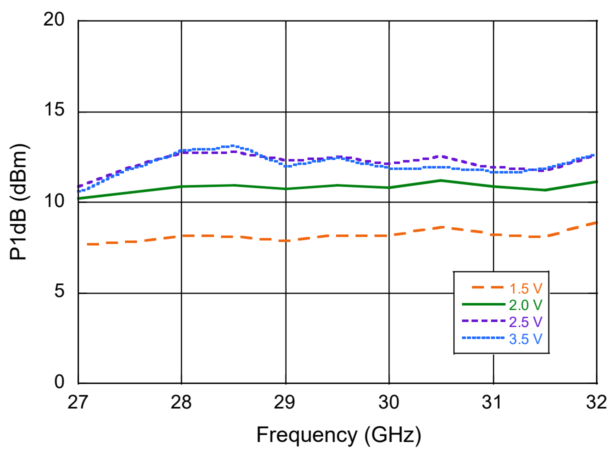
P1dB over Temperature



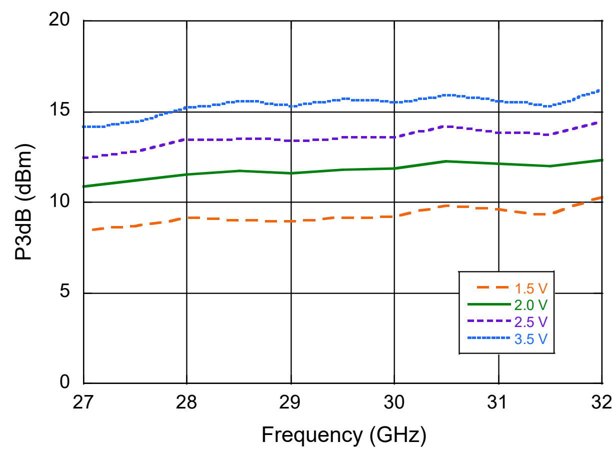
P3dB over Temperature



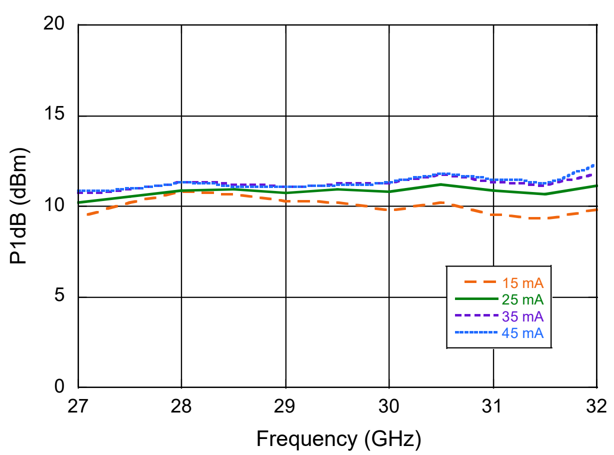
P1dB over Bias Voltage



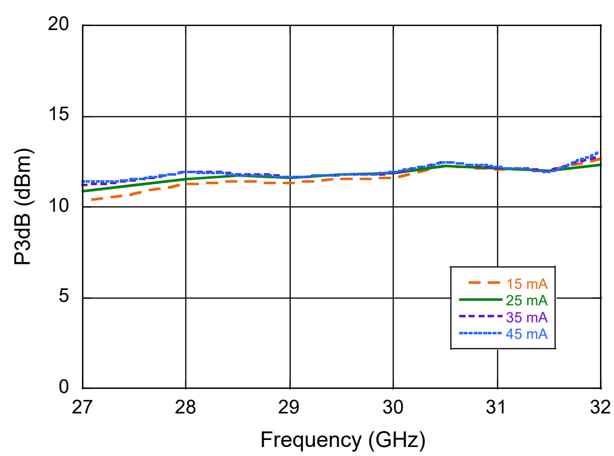
P3dB over Bias Voltage



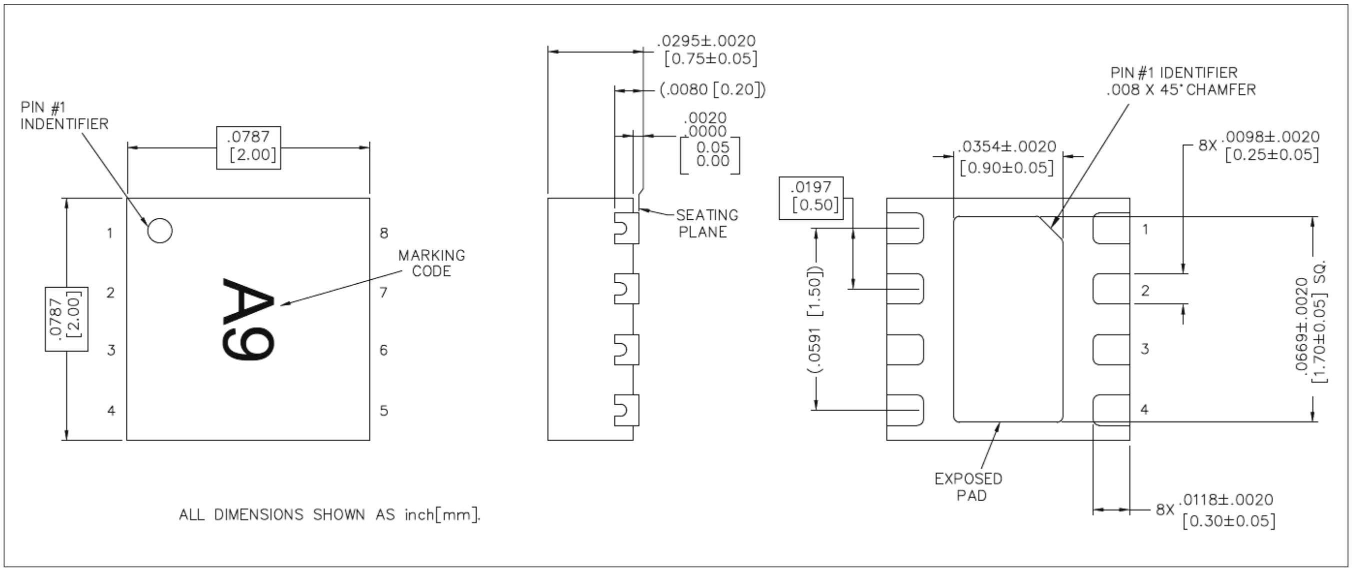
P1dB over Bias Current



P3dB over Bias Current



Lead-Free 2 mm DFN 8-Lead 8LD[7,8,9,10,11]



7. All units in in(mm), unless otherwise noted, with a tolerance of .xxxx = ±.0005 in and .xxx = ±.005 in.
8. Lead finish: NiPdAu plating
9. Marking: line 2 part number; line 3 wafer lot number; line 4 c = country of origin (T = Thailand), yyww = date code, N = Nickel/Palladium/ Gold plating
10. Reference Application Note S2083 for lead-free solder reflow recommendations.
11. Meets JEDEC moisture sensitivity level 1 requirements.