

Two-Stage Low Noise Amplifier

1.8 - 4.2 GHz



MAAL-011216

Rev. V2

Features

- Broadband 2-Stage LNA
- Gain:
 - 36.2 dB @ 2.5 GHz
 - 37.1 dB @ 3.75 GHz
- Noise Figure:
 - 0.65 dB @ 2.5 GHz
 - 0.75 dB @ 3.75 GHz
- Single 5 V Supply
- Power Down pin with 1.8 V logic
- Low DC Current: 100 mA
- Lead-Free 3 mm 16 Lead QFN Package
- RoHS* Compliant

Applications

- 5G Macro and Massive MIMO
- Wireless Infrastructure
- General purpose wireless
- TDD or FDD systems

Description

The MAAL-011216 is a compact surface mount, highly integrated 2-stage low noise amplifier (LNA). This LNA is housed in a lead-free 3 mm 16-lead QFN plastic package.

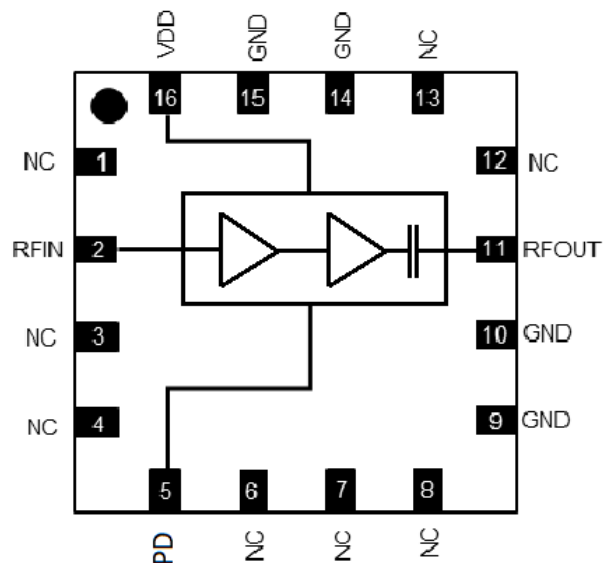
This device features low noise figure, high gain and low power consumption. The LNA requires a single 5 V supply and the Power Down pin is 1.8 V CMOS compatible.

Ordering Information¹

Part Number	Package
MAAL-011216-TR1000	1000 piece reel
MAAL-011216-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration²

Pin #	Pin Name	Description
1, 3, 4, 6 - 8, 12, 13	NC	Internally No Connect
2	RFIN	RF Input
5	PD	Logic Power Down
9, 10, 14, 15	GND	Ground
11	RFOUT	RF Output (DC Blocked)
16	VDD	Supply Voltage
17	Paddle ³	Ground

2. MACOM recommends connecting N/C pin to ground.

3. The exposed pad centered on the package bottom must be connected to PCB ground with low electrical and thermal resistances.

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DC Electrical Specifications: $T_C = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	4.75	5	5.25
Supply Current	LNA ON Mode Disable Mode	mA	—	100 1.5	—
Power Down Control Voltage	LNA ON Mode Disable Mode	V	1.073 -0.3	1.8 0	2.5 0.683
Power Down Logic Input Current	LNA ON Mode Disable Mode	μA	—	40 -2	—

AC Electrical Specifications: $P_{IN} = -30\text{ dBm}$, $T_C = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	2.5 GHz 3.75 GHz	dB	33.0 34.0	36.2 37.1	—
Gain Variation	Over Temperature	dB/ $^\circ\text{C}$	—	0.01	—
Gain Flatness	2.5 GHz, 200 MHz BW 3.75 GHz, 600 MHz BW	dB	—	0.25 0.45	—
Noise Figure	2.5 GHz 3.75 GHz	dB	—	0.65 0.75	—
Noise Figure Variation	Over Temperature, 2.5 GHz Over Temperature, 3.75 GHz	dB/ $^\circ\text{C}$	—	0.003 0.004	—
Input IP3	$P_{IN}/\text{tone} = -30\text{ dBm}$, Tone Delta = 2 MHz, 2.5 GHz 3.75 GHz	dBm	—	-1.5 -3	—
Input P1dB	2.5 GHz 3.75 GHz	dBm	—	-16 -17	—
Input Return Loss	2.5 GHz 3.75 GHz	dB	—	-13.5 -13.5	—
Output Return Loss	2.5 GHz 3.75 GHz	dB	—	-12.0 -13.0	—
Reverse Isolation	RFOUT to RFIN 2.5 GHz 3.75 GHz	dB	—	42.0 43.5	—

Transient Electrical Specifications:

Freq. = 2.5 GHz, P_{IN} = -30 dBm, T_C = 25°C, V_{DD} = 5 V, Z₀ = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
LNA ON Settling Time	Gain shall be within 0.1dB deviation from final value	µs	—	0.3	—
LNA OFF Settling Time	Power shall be within 10% from final value	µs	—	0.1	—

Power Down Truth Table

PD Control	
LNA ON Mode	Logic Low or Open
Disable Mode	Logic High

Recommended Operating Conditions

Parameter	Operation Conditions
DC Supply VDD	4.75 V to 5.25 V
Case Temperature (T _C) ⁴	-40°C to +115°C

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HMB Class 1B and CDM Class C3 devices.

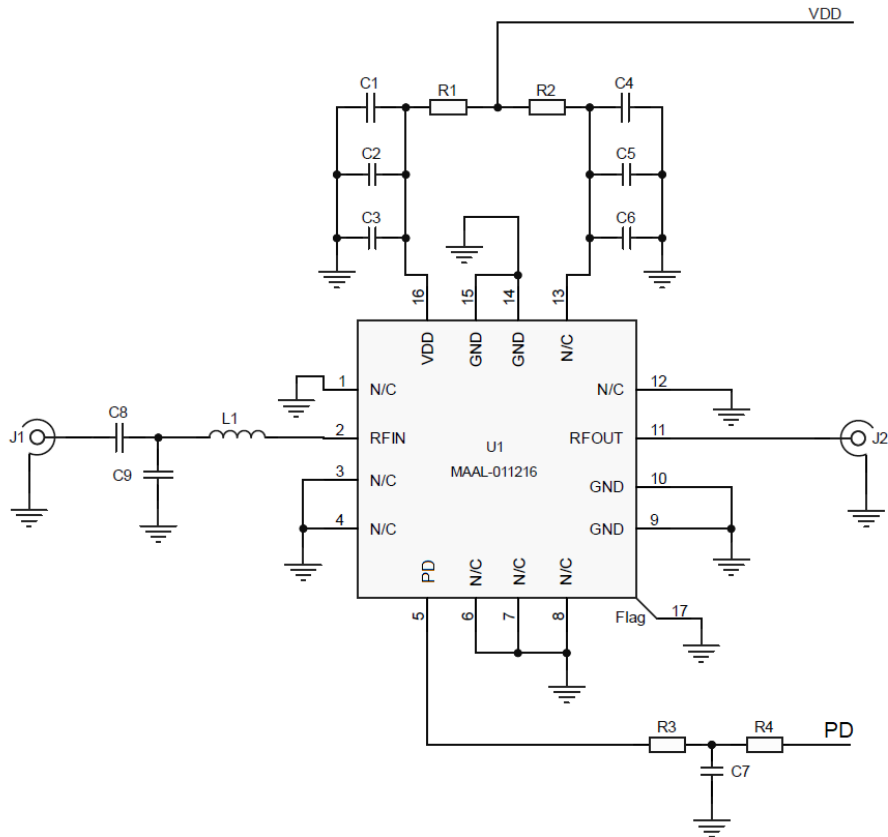
Parameter	Rating	Standard
Human Body Model (HBM)	500 V (Class 1B)	ESDA/JEDEC JS-001
Charged Device Model (CDM)	1000 V (Class C3)	ESDA/JEDEC JS-002

Absolute Maximum Ratings^{5,6}

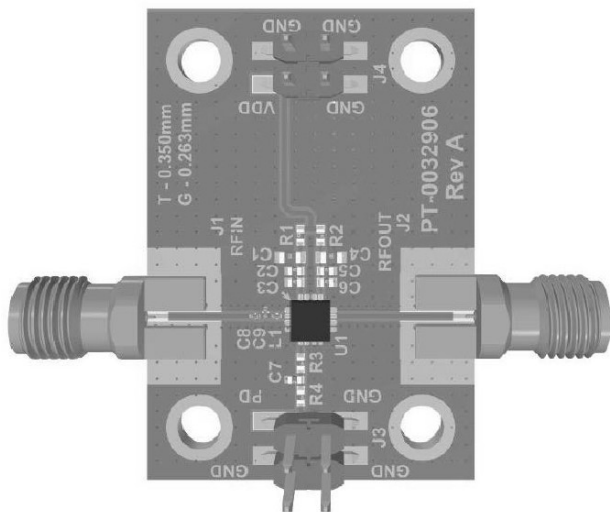
Parameter	Unit
Input Average Power	20 dBm
DC Supply VDD	-0.5 V to 5.5 V
Logic Control Voltage	-0.5 V to 2.75 V
Junction Temperature ^{7,8}	+150°C
Storage Temperature	-55°C to +150°C

4. T_C is defined by exposed paddle temperature.
5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with T_J ≤ +150°C (LNA ON Mode) will ensure MTTF >> 1 x 10⁶ hours.
8. Junction Temperature (T_J) = T_C + Θ_{Jc} * (V * I)
 Typical thermal resistance (Θ_{Jc}) = 33.4 °C/W.
 a) For T_C = +25°C,
 T_J = 41.7 °C @ 5 V, 100 mA
 b) For T_C = +115°C,
 T_J = 131.7 °C @ 5 V, 110 mA

Application Schematic



Sample Board Layout



Parts List

Schematic Component	Component Value
C1	10 μ F
C2	10 nF
C3	470 pF
C4-C6, R2	DNP
C7	5 pF
C8	27pF
R1, L1	0R
R3	100 Ω
R4	1 k Ω

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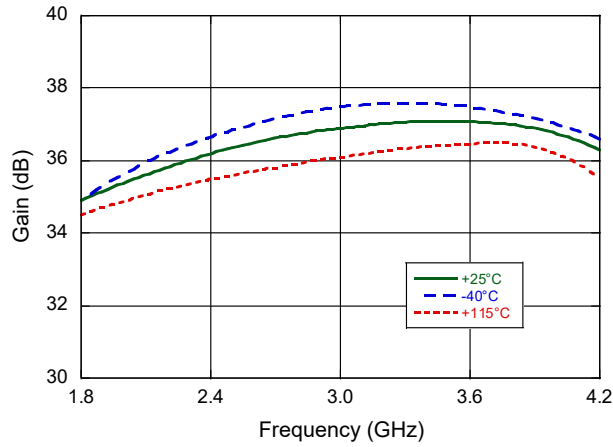


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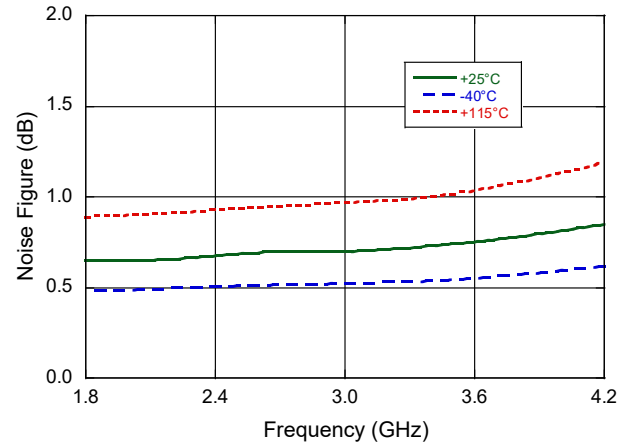
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Typical Performance Curves: $P_{IN} = -30 \text{ dBm}$, $V_{DD} = 5 \text{ V}$, $Z_0 = 50 \Omega$

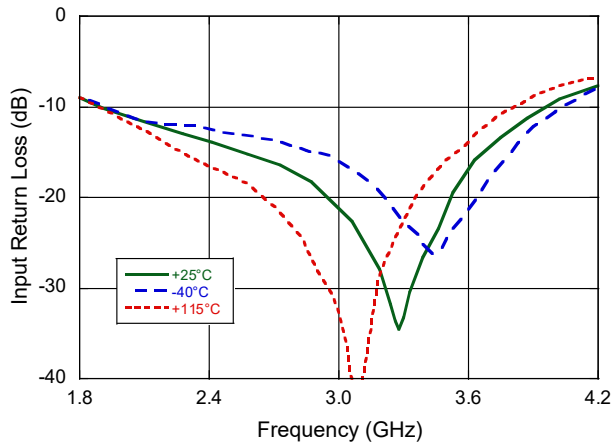
Gain⁹



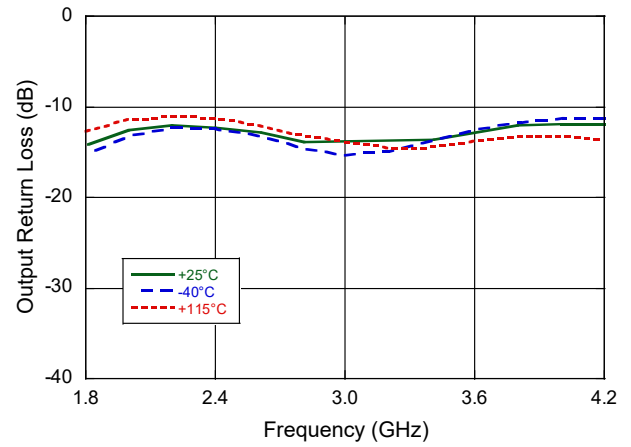
Noise Figure⁹



Input Return Loss

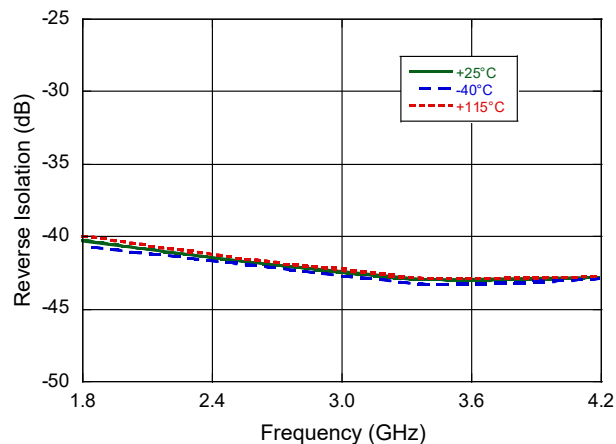


Output Return Loss

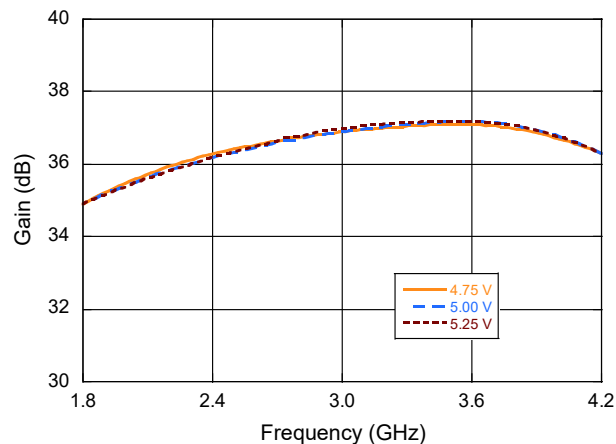


Typical Performance Curves: $P_{IN} = -30$ dBm, $V_{DD} = 5$ V, $Z_0 = 50 \Omega$

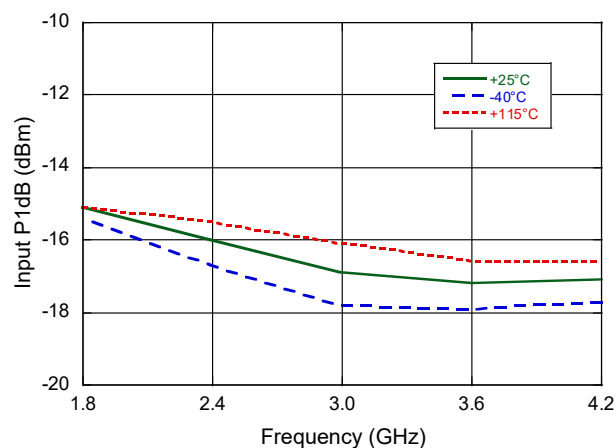
Reverse Isolation⁹



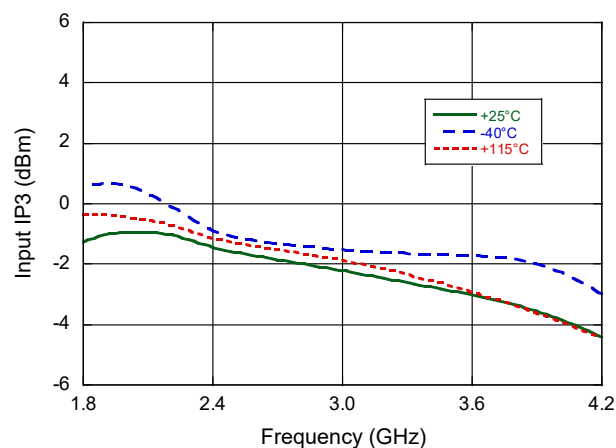
Gain⁹ over Supply



Input P1dB⁹



Input IP3⁹



9. For gain, noise figure, reverse isolation, P1dB and IP3 plots, RF trace and connector losses are de-embedded.

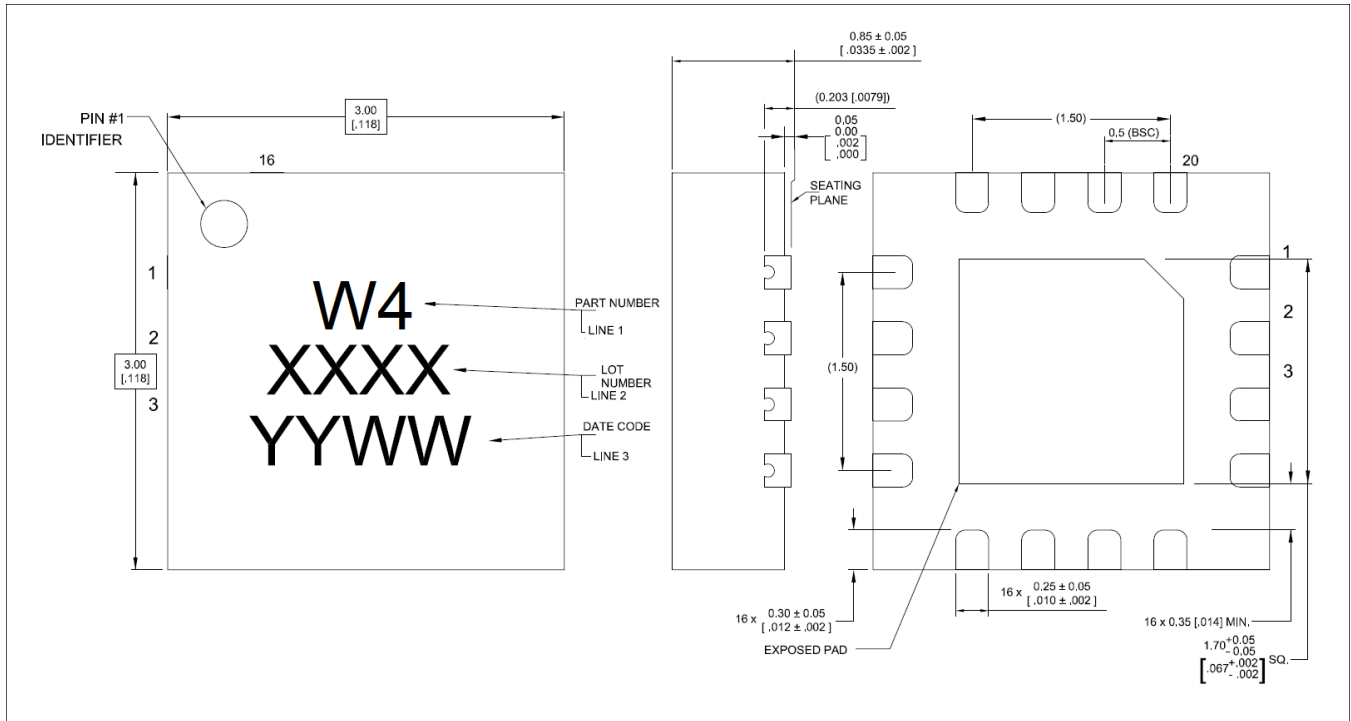
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Lead-Free 3 mm 16-Lead QFN[†]



[†] Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements in accordance to JEDEC J-STD-020D.
Plating is NiPdAu over Copper

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