Low Noise Amplifier
20 - 60 GHz

MAAL-011186-DIE
Rev. V1

Features

- Wideband Performance
- Low Noise Figure: 2.5 dB
- Gain: 22 dB
- P1dB: 14 dBm
- Bias Voltage: V_{DD} = 3.5 V
- Bias Current: I_{DSQ} = 130 mA
- 50 Ω Matched Input and Output
- Positive Voltage Only
- Die size: 2.525 x 1.345 x 0.1 mm
- RoHS* Compliant

Applications

- Test and Measurement
- EW
- ECM
- Radar

Description

The MAAL-011186-DIE is an easy to use wideband low noise amplifier. It operates from 20 - 60 GHz and provides 2.5 dB noise figure, 22 dB gain and 14 dBm P1dB. The input and output are fully matched to 50 Ω with typical return loss of better than –12 dB.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

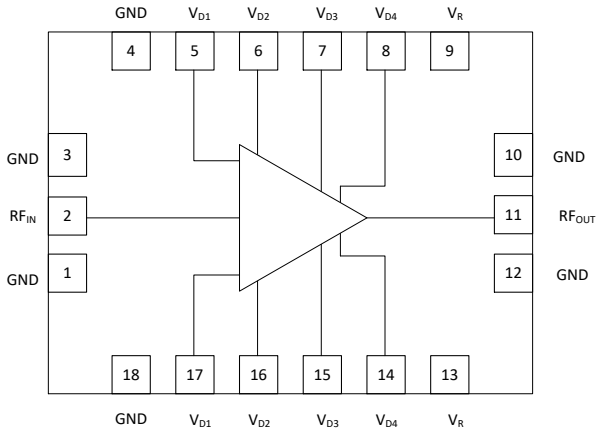
The MAAL-011186-DIE can be used as a low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Test and Measurement, 5G communications, EW, ECM, and Radar applications.

Ordering Information[1]

Part Number	Package
MAAL-011186-DIE	Gel Pack[1]

1. Die quantity varies

Functional Schematic



Pin Configuration[2]

Pin #	Function	Description
1,3,10,12	RF GND	RF ground
2	RF_{IN}	RF Input
4,18	DC GND	DC Ground
5,17	V_{D1}	Drain Bias 1
6,16	V_{D2}	Drain Bias 2
7, 15	V_{D3}	Drain Bias 3
8,14	V_{D4}	Drain Bias 4
9,13	V_R	Current Mirror Reference Voltage
11	RF_{OUT}	RF Output
		Backside of die[2]

2. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 20 - 60 GHz, T_A = +25°C, V_{CC} = 3.5 V, I_{DQ} = 130 mA, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	20 GHz 40 GHz 50 GHz	dB	22.0 17.5 17.0	24.0 19.0 19.0	—
Small Signal Gain Variation over Temperature	—	dB/°C	—	0.06	—
Gain Flatness	—	dB	—	±5	—
Noise Figure	20 GHz 25 - 40 GHz 40 - 50 GHz	dB	—	3.5 2.5 4.0	5.5 — —
Input Return Loss	—	dB	—	10	—
Output Return Loss	—	dB	—	10	—
Output Power 1dB Compression	—	dBm	—	14	—
Saturated Output Power (P_{SAT})	—	dBm	—	17	—
Output 3rd Order Intercept	—	dBm	—	24	—

Operational Maximum Ratings

Parameter	Absolute Maximum
Pin	+2 dBm
V_{DD}	4.0 V
Junction Temperature[4,5]	+150°C
Operating Temperature	-40°C to +85°C

4. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 22 °C/W.
   a) For T_C = +25°C,
   T_J = 36.4 °C @ 4 V, 130 mA
   b) For T_C = +85°C,
   T_J = 96.4 °C @ 4 V, 130 mA

Recommended Operating Conditions

It is recommended to operate at a typical drain voltage of +3.5 V ± 5 %. The maximum recommended operating drain current (set by the voltage on V_R) is fundamentally defined by the combination of the maximum operating junction temperature and the power dissipated. This can be calculated as shown in note 5.

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Pin	+5 dBm
V_{DD}	4.5 V
Junction Temperature	+175°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

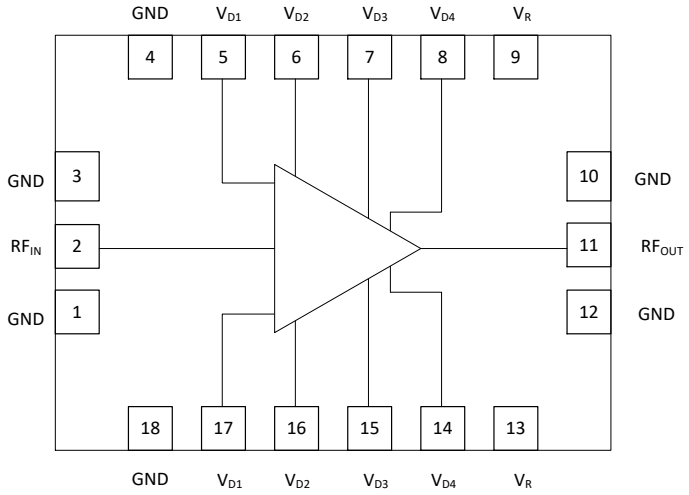
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

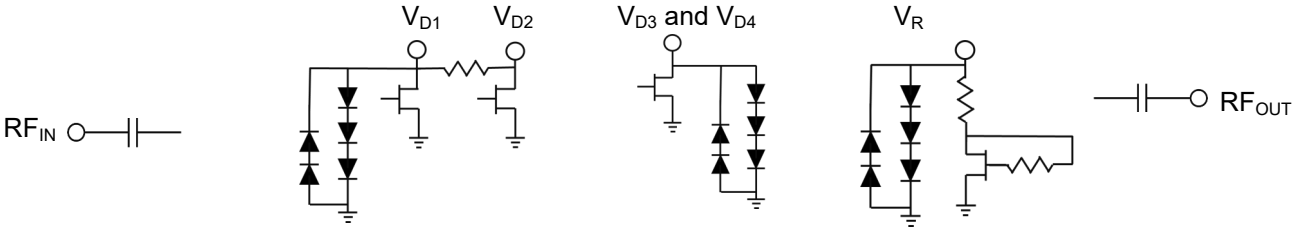
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Pin Configuration and Functional Descriptions

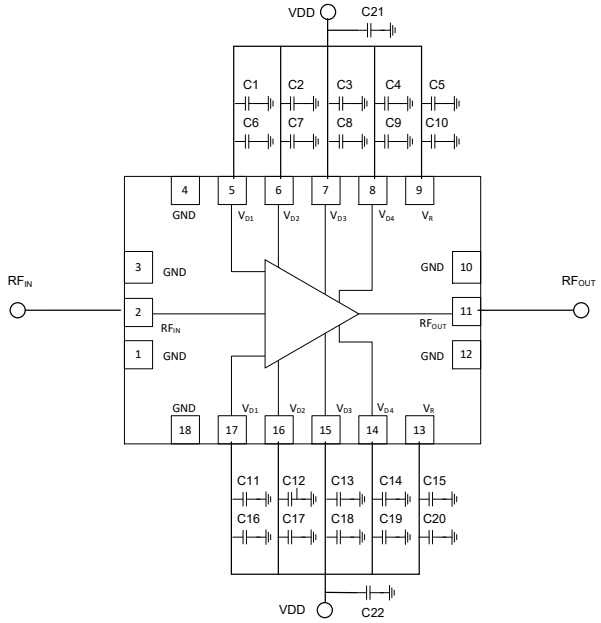


Pin #	Pin Name	Description
1,3,10,12	RF GND	These pads are grounded on the MMIC. They are intended to support both on-wafer G-S-G probing for production test and also the use of RF GND bonds if required in the application.
2	RF_{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
4, 18	DC GND	These pads are grounded on the MMIC. They are intended to support on-wafer G-S-G probing for production test and do not require connection in the application.
5, 17	V_{D1}	Drain biases for stage 1 of the amplifier. External bypass capacitors and de-Q resistors are required as described in the applications schematic. There is no internal connection between these pads and so pads 5 and 17 both need to be used.
6, 16	V_{D2}	Drain biases for stage 2 of the amplifier. External bypass capacitors and de-Q resistors are required as described in the applications schematic. There is no internal connection between these pads and so pads 6 and 16 both need to be used.
7, 15	V_{D3}	Drain biases for stage 3 of the amplifier. External bypass capacitors and de-Q resistors are required as described in the applications schematic. There is no internal connection between these pads and so pads 7 and 15 both need to be used.
8, 14	V_{D4}	Drain biases for stage 4 of the amplifier. External bypass capacitors and de-Q resistors are required as described in the applications schematic. There is no internal connection between these pads and so pads 8 and 14 both need to be used.
9, 13	V_R	Reference voltage for the amplifier. This is used to set the drain current of the device. A voltage can be applied using series resistor to V_D, or can be applied using an active bias circuit for more precise control of the drain current There is no internal connection between these pads and so pads 9 and 13 both need to be used. See applications section for the correct usage of this pin.
11	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled.

Interface Schematics



Application Schematic



Parts List

Part	Value	Case Style
C6 - C15	100 pF	Chip capacitor Murata 100pF BV150
C1 - C5, C16 - C20	0.1 µF	0402
C21,22	1µF	0402

Operating the MAAL-011186-DIE

Turn-on

1. Increase V_{D1}, V_{D2}, V_{D3}, V_{D4} to 3.5 V.
2. Set I_{DQ} by adjusting V_R or selecting a suitable resistor size. For a drain voltage of 3.5 V, a voltage of 1.4 V on the V_R pins will result in a drain current of 130 mA. This corresponds to a 650 Ω resistor between the drain supply on each V_R pin.
3. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_{D1}, V_{D2}, V_{D3}, V_{D4} to 0 V.

Application Circuit and Operation

The basic application circuit is shown below. Place C6 - C15 chip capacitors as close to the package as physically possible. The position of the C1 - C5 and C16 - C20 capacitors are not as critical but should also be placed as closely as practically possible. C21 and C22 should be on the same PCB as C1-5 and C16-20. All drain connections can be connected together so long as the recommended capacitors are placed as advised.

To set the drain current, a reference voltage (V_R) is applied to pins 9 and 13. If single positive supply operation is desired, a resistor can be connected in series between the drain supply and pin 9, and pin 13. A resistor value of 650 Ω between a drain supply of 3.5 V and each V_R pin, will result in a typical I_{DQ} of 130 mA. Alternatively, V_R can be supplied by a second voltage source, adjusted to achieve the desired drain current.

If using a fixed voltage on V_R to set the drain current it should be expected that there will be an amount of drain current variation over temperature and also between individual devices and manufacturing lots. If more precise control over the drain current is required, a simple, low cost active bias circuit can be used.

A suitable active bias circuit for use with the MAAL-011186-DIE is detailed in MACOM applications note AN-0004357 which gives a full schematic, BOM, theory of operation and design guide. Here V_R should be considered to be the gate of the device as described in AN-0004357.

For all approaches to setting I_{DQ}, each V_R pin will sink between approximately 3 mA to 5 mA depending on the voltage applied: this should be accounted for when designing the circuit interfacing with the V_R pins.

Wire Bonding

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect.

Alternatively, a 3 mil bond ribbon could be used.

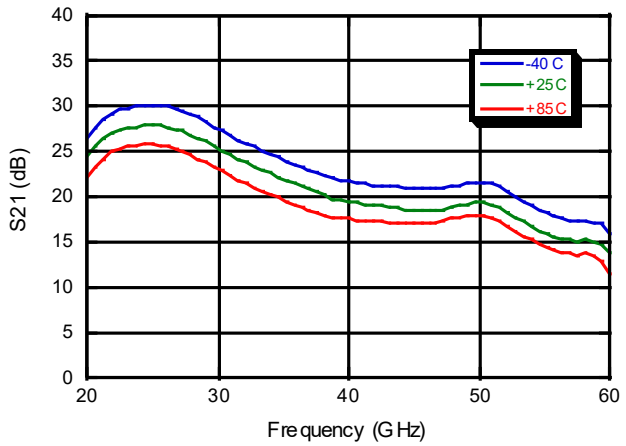
Die Attach

For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used.

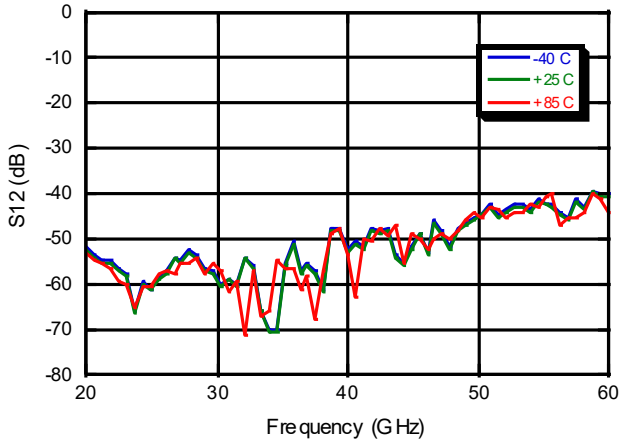
If using eutectic, an 80% Au / 20% Sn preform is recommended.

Typical Performance Curves @ V_D = 3.5 V, I_D = 130 mA, Z_0 = 50 Ω

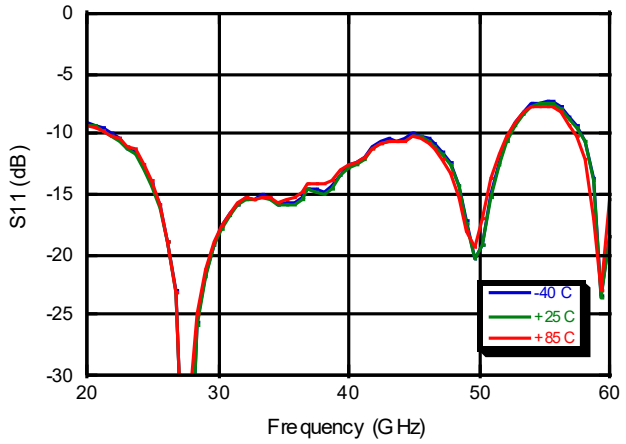
Gain



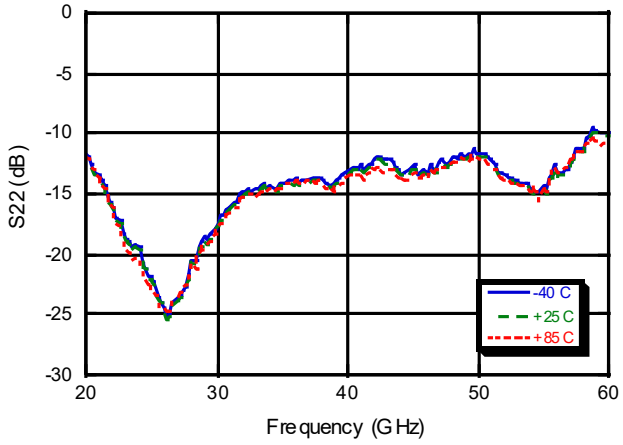
Reverse Isolation



Input Return Loss

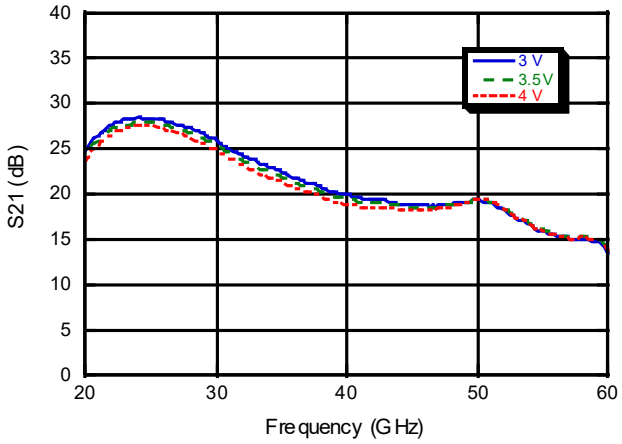


Output Return Loss

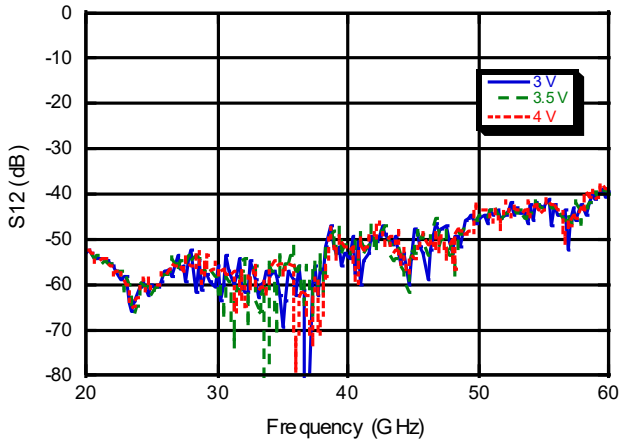


Typical Performance Curves @ I_D = 130 mA, T_A = 25°C, Z_0 = 50 Ω

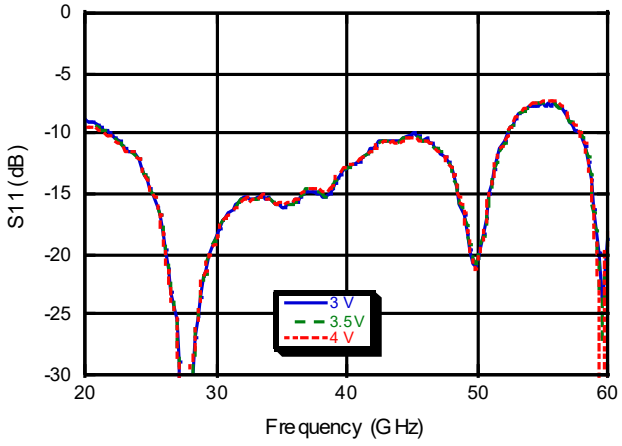
Gain



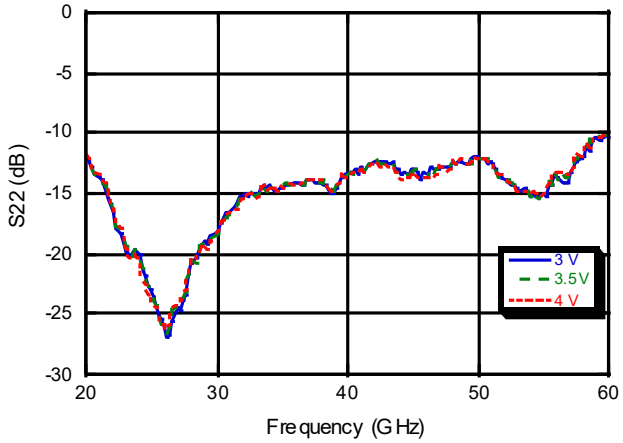
Reverse Isolation



Input Return Loss

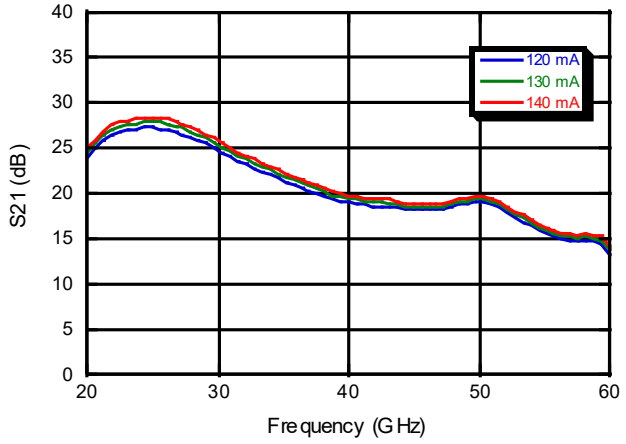


Output Return Loss

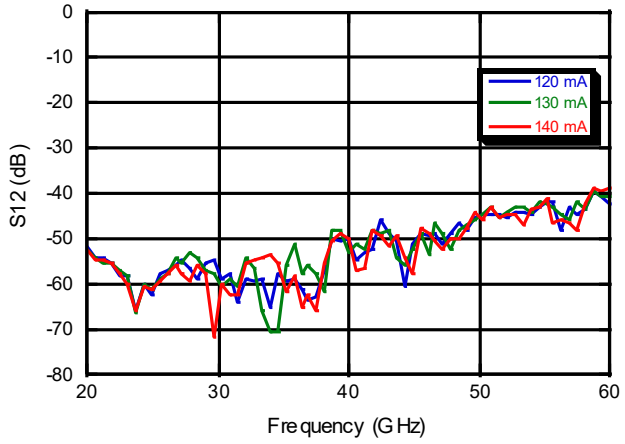


Typical Performance Curves @ V_D = 3.5 V, T_A = 25°C, Z_0 = 50 Ω

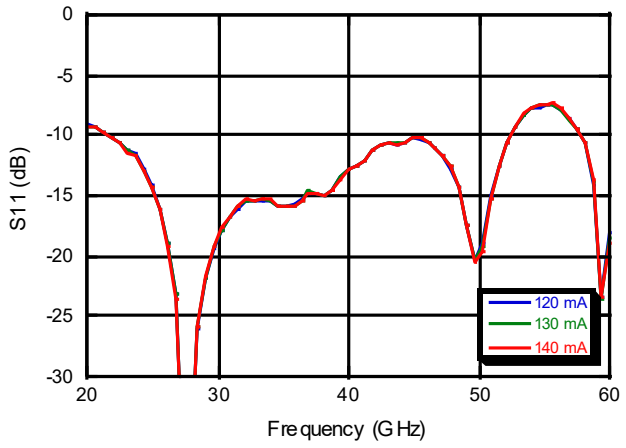
Gain



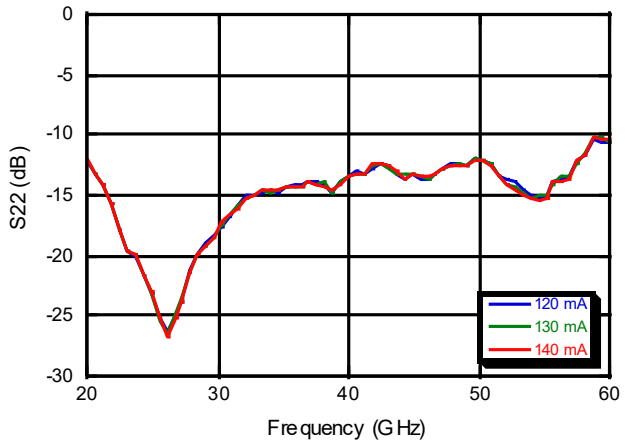
Reverse Isolation



Input Return Loss

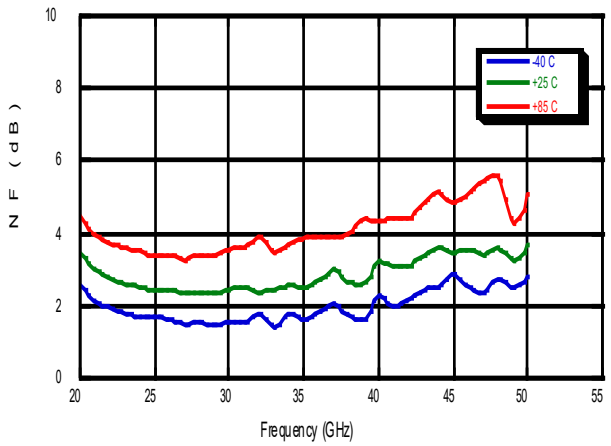


Output Return Loss

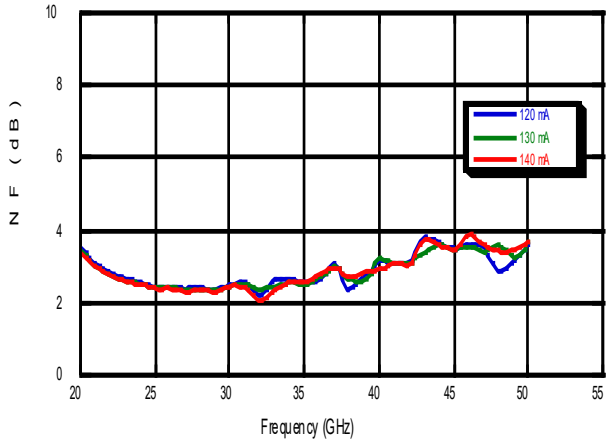


Typical Performance Curves @ V_D = 3.5 V, I_D = 130 mA, T_{AMB} = 25°C, Z_0 = 50 Ω

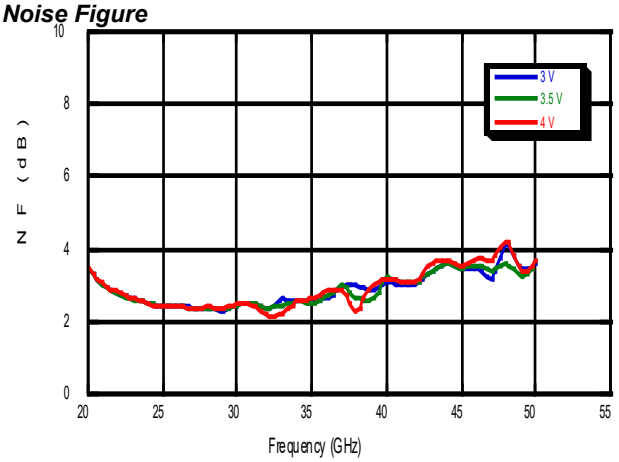
Noise Figure



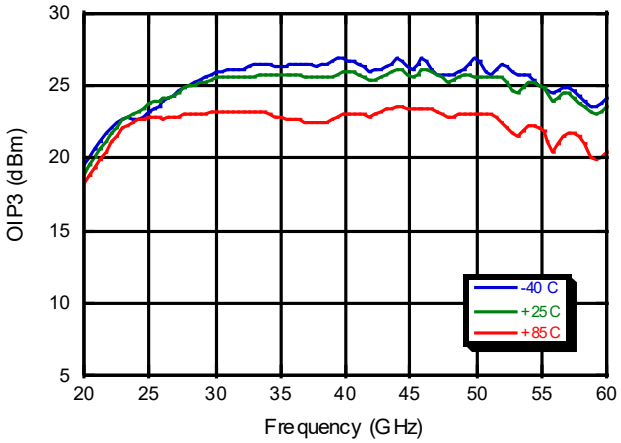
Noise Figure



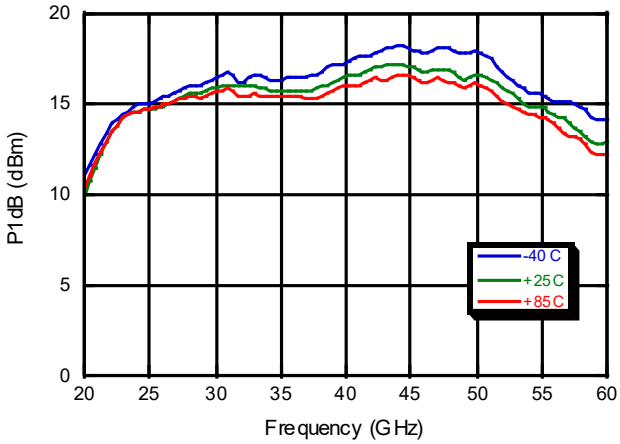
Noise Figure



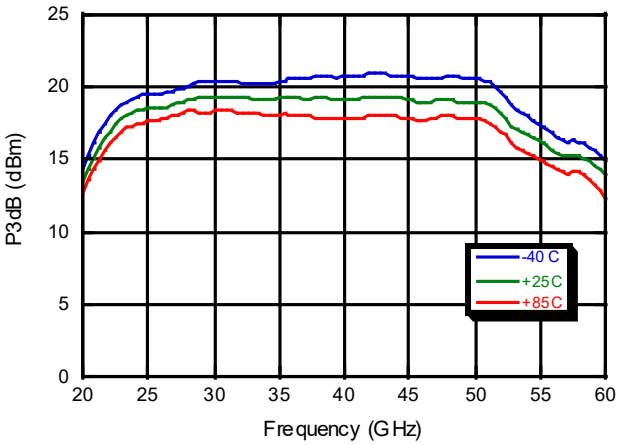
OIP3



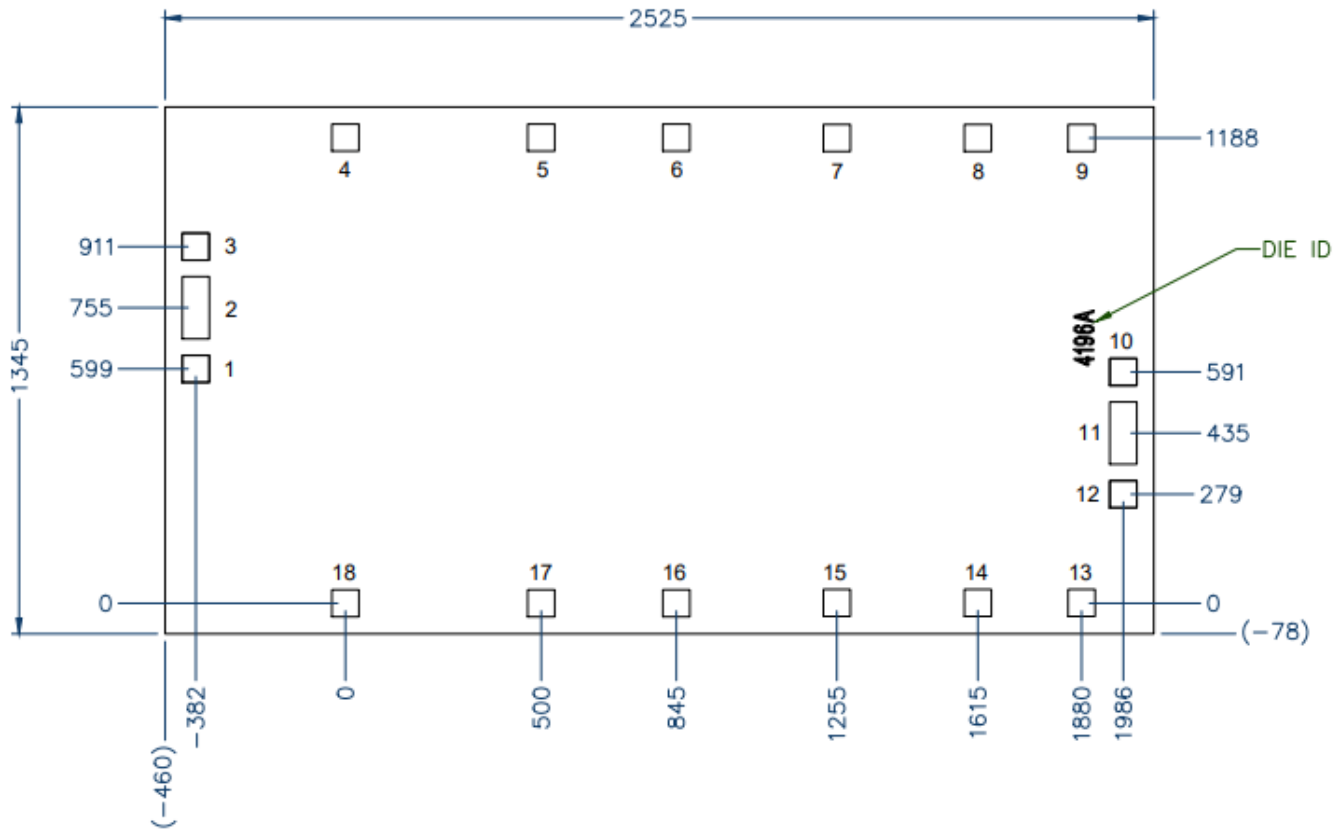
P1dB



P3dB



MMIC Die Outline[9,10,11,12]



Bond Pad Detail (µm)

Pad	Size (x)	Size (y)
Single	69	69
Double	69	159

9. All units in mm, unless otherwise noted, with a tolerance of ±5 µm
10. Die thickness is 100 µm with a tolerance of ±5 µm
11. Bond pad / backside metallization: gold
12. Die size reflects final dimensions