Digital Attenuator, 0.5 dB LSB, 6-Bit, Consistent Phase 31.5 dB, DC - 26.5 GHz

MAAD-011061
Rev. V1

Features

- 6-Bit, 0.5 dB LSB, 31.5 dB range
- Consistent Phase over All Attenuation States
- Integrated CMOS/TTL Compatible Driver
- Compatible with 1.8 V, 2.5 V, 3.3 V, 5 V CMOS and 5 V TTL logic input
- Parallel or Serial (P/S) Control
- Low DC Power Consumption
- Attenuation Accuracy:
  +/-(0.2 + 2% of attenuation setting) dB
- Lead-Free 3 mm 20-Lead Package
- RoHS* Compliant

Applications

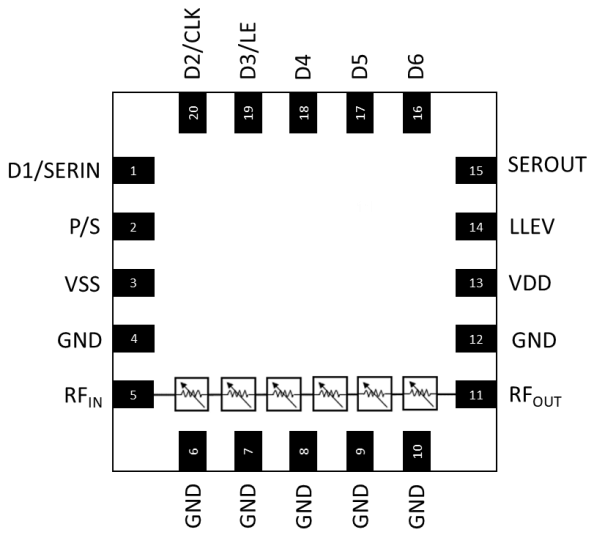
- Multi Market-MMIC
- Metro Long Haul

Description

The MAAD-011061 is a wide band 6-bit, 0.5 dB step MMIC digital attenuator in a lead-free 3 mm, 20-lead surface mount plastic package. The phase is consistent across all attenuation states. This device is ideally suited for use where high accuracy, very low power consumption, and low intermodulation products are required.

This attenuator is controlled with either a SPI compatible serial interface or a 6-bit parallel word. SEROUT is the SERIN delayed by 6 clock cycles which can be used in daisy-chain operation.

Functional Schematic



Pin Configuration[3]

Pin #	Pin Name	Function
1	D1 or SERIN	0.5 dB Bit or Serial In
2	P/S	Parallel/Serial Selection
3	VSS	Negative Supply
4, 6-10,12	GND	Ground
5	RF_{IN}	RF Input
11	RF_{OUT}	RF Output
13	VDD	Positive Supply
14	LLEV	Logic Level
15	SEROUT	Serial Output
16	D6	16 dB Bit Control
17	D5	8 dB Bit Control
18	D4	4 dB Bit Control
19	D3 or LE	2 dB Bit or LE
20	D2 or CLK	1 dB Bit or Clock

3. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground. MACOM recommends connecting all GND and NC pins to ground.

Ordering Information[1,2]

Part Number	Package
MAAD-011061-TR0500	500 Piece Reel
MAAD-011061-SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

1 * Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = DC - 26.5 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{DD} = +5 V, V_{SS} = -5 V[4], P_{IN} = 0 dBm

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Insertion Loss	DC - 10.0 GHz 10.0 - 18.0 GHz 18.0 - 26.5 GHz	dB	—	2.7 3.5 5.4	3.7 4.9 6.7
RMS Attenuation Error	DC - 26.5 GHz	dB	—	0.25	—
Attenuation Accuracy	Relative to Insertion Loss	± (0.2 + 2% of attenuation setting) dB typ.			
Relative Phase, 0.5 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -2 -2	-1 to +1 -1 to +1 -1 to +1	2 2 2
Relative Phase, 1 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -2 -2	-1 to +1 -1 to +1 -1 to +1	2 2 2
Relative Phase, 2 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -2 -2	-1 to +1 -1 to +1 -1 to +1	2 2 2
Relative Phase, 4 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -2 -2	-1 to +2 -1 to +3 -1 to +3	3 4 4
Relative Phase, 8 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -3 -5	-1 to +1 -2 to +2 -4 to +2	2 3 3
Relative Phase, 16 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-3 -3 -4.5	-2 to +2 -2 to +2 -3 to +1	3 3 2
Relative Phase, 31.5 dB Attenuation (Reference to Insertion Loss State)	10.0 GHz 18.0 GHz 26.5 GHz	deg	-2 -8 -13	-1 to +3 -5 to +3 -8 to +3	5 4 4
Return Loss	All states	dB	—	-15	—
Input P0.1dB	Reference State @ 10 GHz	dBm	—	27	—
IIP_3	2-Tone, +7 dBm/tone, 1 MHz Spacing (Reference State) @ 10 GHz	dBm	—	49	—
T_{RISE}, T_{FALL}	10% to 90% RF, 90% to 10% RF	ns	—	20	—
T_{ON}, T_{OFF}	50% triggered control to 90%, 10% of RF	ns	—	50	—

4. Apply VDD and VSS before RF signal. No sequence requirement for VDD & VSS.

Electrical Specifications (continued):
Freq. = DC - 26.5 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{DD} = +5 V, V_{SS} = -5 V[4], P_{IN} = 0 dBm

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Logic Input High V_{IH}	LLEV (pin 14) Grounded LLEV (pin 14) Open	V	1.17 3.5	—	5.0 5.0
Logic Input Low V_{IL}	LLEV (pin 14) Grounded LLEV (pin 14) Open	V	0.0 0.0	—	0.8 1.5
Control Logic Current	LLEV (pin 14) Grounded LLEV (Pin 14) Open	µA	— —	50 60	— —
Overshoot	All state changes	dB	—	2.8	—
Undershoot	All state changes	dB	—	-10	—
V_{DD}	—	V	+4.75	+5.0	+5.25
I_{DD} Quiescent Current	—	mA	—	1.5	—
V_{SS}	—	V	-5.25	-5.0	-4.75
I_{SS} Quiescent Current	—	mA	—	1	—
Output High Voltage V_{OH} of SEROUT	I_{OH} = -100 µA	V	—	1.8	—
Output Low Voltage V_{OL} of SEROUT	I_{OH} = -100 µA	V	0	—	0.2

4. Apply VDD and VSS before RF signal. No sequence requirement for VDD & VSS.

Absolute Maximum Ratings

Parameter	Absolute Maximum
Input Power 1 - 26.5 GHz	27 dBm
V_{DD} Voltage	+5.5 V
V_{SS} Voltage	-5.5 V
Control Voltage	-0.5 V $\leq V_C \leq$ 5.5 V
SEROUT Current	200 µA
Junction Temperature	+135°C
Operating Temperature	-40°C to +105°C
Storage Temperature	-65°C to +135°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.

Recommended Operating Conditions

Parameter	Maximum
Input Power	26 dBm
Junction Temperature	+125°C
Case Temperature	-40°C to +105°C

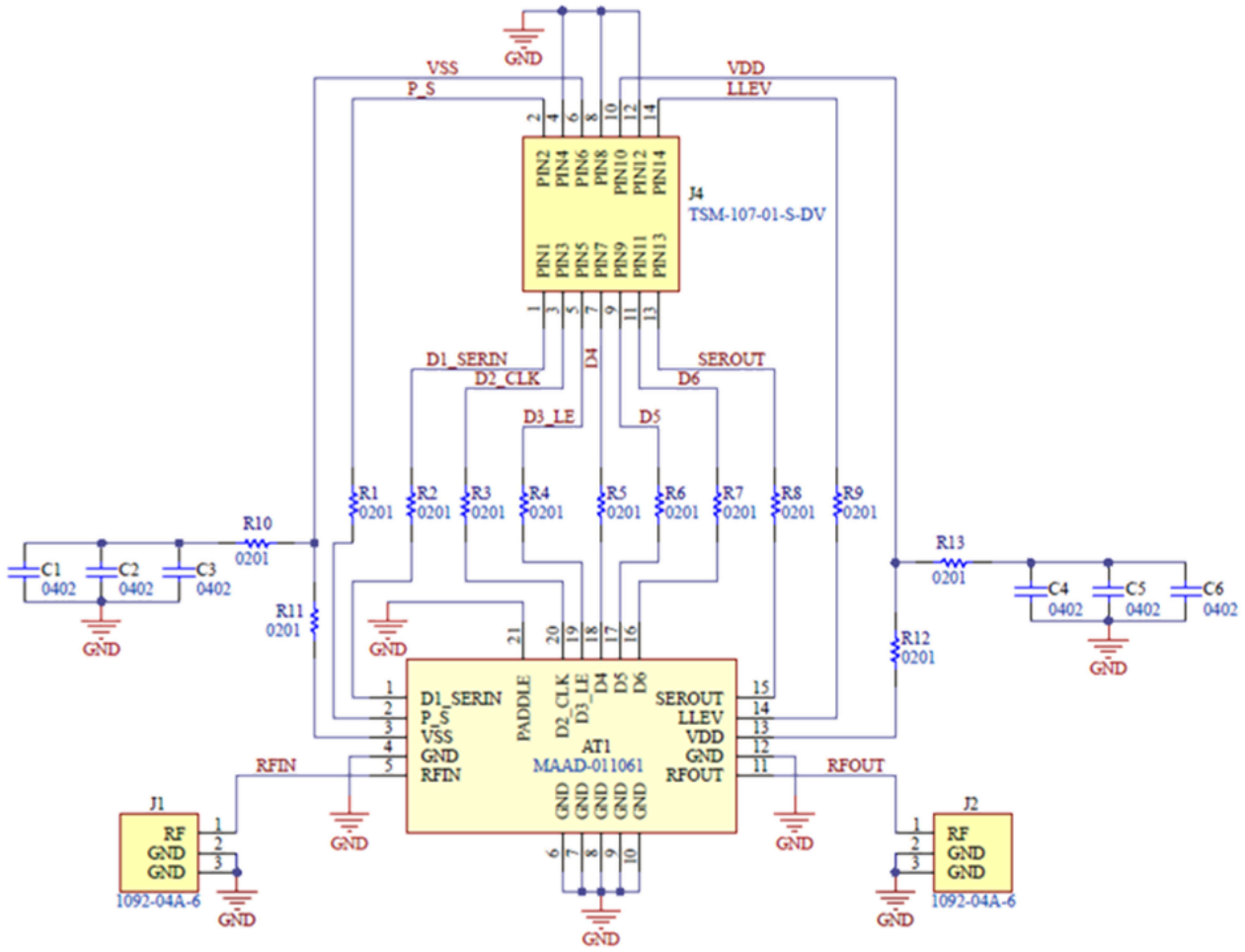
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

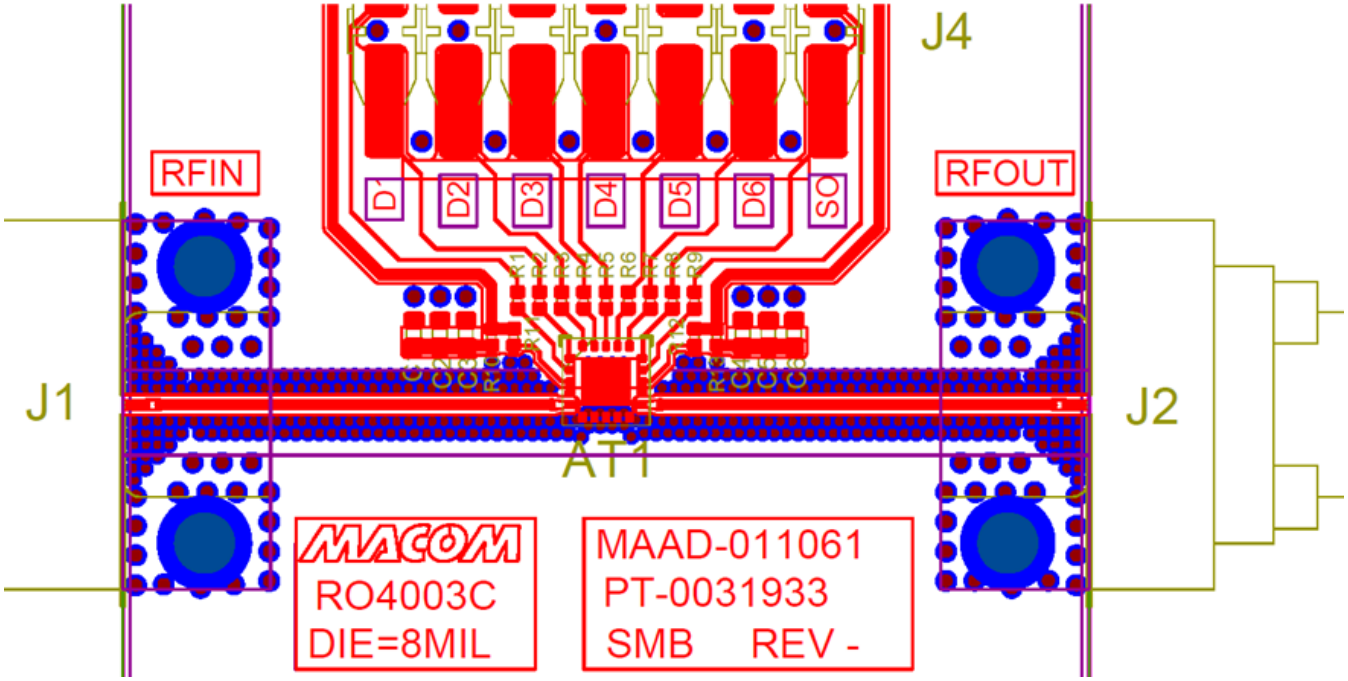
Application Schematic



Parts List

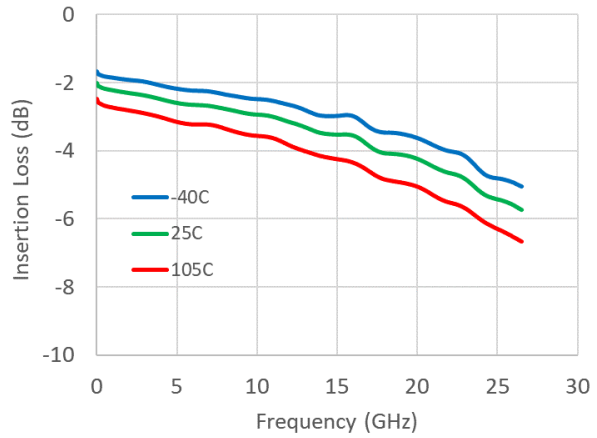
Part	Value	Case Style
AT1	MAAD-011061	3mm, 20 Lead
C1, C4	Capacitor, 10 pF, 50 V	0402
C2,C5	Capacitor, 1000 pF, 25 V	0402
C3, C6	Capacitor, 1 µF, 10 V	0402
R1 - R13	Resistor, 0 Ω	0201
J1 - J2	Southwest 1492-03A-5	End Launch 2.4 mm Female
J4	DC Connector	TSM-107-01-S-DV

Evaluation Board layout

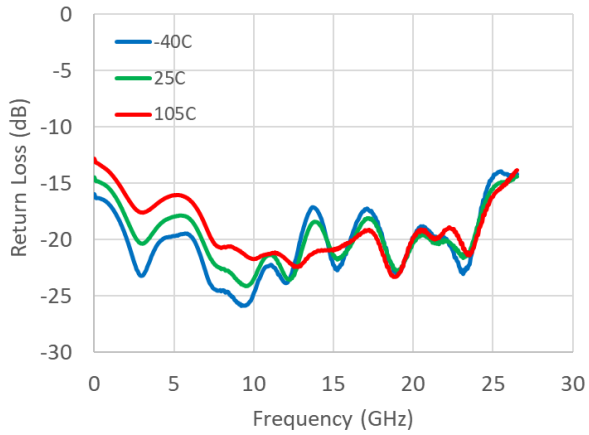


Typical Performance Curves

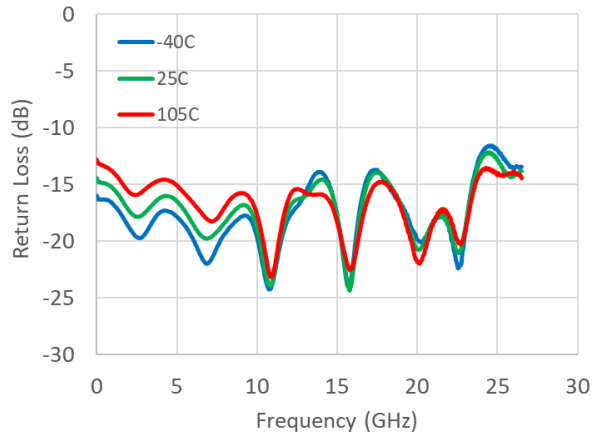
Insertion Loss



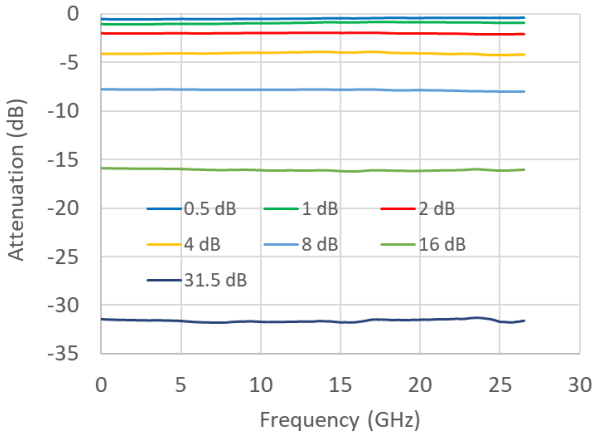
Input Return Loss - Reference State



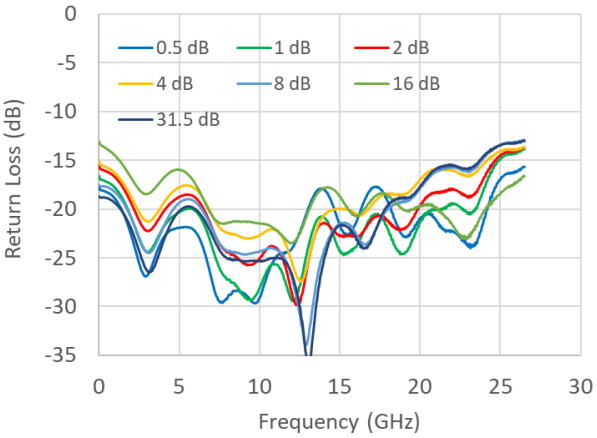
Output Return Loss - Reference State



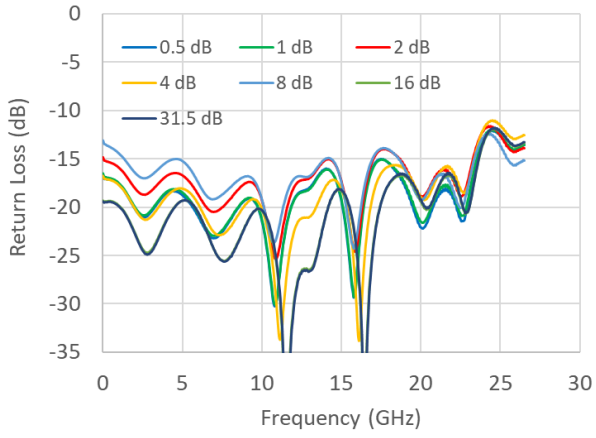
Attenuation - Major Bits



Input Return Loss - Major Bits

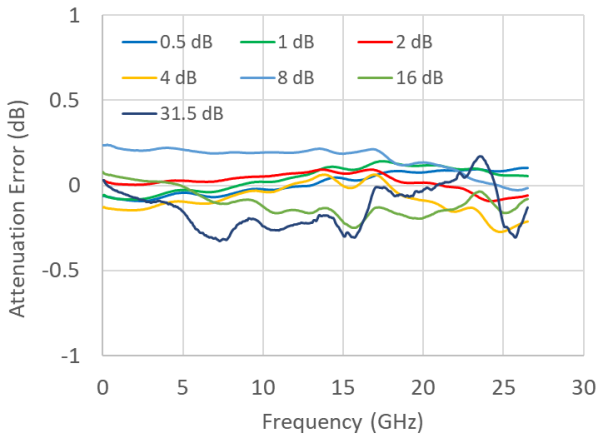


Output Return Loss - Major Bits

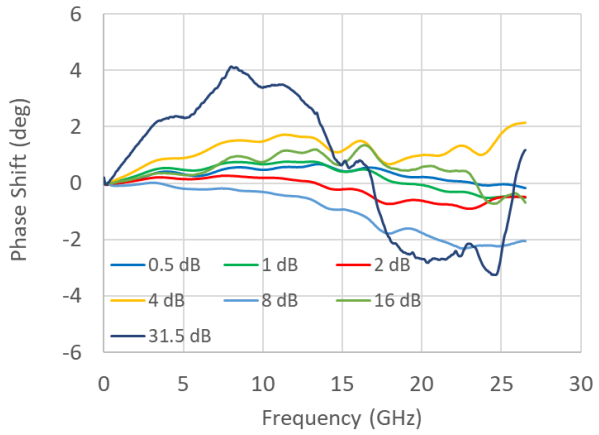


Typical Performance Curves

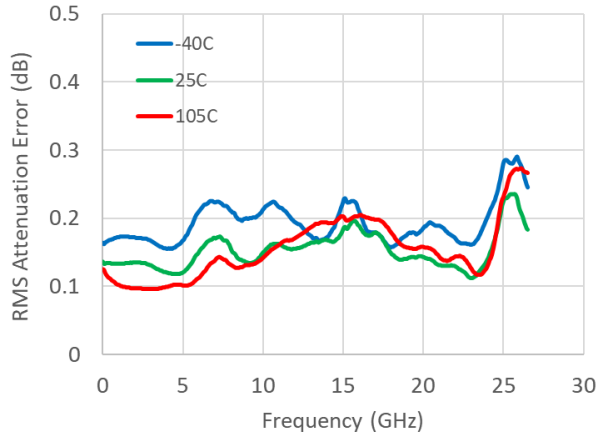
Attenuation Error - Major Bits



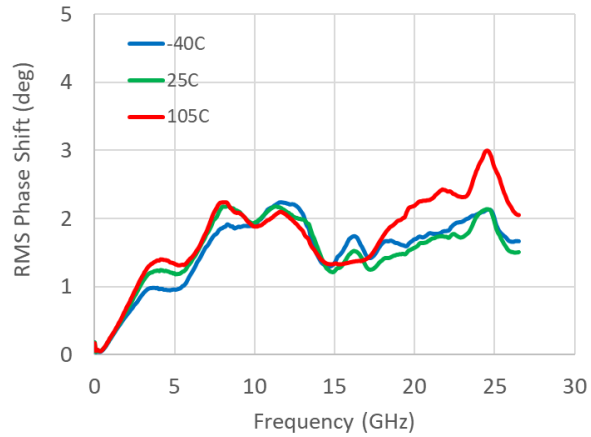
Phase Shift - Major Bits



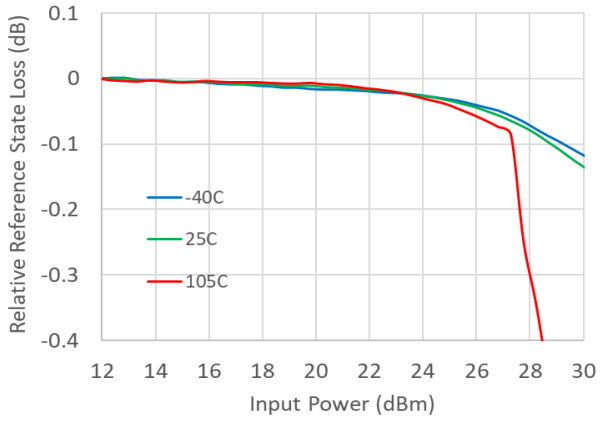
RMS Attenuation Error



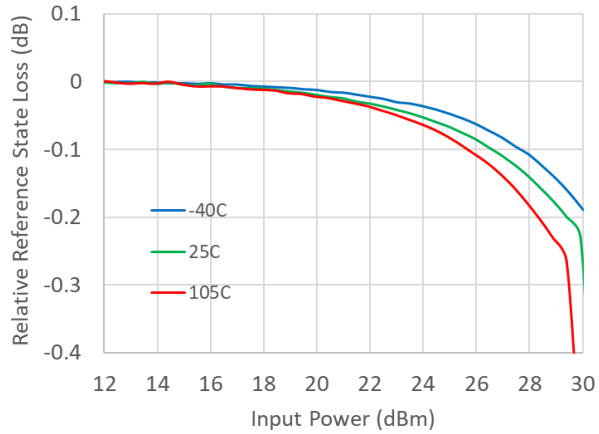
RMS Phase Shift



Ref. State Insertion Loss Compression - 1 GHz

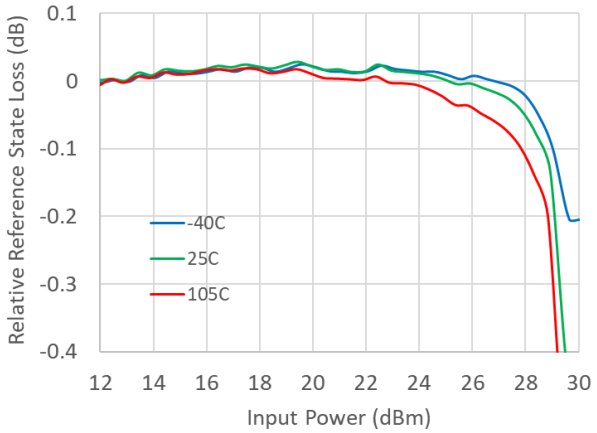


Ref. State Insertion Loss Compression - 10 GHz

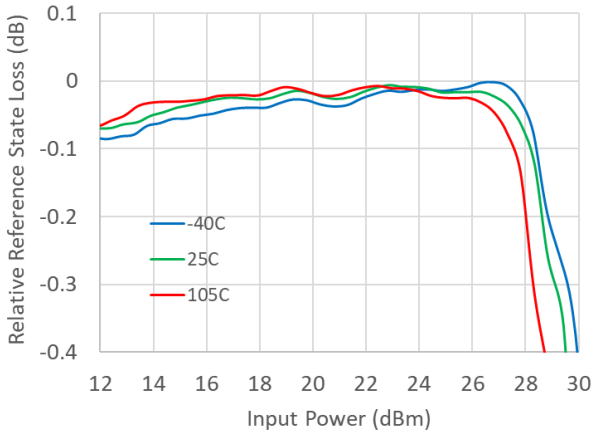


Typical Performance Curves

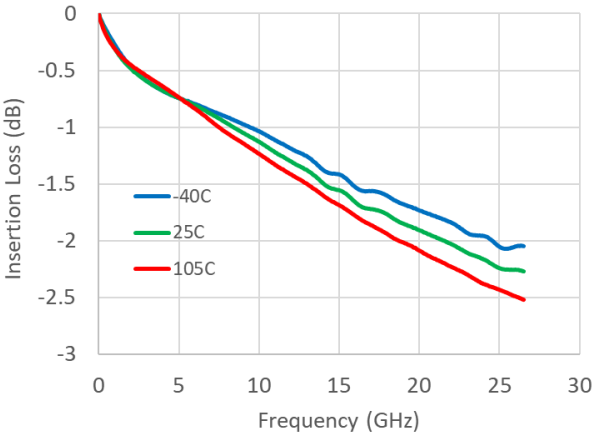
Ref. State Insertion Loss Compression - 18 GHz



Ref. State Insertion Loss Compression - 26.5 GHz



Evaluation Board Thru Line Insertion Loss



Modes of Operation: Serial and Direct Parallel

Bias Sequencing for both Modes

To avoid potential problems with application of RF signal, VDD and VSS should be supplied first. VDD and VSS can be applied in either order.

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, pins 19, 20, and 1 have the LE, CLK, and SERIN functions, respectively.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, Pins 19, 20, and 1 have the D3, D2, and D1 functions.

Mode Truth Table

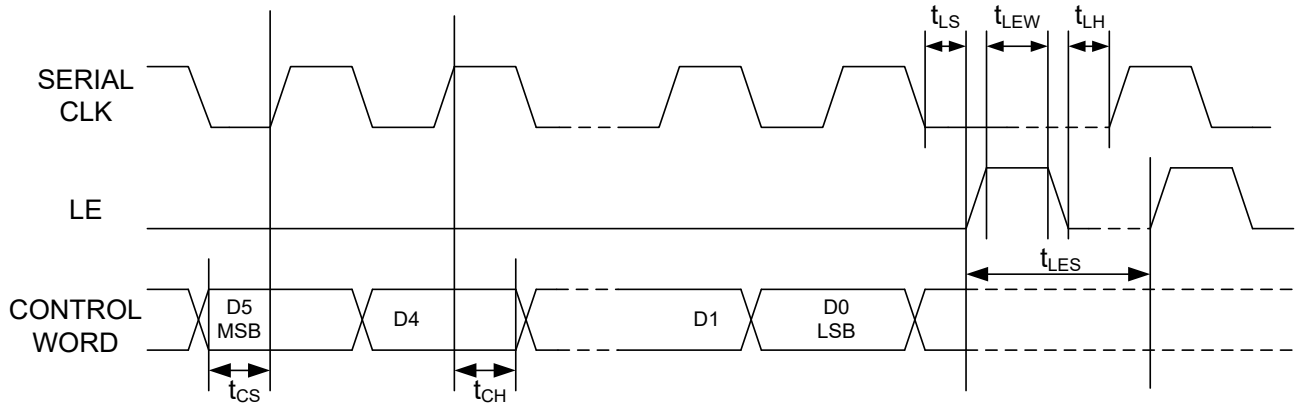
P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

Truth Table[6]

D6	D5	D4	D3	D2	D1	Attenuation (dB)
0	0	0	0	0	0	Reference IL
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

6. "0" = V_{IL}, "1" = V_{IH}.

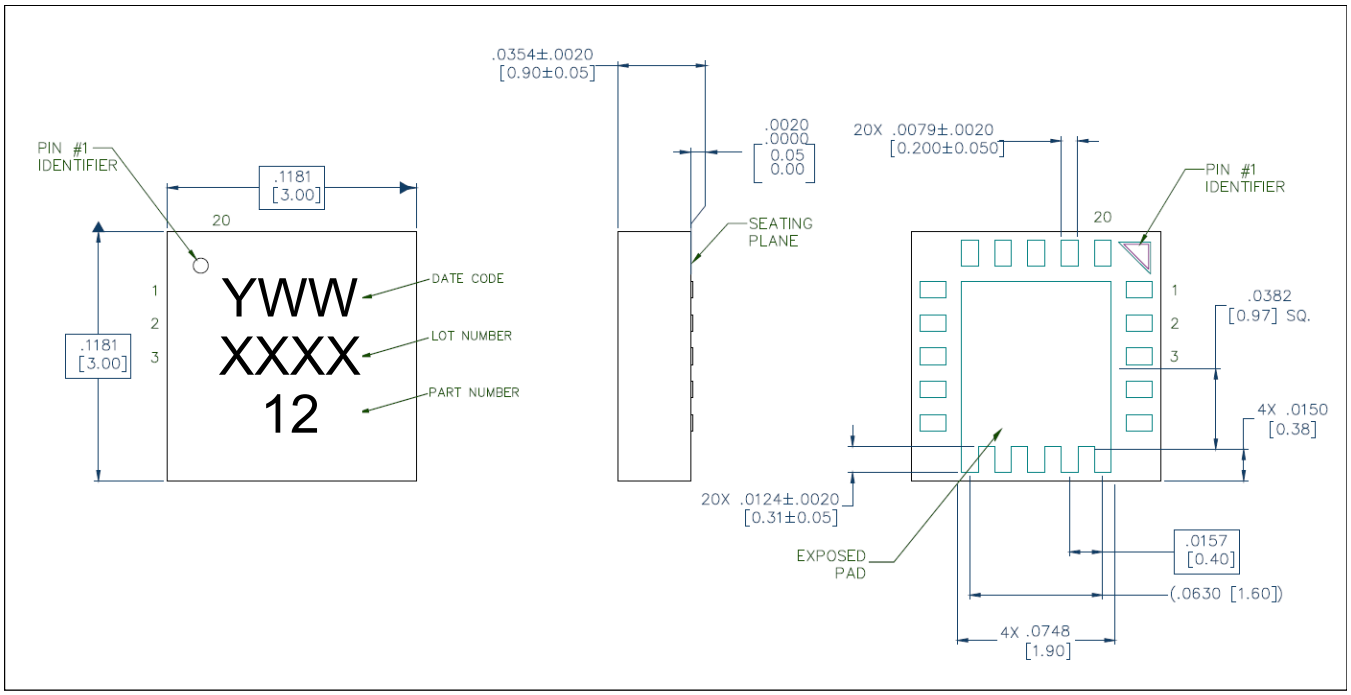
Functionality Modes of Operation: Serial and Direct Parallel
Serial Input Interface Timing Diagram



Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+105°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Lead-Free 3 mm, 20-Lead Laminate Package†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements in accordance to JEDEC J-STD-020D.
Plating is 100% NiPdAg over copper.