Digital Attenuator, 1 dB LSB, 5-Bit
31 dB, DC - 55 GHz

MAAD-011048
Rev. V3

Features

- 5-Bit, 1 dB LSB, 31 dB range
- Insertion Loss:
  - 2.0 dB @ 26.5 GHz
  - 3.1 dB @ 50 GHz
- P0.1 dB: 26 dBm @ 40 GHz
- Integrated CMOS Compatible Driver
- Compatible with 1.8 V CMOS logic
- Parallel or Serial (P/S) Control
- Low DC Power Consumption
- Lead-Free 3 mm 20-Lead Package
- RoHS* Compliant

Applications

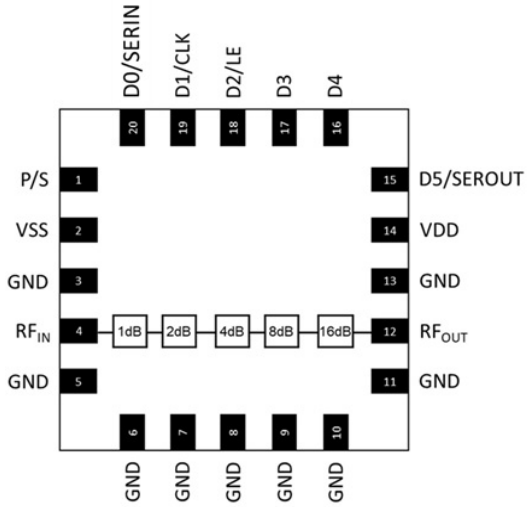
- ISM
- Multi Market

Description

The MAAD-011048 is a wide band 5-bit, 1 dB step MMIC digital attenuator in a lead-free 3 mm, 20 lead surface mount laminate package. This device is ideally suited for use where high accuracy, very low power consumption, and low intermodulation products are required.

This attenuator is controlled with either a SPI compatible serial interface or a 5 bit parallel word. SEROUT is the SERIN delayed by 6 clock cycles which can be used in daisy-chain operation.

Functional Schematic



Pin Configuration[3]

Pin #	Function
1	Parallel/Serial Selection
2	Negative Supply
3, 5 - 11, 13	Ground
4	RF Input
12	RF Output
14	Positive Supply
15	16 dB bit or Serial Output
16	8 dB Bit Control
17	4 dB Bit Control
18	2 dB Bit or LE
19	1 dB Bit or Clock
20	Serial Input
21[4]	Ground Pad

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information[1,2]

Part Number	Package
MAAD-011048-TR0500	500 piece reel
MAAD-011048-SB1	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
1	P/S	Selection of serial or parallel control mode
2	VSS	Negative supply Input
3, 5~11,13	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB
4	RF_{IN}	Attenuator Input. The RF_{IN} pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking
12	RF_{OUT}	Attenuator Output. The RF_{OUT} pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking
14	VDD	Positive supply Input
15	D5/ SEROUT	Parallel control input for 16 dB attenuation bit or serial input control delayed by 6 clock cycles
16	D4	Parallel control input for 8 dB attenuation bit
17	D3	Parallel control input for 4 dB attenuation bit
18	D2/LE	Parallel control input for 2 dB attenuation bit or latch enable input of serial control mode
19	D1/CLK	Parallel control input for 1 dB attenuation bit or clock input of serial control mode
20	SERIN	Control word input of serial control mode
21	Pad	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB

AC Electrical Specifications:
T_A = 25°C, VDD = +3.3 V, VSS= -3.3 V[5], P_{IN} = 0 dBm, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Insertion Loss	DC - 18.0 GHz 18.0 - 26.5 GHz 26.5 - 40.0 GHz 40.0 - 50.0 GHz 50.0 - 55.0 GHz	dB	—	1.5 2.0 2.4 3.1 3.1	2.6 3.2 3.8 4.7 —
RMS Attenuation Error	DC - 18.0 GHz 18.0 - 26.5 GHz 26.5 - 40.0 GHz 40.0 - 55.0 GHz	dB	—	0.4 0.7 0.9 0.7	—
Attenuation Accuracy	DC - 18.0 GHz 18.0 - 26.5 GHz 26.5 - 40.0 GHz 40.0 - 55.0 GHz	± (0.3 + 2% of attenuation setting) dB typ. ± (0.3 + 3% of attenuation setting) dB typ. ± (0.3 + 5% of attenuation setting) dB typ. ± (0.3 + 5% of attenuation setting) dB typ.			
Input Return Loss	All states	dB	—	-15	—
Output Return Loss	All states	dB	—	-12	—
Input P0.1dB	10 GHz @ Reference State	dBm	—	27	—
IIP_3 @ 10 GHz	2-Tone, +7 dBm/tone, 1 MHz Spacing (Reference State)	dBm	—	50	—
T_{RISE}, T_{FALL}	10% to 90% RF, 90% to 10% RF	ns	—	15	—
T_{ON}, T_{OFF}	50% triggered control to 90%, 10% of RF	ns	—	125	—
Overshoot	All state changes	dB	—	2.8	—
Undershoot	All state changes	dB	—	-10	—

5. Apply VDD and VSS before RF signal. No sequence requirement for VDD & SVSS.

DC Electrical Specifications: T_A = 25°C, VDD = +3.3 V, VSS = -3.3 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
I_{DD} Quiescent Current	—	mA	—	0.3	—
I_{ss} Quiescent Current	—	mA	—	0.6	—
Logic Input High V_{IH}	—	V	1.17	—	2
Logic Input Low V_{IL}	—	V	0	—	0.8
Logic Input Current	V_{IH}= 1.8 V	µA	—	—	10
SEROUT Output High V_{OH}	18 KΩ load	V	—	1.8	—
SEROUT Output Low V_{OL}	18 KΩ load	V	—	0	—

Recommended Operating Conditions

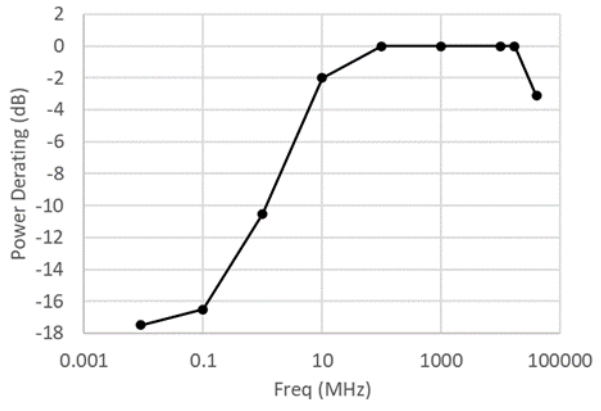
Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power, 100 MHz to 40 GHz (RF_{IN} and RF_{OUT})[6]	-	dBm	—	—	26
Positive Supply Voltage	VDD	V	+3.15	+3.3	+3.45
Negative Supply Voltage	VSS	V	-3.45	-3.3	-3.15
Operating Temperature[7]	T_c	°C	-40	25	105

Absolute Maximum Ratings[8,9]

Parameter	Symbol	Unit	Min.	Max.
Input Power	-	dBm	—	27
Positive Supply Voltage	VDD	V	-0.3	3.6
Negative Supply Voltage	VSS	V	-3.6	+0.3
Logic Input Voltage	V_I	V	-0.2	+2
Operating Temperature[7]	T_c	°C	-40	105
Storage Temperature	-	°C	-65	150

6. T_{PADDLE} = +105°C. See power derating curve for details.
7. Temperature of the exposed pad.
8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.

Power Derating Curve



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Parameter	Rating	Standard
Human Body Model (HBM)	Class 1B	ESDA/JEDEC JS-001
Charged Device Model (CDM)	Class C3	ESDA/JEDEC JS-002

Modes of Operation: Serial and Direct Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, pins 18, 19, & 20 have the LE, CLK, and SER IN functions, respectively.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, pins 18 & 19 have the D2 & D1 functions.

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

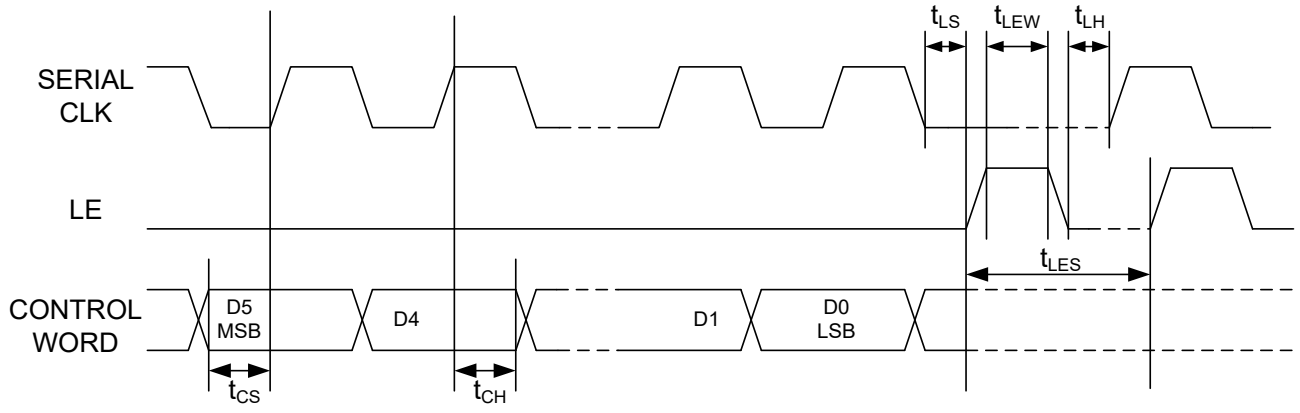
Truth Table[10]

D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	X	Reference IL
0	0	0	0	1	X	1
0	0	0	1	0	X	2
0	0	1	0	0	X	4
0	1	0	0	0	X	8
1	0	0	0	0	X	16
1	1	1	1	1	X	31

10.“0” = V_{IL}, “1” = V_{IH}.

Functionality
Modes of Operation: Serial and Direct Parallel

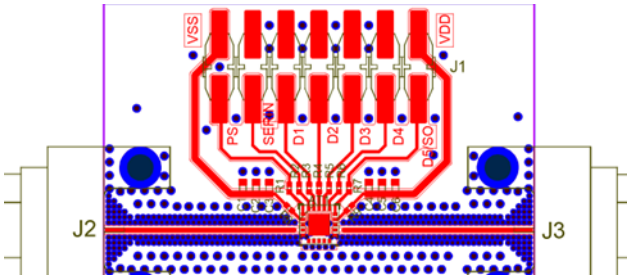
Serial Input Interface Timing Diagram



Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	+25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

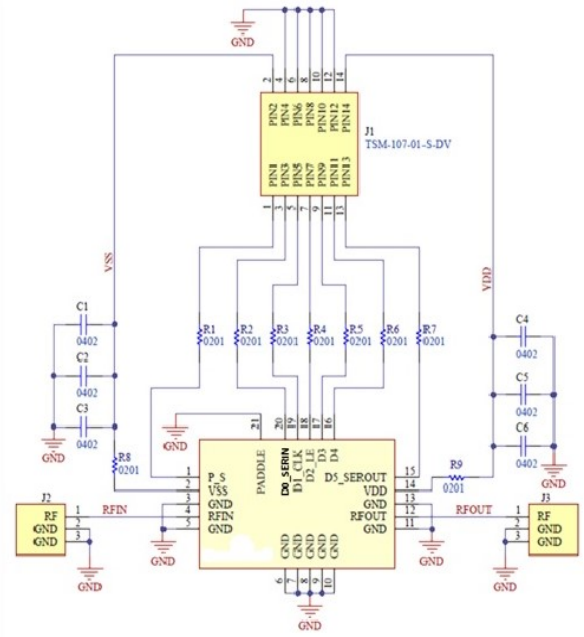
PCB Layout



Parts List

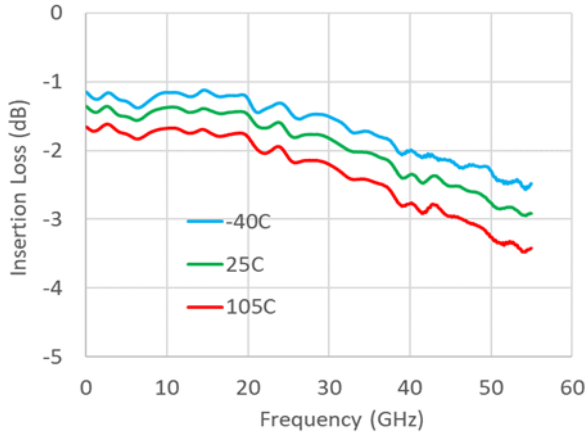
Part	Value	Case Style
AT1	MAAD-011048	3 mm, 20 Lead
C1, C6	Capacitor, 1 µF, 50 V	0402
C2, C5	Capacitor, 10 nF, 50 V	0402
C3, C4	Capacitor, 100 pF, 50 V	0402
R1 - R9	Resistor, 0 Ω	0201
J2 - J3	Southwest 1492-03A-5	End Launch 2.4 mm Female
J1	DC Connector	TSM-107-01-S-DV

Application Schematic

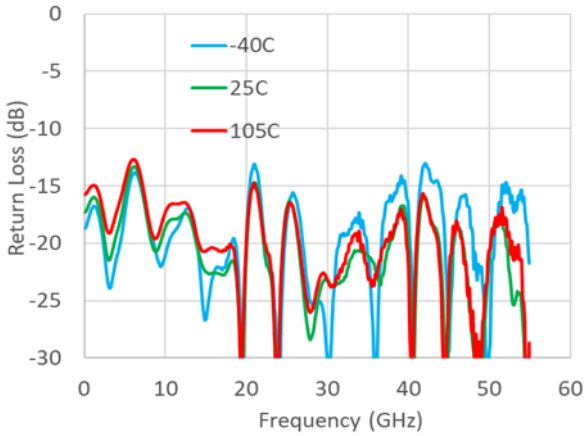


Typical Performance Curves

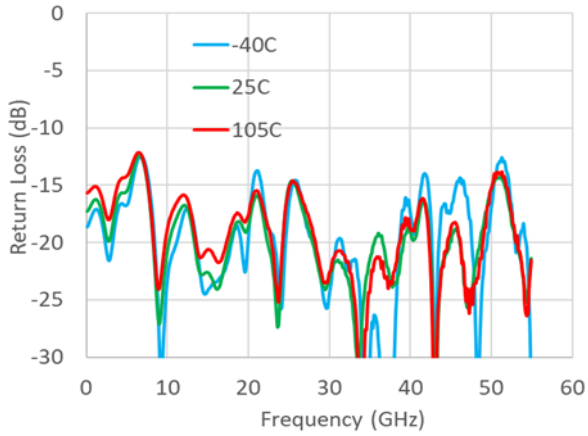
Insertion Loss



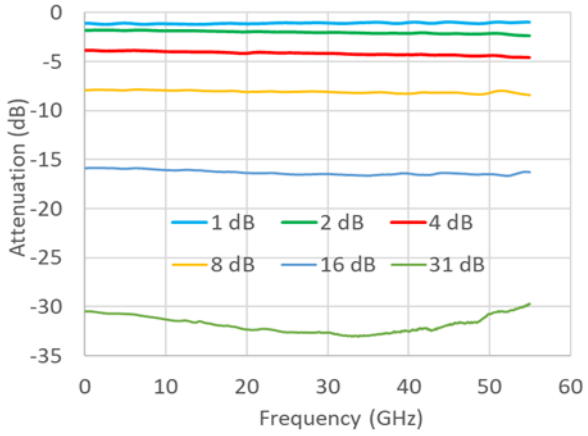
Input Return Loss - Reference State



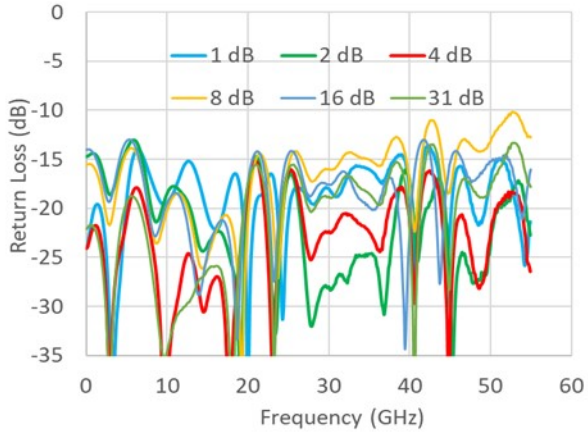
Output Return Loss - Reference State



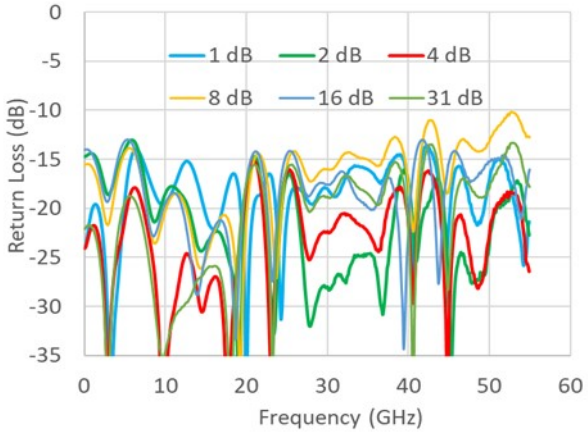
Attenuation - Major Bits



Input Return Loss - Major Bits

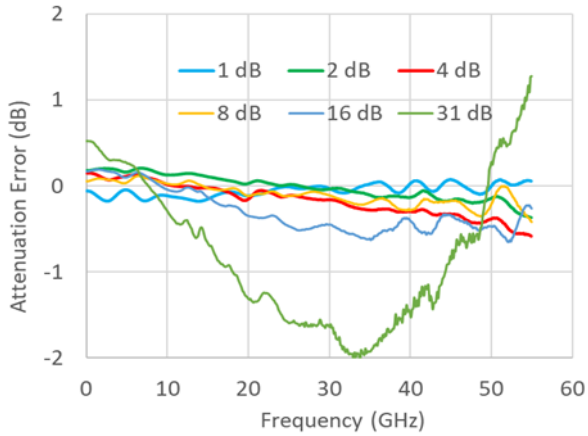


Output Return Loss - Major Bits

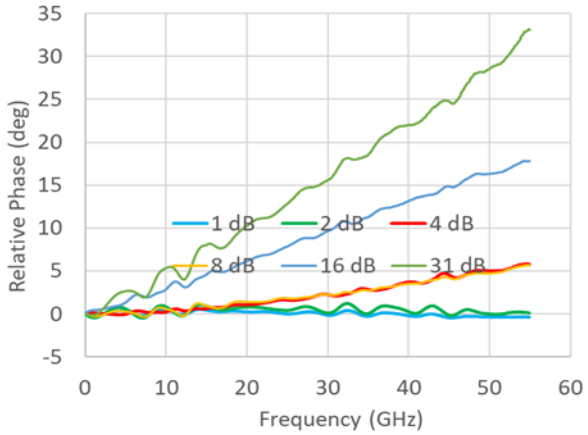


Typical Performance Curves

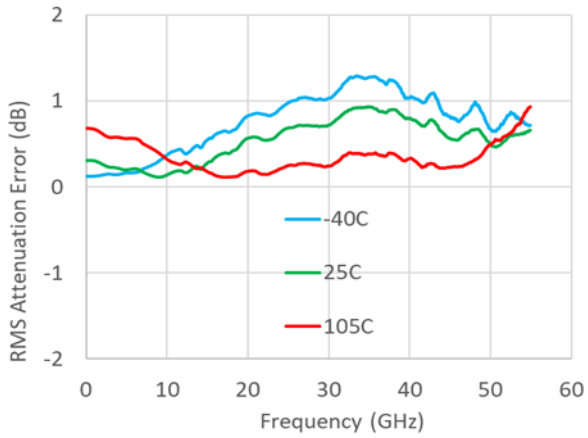
Attenuation Error - Major Bits



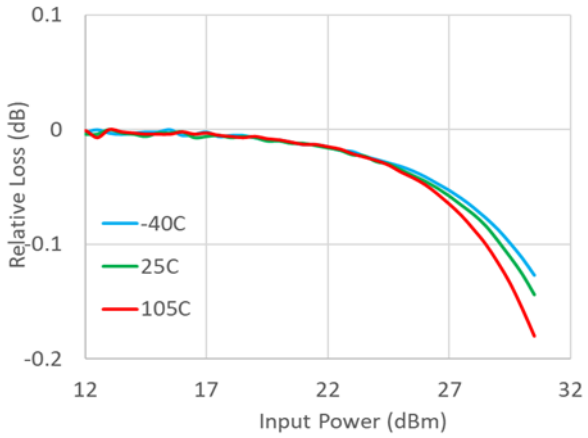
Relative Phase - Major Bits



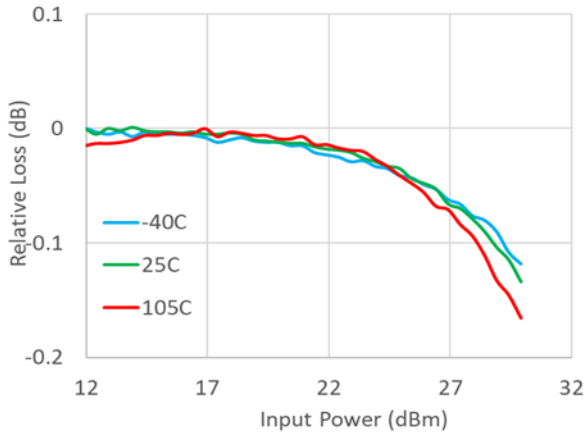
RMS Attenuation Error



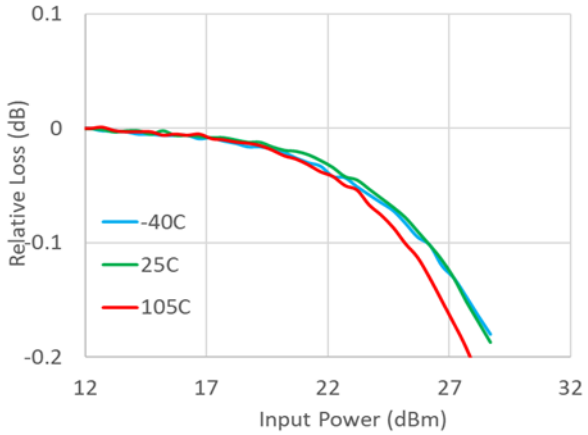
Ref. State Insertion Loss Compression - 100 MHz



Ref. State Insertion Loss Compression - 10 GHz

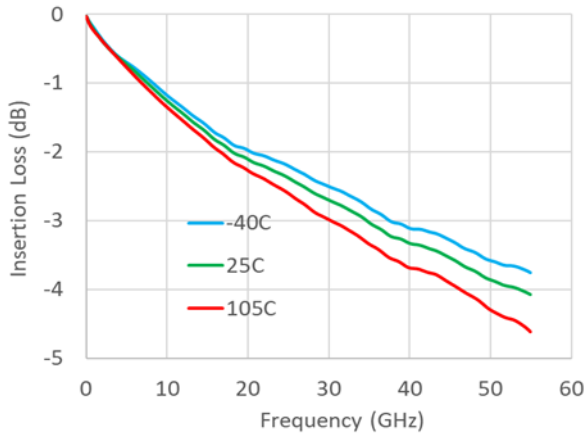


Ref. State Insertion Loss Compression - 40 GHz

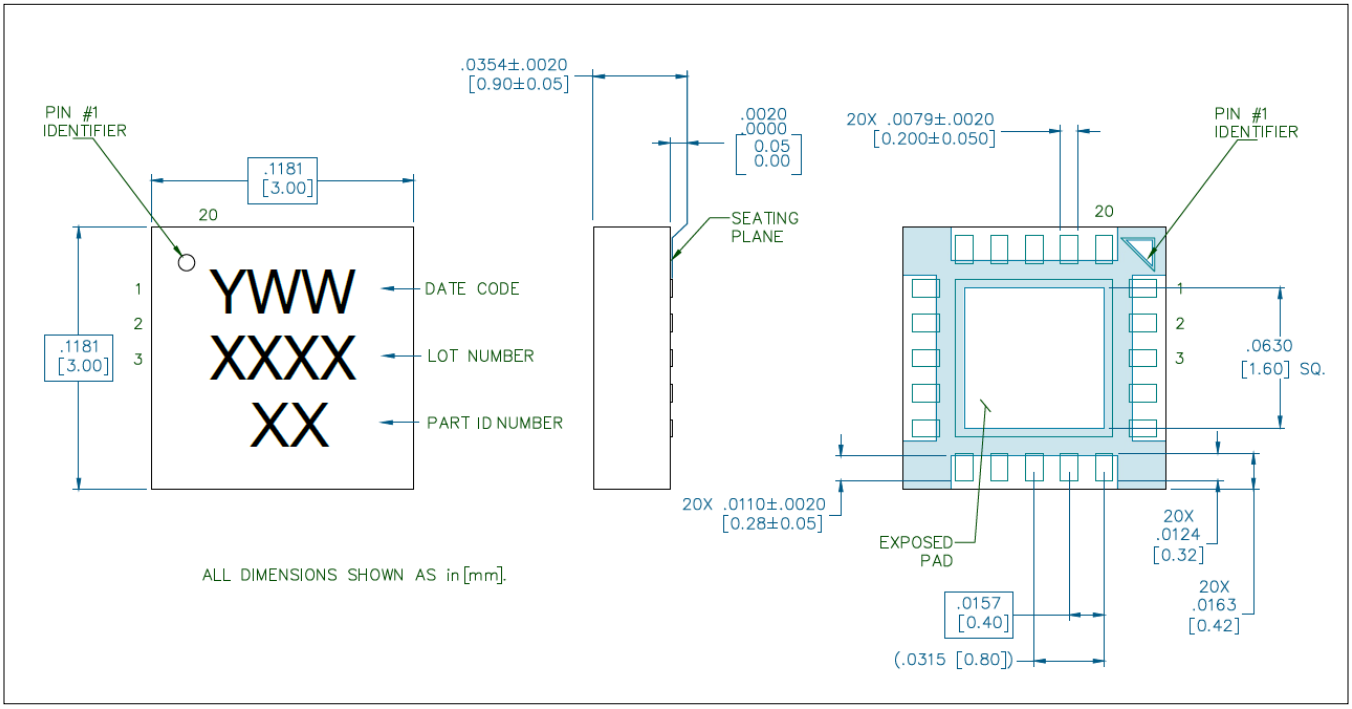


Typical Performance Curves

Evaluation Board Thru Line Insertion Loss



Lead-Free 3 mm, 20-Lead Laminate Package†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements in accordance to JEDEC J-STD-020D.
Plating is 100% NiPdAg over copper.