M21234-33

Wideband (SD/HD-SDI) Adaptive Co-axial Cable Equalizer

Rev V2

Features

- SMPTE/DVB-ASI compliant from 143 to 1485 Mbps operation
- CML, LVPECL and LVDS selectable output modes
- Improved distance: cable EQ up to 350m SD and 175m HD
- Low Power (125 mW @ 1.8V, 175 mW @ 2.5V, 230 mW @ 3.3V)
- Extended Temperature range: -10 to 85°C

Applications

- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

Standards Compliance

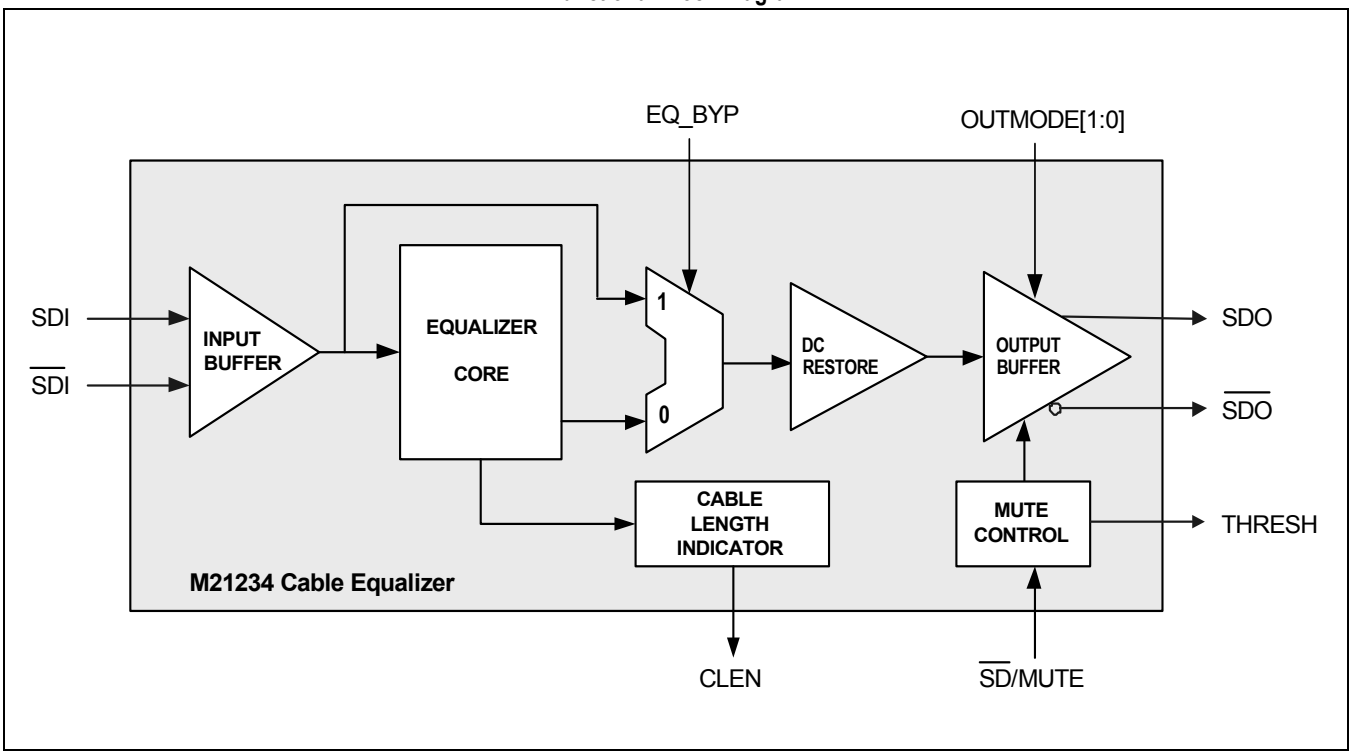
- SMPTE 259M, SMPTE 292M, SMPTE 344M

The M21234 is a high-speed, low-power, adaptive co-axial cable equalizer designed to increase the maximum low-jitter transmission distance of serial digital interface (SDI) video signals and DVB-ASI across commonly used bandwidth-limiting 75Ω coaxial cable. This device automatically optimizes its transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable as well as remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

The M21234 is designed to support SMPTE (292M) at HD data rates as well as SMPTE (259M and 344M) at SD data rates between 143 Mbps and 540 Mbps.

The low-noise, high-gain equalizer allows for low jitter (output jitter of 0.25 UI pp @ 1.485 Gbps) HD transmissions up to a typical cable length of 175m (Belden 1694A) and 130m (Belden 8281). For SD data rates, a typical cable length of 350m (Belden 1694A) and 275m (Belden 8281) at 270 Mbps SD rate (with typical output jitter of 0.20 UI) is supported.

Functional Block Diagram



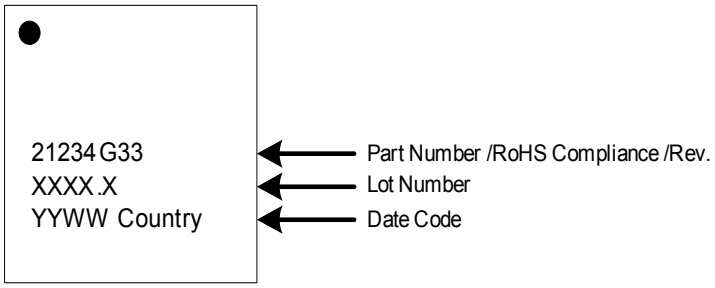
Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21234-33	32-pin QFN	143 - 1485 Mbps	–10°C to 85°C
M21234G-33*	32-pin QFN (RoHS compliant)	143 - 1485 Mbps	–10°C to 85°C
* The letter "G" designator after the part number indicates that the device is RoHS-compliant.			

Revision History

Revision	Level	Date	Description
V2	Release	December 2015	Updated package details (Figure 2-2). Package effective as of July 2014.
B (V1)	Release	April 2010	Updated part revision number in ordering information table. Updated to release status.
A (V1A)	Advance	May 2005	Initial Release

M21234 Marking Diagram



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1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AV_{DD}	Positive Supply	AV_{SS} - 0.5V	AV_{SS} + 3.6	V
T_{STORE}	Storage Temperature	– 65	+ 150	°C
$V_{ESD, HBM}$	Human Body Model (low-speed)	2000	—	V
$V_{ESD, HBM}$	Human Body Model (high-speed)	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

NOTES:

1. No Damage.

Table 1-2. Recommended Operating Conditions

Parameter	Notes	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	1	AV_{DD}	1.71	1.8/2.5/3.3	3.47	V
Ambient Temperature	—	T_{CASE}	-10	—	+85	°C
Junction to Ambient Thermal Resistance	2,3	θ_{JA}	—	40	—	°C/W

NOTES:

1. -33 revision supports 2.5V and 3.3V operation.
2. Mounted on multilayer board (≥ 4 layers).
3. Airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
I_{DD}	Supply Current	1	—	70	80	mA
P_{TOTAL}	Total Power Dissipation (@1.8V)	1, 2,3	—	125	145	mW
P_{TOTAL}	Total Power Dissipation (@2.5V)	1, 2,3	—	175	210	mW
P_{TOTAL}	Total Power Dissipation (@3.3V)	1, 2,3	—	230	280	mW

NOTES:

1. Recommended operating conditions - see Table 1-2.
2. Includes on-chip power dissipation as well as off-chip power dissipated by termination resistors.
3. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage + 5%.

Table 1-4. CMOS Input/Output Electrical Specifications (Logic Signals Only)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
V_{OH}	Output Logic High Voltage	1	0.8 x AV_{DD}	AV_{DD}	—	V
V_{OL}	Output Logic Low Voltage	1	—	0.0	0.2 x AV_{DD}	V
I_{OH}	Output Current (logic High)	1	–10	—	0	mA
I_{OL}	Output Current (logic Low)	1	0	—	10	mA
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	—	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	—	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic high)	1	–100	—	100	µA
I_{IL}	Input Current (logic low)	1	–100	—	100	µA
t_R	Output Rise Time (20-80%)	1	—	—	10	ns
t_F	Output Fall Time (20-80%)	1	—	—	10	ns

NOTES:

1. Specified at recommended operating conditions – see Table 1-2. Spec is for a max load of 20 pF.

Table 1-5. High-Speed Input Electrical Specifications

Parameter	Notes	Minimum	Typical	Maximum	Unit
Input Bit Rate	1	143	—	1485	Mbps
Input Single-ended Voltage (P-P) @ 0m cable	1	500	800	1800	mV
Input Common-Mode Voltage	1	—	0.72 x AV_{DD}	—	mV
Maximum Input High Voltage	1	—	—	AV_{DD} + 500	mV
Minimum Input Low Voltage	1	AV_{DD} - 1.6	—	—	mV
Input capacitance	1	—	0.5	—	pF
Input resistance	1	—	1.64	—	kΩ
Input Return Loss (5 MHz to 1.5 GHz)	1, 2	—	25	—	dB

NOTES:

1. Specified at recommended operation conditions - see Table 1-2.
2. Using the recommended input termination shown in Figure 3-2.

Table 1-6. Output Electrical Specifications

Parameter	Notes	Minimum	Typical	Maximum	Unit
Rise/Fall Time (20% - 80%)	1, 2	—	120	150	ps
Common mode Voltage Outmode[1:0] = 00 (CML, 750 mV)	1, 3	—	AV_{DD} – 0.25	—	V
Differential Output Voltage p-p Outmode[1:0] = 00 (CML, 750 mV)	1, 3	700	800	900	mV
Common mode Voltage Outmode[1:0] = 01 (CML, 500 mV)	1, 3	—	AV_{DD} – 0.15	—	V
Differential Output Voltage p-p Outmode[1:0] = 01 (CML, 500 mV)	1, 3	450	500	550	mV
Common mode Voltage Outmode[1:0] = 10 (LVDS, 700 mV)	1, 2	1.1	1.2	1.3	V
Differential Output Voltage p-p Outmode[1:0] = 10 (LVDS, 700 mV)	1, 2	600	700	800	mV
Common mode Voltage Outmode[1:0] =11 (LVPECL, 1600 mV)	1, 2	—	AV_{DD} – 1.3	—	mV
Differential Output Voltage Outmode[1:0] =11 (LVPECL, 1600 mV)	1, 2	1400	1600	1800	mV

NOTES:

1. Specified at recommended operation conditions - see Table 1-2.
2. With 100Ω differential termination.
3. With 50Ω to AV_{DD} termination.

Table 1-7. Cable Equalizer Distance Specifications

Parameter	Conditions	Notes	Minimum	Typical	Maximum	Unit
Max Cable Length	AV_{DD} = 3.3V, 270 Mbps, PRBS and Pathological Data, Belden 1694A	1, 2, 3, 4		350		m
Max Cable Length	AV_{DD} = 2.5V, 270 Mbps, PRBS and Pathological Data, Belden 1694A	1, 2, 3, 4		315		m
Max Cable Length	AV_{DD} = 3.3V, 270 Mbps, PRBS and Pathological Data, Belden 8281	1, 2, 3, 4		275		m
Max Cable Length	AV_{DD} = 2.5V, 270 Mbps, PRBS and Pathological Data, Belden 8281	1, 2, 3, 4		265		m
Max Cable Length	AV_{DD} = 3.3V, 1485 Mbps, Eq Pathological Data, Belden 1694A	1, 2, 3, 5		175		m
Max Cable Length	AV_{DD} = 3.3V, 1485 Mbps, 2^{23-1} PRBS Data, Belden 1694A	1, 2, 3, 5		200		m
Max Cable Length	AV_{DD} = 2.5V, 1485 Mbps, Eq Pathological Data, Belden 1694A	1, 2, 3, 5		160		m
Max Cable Length	AV_{DD} = 2.5V, 1485 Mbps, 2^{23-1} PRBS Data, Belden 1694A	1, 2, 3, 5		185		m
Max Cable Length	AV_{DD} = 3.3V, 1485 Mbps, Eq Pathological Data, Belden 8281	1, 2, 3, 5		130		m
Max Cable Length	AV_{DD} = 3.3V, 1485 Mbps, 2^{23-1} PRBS Data, Belden 8281	1, 2, 3, 5		150		m
Max Cable Length	AV_{DD} = 2.5V, 1485 Mbps, Eq Pathological Data, Belden 8281	1, 2,3, 5		115		m
Max Cable Length	AV_{DD} = 2.5V, 1485 Mbps, 2^{23-1} PRBS Data, Belden 8281	1, 2, 3, 5		140		m

NOTES:

1. Specified at recommended operating conditions - see Table 1-2
2. Distance measured with a bit error rate (BER) of 1x10-12 or better
3. Distance measured using MACOM's M21232 cable driver to launch signal on cable as indicated.
4. 0.2 UI output jitter
5. 0.25 UI output jitter

Table 1-8. Cable Length Indicator Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
V_{CLEN}	Belden 1694A	1, 2	—	(AV_{DD}-0.9V) - (0.0015 x Cable Length)	—	V
V_{CLEN}	Belden 8281	1, 2	—	(AV_{DD}-0.9V) - (0.0021 x Cable Length)	—	V

NOTES:

1. Specified at recommended operating condition – see Table 1-2.
2. Cable Length Transfer equations valid for all bit rates.

Table 1-9. Mute Threshold Indicator Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
$V_{TH, CLEN}$	Mute threshold (all rates with 1694A cable)	1, 2	—	AV_{DD} - (0.0030 X Cable Length)	—	V
$V_{TH, CLEN}$	Mute threshold (all rates with 8281 cable)	1, 2	—	AV_{DD} - (0.0042 X Cable Length)	—	V

NOTES:

1. Specified at recommended operating condition – see Table 1-2.
2. Mute Threshold transfer equations valid for all bit rate.

Table 1-10. $\overline{SD}$/MUTE Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
$V_{TH, LOS-DEASSERT}$	Output voltage when input signal detected ($\overline{SD}$/MUTE)	1	—	0.55	—	V
$V_{TH, LOS-DEASSERT}$	Output voltage when input signal not detected ($\overline{SD}$/MUTE)	1	—	0.806 x AV_{DD}	—	V

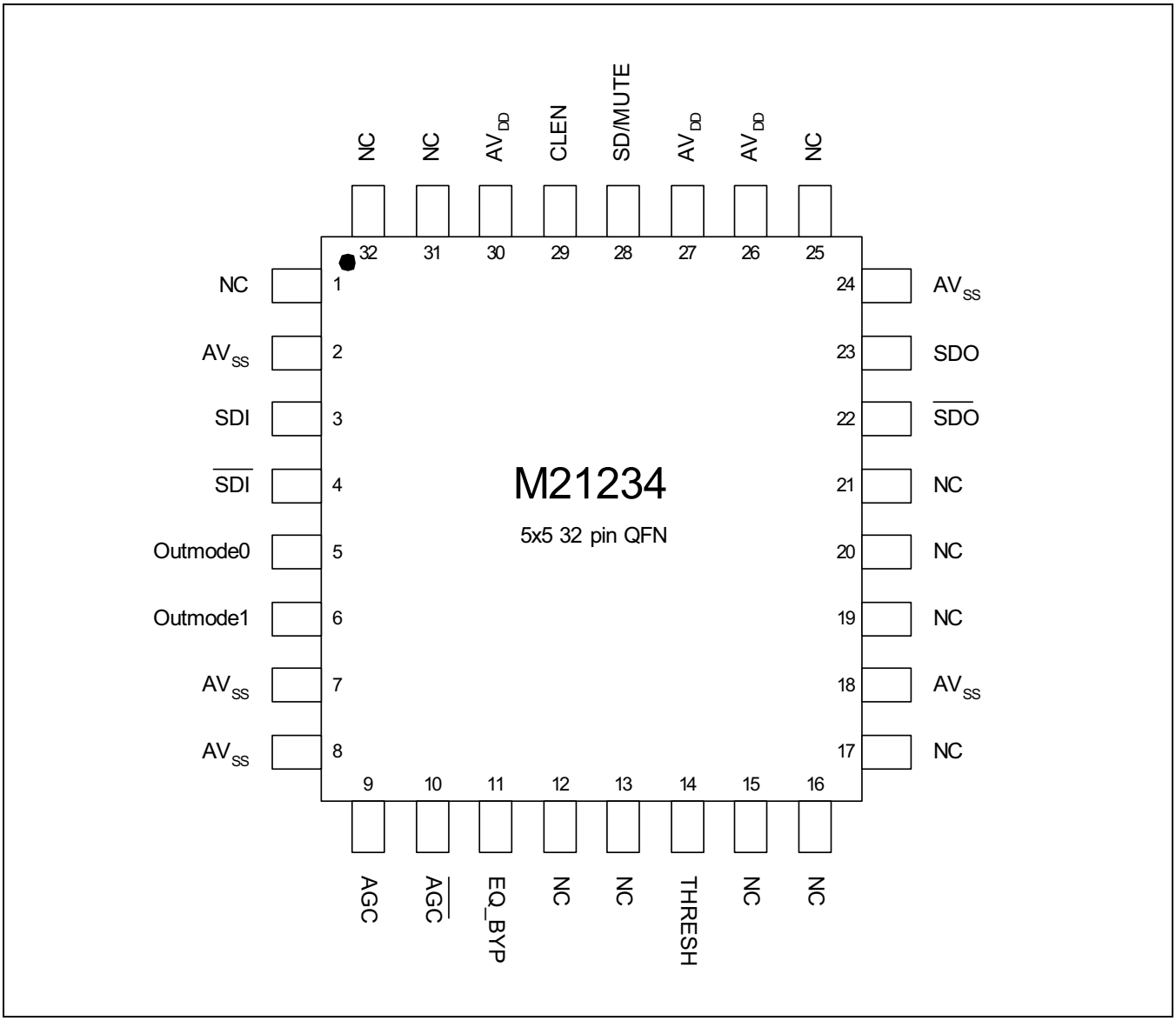
NOTES:

1. Specified at recommended operating condition – see Table 1-2.

2.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

The M21234 pin assignments are illustrated in Figure 2.1. The M21234 is available in a standard Pb-type package or in a RoHS compliant package.

Figure 2-1. M21234 Pin Diagram



2.1 Pin Signals by Interface

Table 2-1. Power Pins

Pin Name	Pin Number	Type	Description
AV_{SS}	2, 7, 8, 18, 24	Power	Ground
AV_{DD}	26, 27, 30	Power	Positive Supply

Table 2-2. High-speed Signal Pins

Pin Name	Pin Number	Type	Function
SDI/$\overline{\text{SDI}}$	3, 4	I-AC coupled high speed	Non-inverting and Inverting Serial Data Input to the adaptive equalizer
$\overline{\text{SDO}}$/SDO	22, 23	O-High speed CML, LVDS or PECL	Non-inverting and Inverting Serial Data Output

Table 2-3. Control/Interface Pins

Pin Name	Pin Number	Type	Function	Default
NC	1	N/A	Do not connect to the pin.	N/A
OUTMODE[1:0]	5, 6	I-CMOS	Output Control Pins: 00: CML, 750 mV_{PP} diff. (default) 01: CML, 500 mV_{PP} diff. 10: LVDS, common mode = 1.2V, 700 mV_{PP} diff. 11: LVPECL, common mode = V_{DD} - 1.3V, 1600 mV_{PP} diff. (only available with 3.3V supply)	Internal pull down
AGC/$\overline{\text{AGC}}$	9, 10	Analog	External AGC (Automatic Gain Control) capacitor connection points. Use 1.0 µF capacitor.	Internal pull up
EQ_BYP	11	I-CMOS	Input control signal that when enabled (High) bypasses the inputs directly to the output stage. Low = Normal operation, High = Disables EQ and bypasses input to output	Internal pull down
NC	12, 13	N/A	Do not connect to the pin.	N/A
THRESH	14	Analog	Input control signal. Programmable cable length forced mute threshold. This function is disabled if **$\overline{\text{SD}}$/MUTE** = Low	Internal pull down
NC	15, 16, 17, 19, 20, 21, 25	N/A	Do not connect to the pin.	N/A

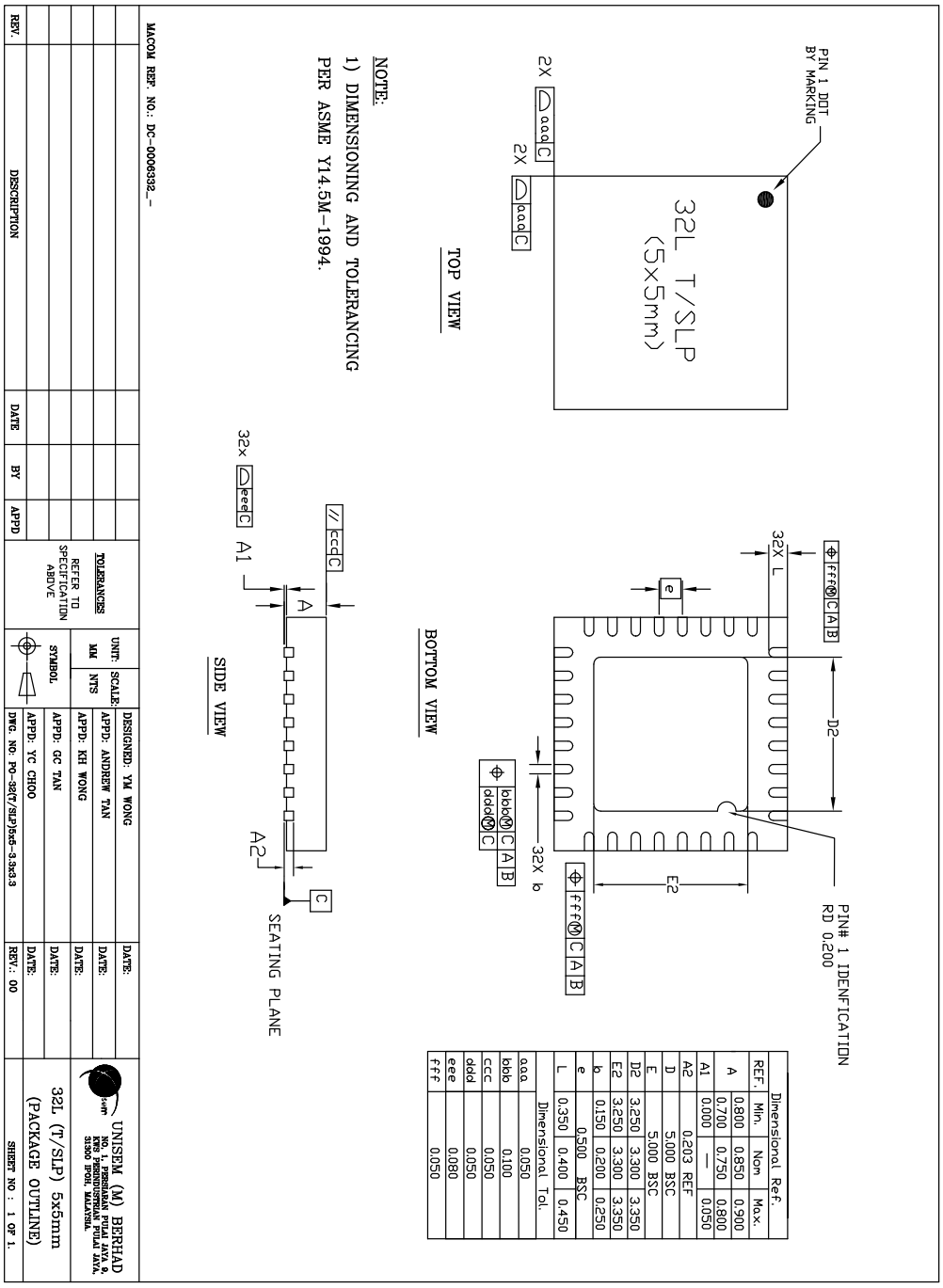
Table 2-3. Control/Interface Pins

Pin Name	Pin Number	Type	Function	Default
$\overline{SD}$/MUTE	28	I/O	Bidirectional Signal that can be used as an input control signal or as an output status indicator. When configured as an input by forcing a voltage on **$\overline{SD}$/MUTE** = High (V_{DD}), the output of the M21234 will be inhibited at logic low (outputs muted). When **$\overline{SD}$/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled. When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled Configured as Output: Low = V_{SS} = Input signal detect High = V_{DD} = Loss of signal Configured as Input: Low = V_{SS} = Never mute High = V_{DD} = Force Mute	—
CLEN	29	Analog	Cable length Indicator output	—
NC	31, 32	N/A	Do not connect to the pin.	N/A

NOTES:

Internal pull-up/pull-down is 100 kΩ

Figure 2-2. M21234 Packaging Details



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
A1	0.000	0.750	0.800
A2		0.203 REF	0.050
D		5.000 BSC	
E		5.000 BSC	
D2	3.250	3.300	3.350
E2	3.250	3.300	3.350
b	0.150	0.200	0.250
e		0.500 BSC	
L	0.350	0.400	0.450
Dimensional Tol.			
aaa			0.050
bbb			0.100
ccc			0.050
ddd			0.050
eee			0.080
fff			0.050

1. For dimensions reference A, Min. is 0.800, Nom is 0.850 and Max. is 0.900.
2. New Unisem Package and the old Amkor package have the same footprint dimensions.

2.2 Manufactureability

The values shown in this section may change; however, these are standard requirements.

2.2.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85°C during Latchup testing.

2.2.2 Peak Reflow Temperature

M21234 (Std Pb-type package): Peak reflow temperature is 220 to 225°C per JEDEC standards.
M21234G (RoHS compliant package): Peak reflow temperature is 260°C per JEDEC standards.

2.2.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

2.3 Design Considerations

See Digital Video Interfacing Application Note (212xx-APP-001-A) for guidance on the following:

- Component Placement and Layout
- Routing Considerations

2.3.1 Thermal Considerations

The M21234 consumes less power than legacy devices, therefore the M21234 will contribute less thermal energy and should result in a lower operating temperature.

3.0 Functional Description

3.1 Overview

The M21234 is a high-speed, low-power, adaptive co-axial cable equalizer designed to increase the maximum low-jitter transmission distance of serial digital interface (SDI) video signals and DVB-ASI across commonly used bandwidth-limiting 75Ω coaxial cable. This device automatically optimizes its transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable as well as remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

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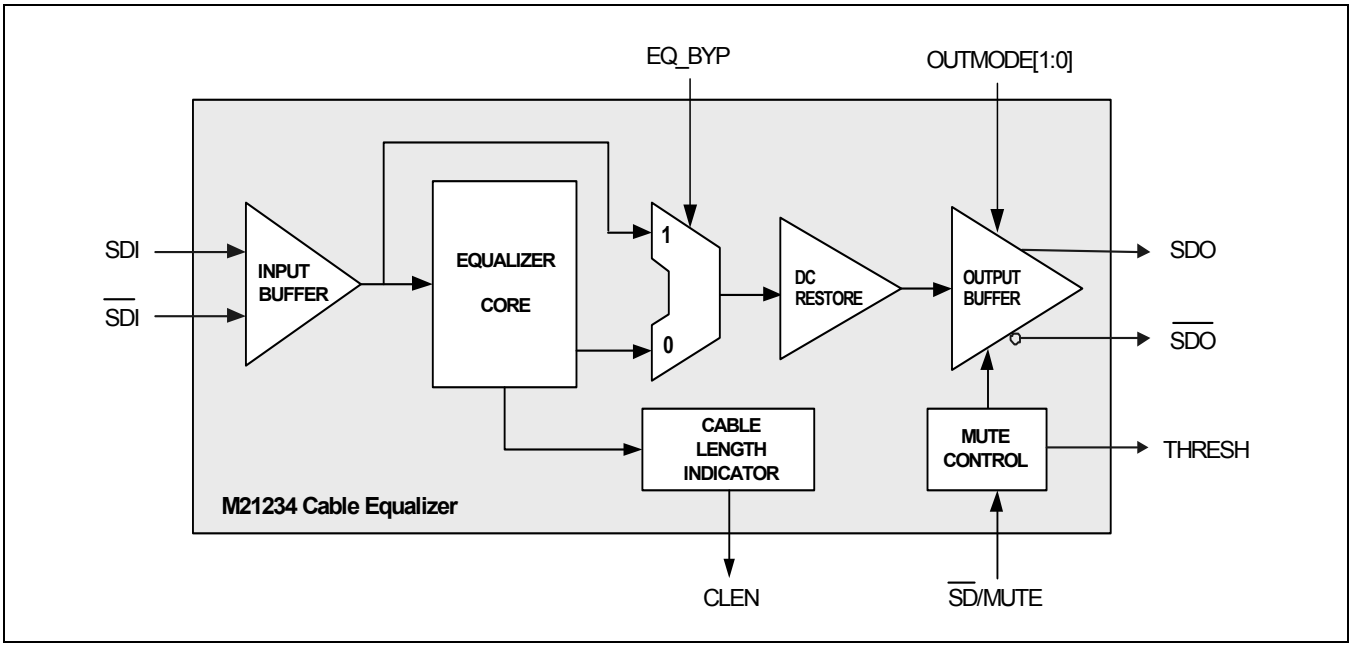
Figure 3-1. M21234 Block Diagram



3.2 Features

- SMPTE/DVB-ASI compliant from 143 to 1485 Mbps operation
- CML, LVPECL and LVDS selectable output modes
- Improved distance: cable EQ up to 350m SD and 175m HD
- Low Power (125 mW @ 1.8V, 175 mW @ 2.5V, 230 mW @ 3.3V)
- Extended Temperature range: -10 to 85°C

3.3 Applications

- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

3.4 Pin Descriptions

3.4.1 General Nomenclature

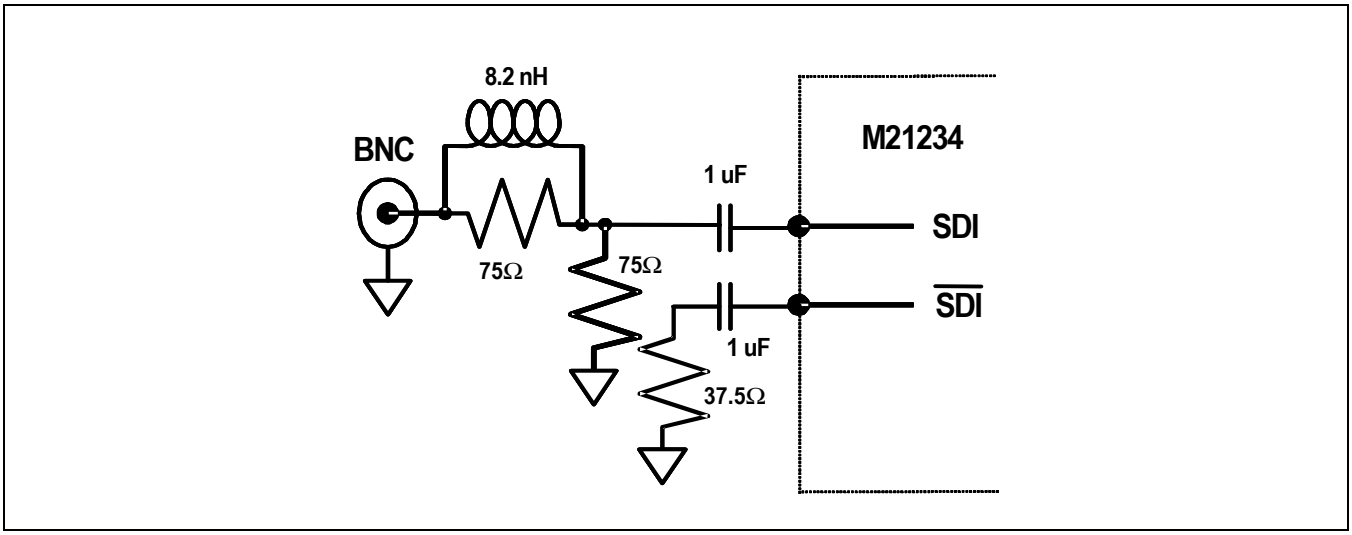
Throughout this data sheet, physical pins will be denoted in **BOLD** print. An array of pins can be called by each individual pin name (e.g. **MF0, MF1, MF2, MF3**, and **MF6**) or as an array (e.g. **MF[0...3,6]** or **MF[0:3,6]**]).

3.4.2 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs, **SDI/$\overline{\text{SDI}}$**, which, are designed to operate in both the single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **SDI** input biased to match the bias on the input used.

The M21234 does not contain any internal input terminations and requires both external input termination as well as the matching circuit to exceed the SMPTE input return loss specifications. The package and IC design of the M21234 has been optimized for high-speed performance allowing it to exceed the SMPTE return loss spec by 5 dB to 10 dB external matching/termination network and commonly employed right-angle, through-hole, or vertical mount 75Ω BNC connectors. For non-inverting single-ended operation, the recommended input circuit is shown in Figure 3-2. For differential operation, the matching/termination circuit on **SDI** should be duplicated on **SDI**. The internal pull ups automatically bias **SDI/SDI** to 0.72 x $\mathbf{AV_{DD}}$ for proper AC coupled operation.

Figure 3-2. Single-ended Typical Input Matching/termination Network



3.4.3 High-Speed Output

The high-speed differential outputs after equalization are made available on the **SDO/$\overline{\text{SDO}}$** pins. The M21234 operates from 1.8V to 3.3V supplies. **Outmode0** and **Outmode1** control what standard of output is used. See below:

OUTMODE[1:0]	Output Mode
00:	CML, 750 mV_{PP} (default)
01:	CML, 500 mV_{PP}
10:	LVDS, common mode = 1.2V, 700 mV_{PP}
11:	LVPECL, common mode = V_{DD} - 1.3V, 1600 mV_{PP} differential (3.3V supply only)

3.4.4 Adaptive Equalization Selection

In typical operation, the adaptive equalization is enabled with **EQ_BYP** = Low; however, with **EQ_BYP** = High, the adaptive equalization and DC restore circuit is bypassed and the input is fed directly to the output.

3.4.5 Cable Length Indicator

When the adaptive equalization is enabled (**EQ_BYP** = Low), an analog voltage inversely proportional to the cable length is made available on **CLEN** and defined by the equation **V_{CLEN} = (V_{DD} - 0.9V) – (slope x Cable length)**. The transfer function of M21234 is designed for all bit rates. The slope is 0.0021 with Belden 8281 and 0.0015 with Belden 1694A. The dynamic range of **CLEN** will exceed older legacy devices. When the adaptive equalization is disabled (**EQ_BYP** = High), the voltage falls to its highest value (it indicates 0m cable length). During an LOS (Loss of input Signal) event, the voltage falls to its lowest value.

3.4.6 Output Mute and Signal Detect

When configured as an input by forcing a voltage on **$\overline{\text{SD}}$/MUTE** = High (V_{DD}), the output of the M21234 will be inhibited at logic low (outputs muted). When **$\overline{\text{SD}}$/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled.

When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled and the pin is defined as an LOS output (logic). In the event of an LOS, the output is muted. The inhibit threshold is set with an analog voltage applied to the **THRESH** input pin. For Belden 1694A, the threshold is set by the following equation: $\mathbf{V_{THRESH} = V_{DD} - (0.0030 \times Cable\ length)}$. This transfer function is designed to match the Gennum part at 3.3V. For Belden 8281 co-axial cable the formula is $\mathbf{V_{THRESH} = V_{DD} - (0.0042 \times Cable\ length)}$. The transfer function is valid at all bit rates.

3.4.7 Equalizer Detailed Description

The basic equalizer design consists of interlaced stages of gain and equalization to maximize both the overall equalization gain as well as the input sensitivity for maximum performance with minimum jitter. In order to achieve 350m distance at 270 Mbps and 175m at 1.485 Gbps with Belden 1694A, the overall equalizer block has over 50 dB of broadband signal boost up to and past 1.5 GHz and maintains an input sensitivity of approximately 10 mV. Using a high-performance silicon process, high gain-bandwidth products are achieved allowing for high-performance, wide dynamic range design with minimum power dissipation.

Since 270 Mbps and 1.485 Gbps signals are launched with different SMPTE specified rise and fall times which can vary substantially (especially at the receive end after going though a wide dynamic range of valid cable lengths) the M21234 equalization routine determines both the bit rate and the resultant signal HF attenuation as opposed to just looking at the launch edge rates. By determining both sets of conditions, it is possible to optimize the equalizer for both HD and SD performance. Therefore, the M21234 maintains the same max. cable length as optimized SD only equalizers. For example, a SD signal through a short cable can have the same edge rate as a HD signal through a long cable; yet, both conditions require different levels of equalization as well as different optimized inverse-transfer functions. The M21234 advanced equalization technology can make the distinction between the two cases for optimal performance. This also leads to proper mute threshold (**THRESH**) and cable length indicator (**CLEN**) operation that is independent of the bit rate.

In order to accommodate both the SMPTE worst case equalizer pathological patterns as well as some customer derived worst case DC offset patterns, a high-gain slicer is included in the signal path to correct for any eye-crossing wander due to AC coupling of the input.