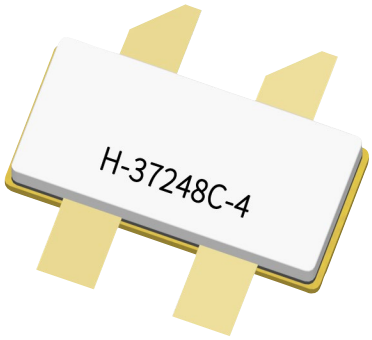
GTRB204402FC/1

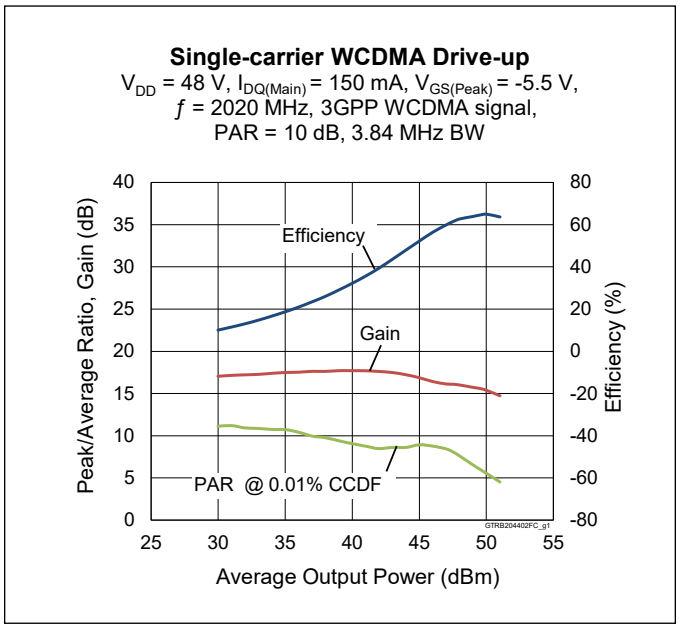
Thermally-Enhanced High Power RF GaN on SiC HEMT
350 W, 48 V, 1930 – 2020 MHz



Package Types: H-37248C-4

Description

The GTRB204402FC/1 is a 350-watt (P3dB) GaN on SiC high electron mobility transistor (HEMT) designed for use in multi-standard cellular power amplifier applications. It features high efficiency, and a thermally-enhanced package with earless flange.



Features

- GaN on SiC HEMT technology
- Typical Pulsed CW performance, 2020 MHz, 48 V, 10 µs pulse width, 10% duty cycle, combined outputs
  - Output power at P_{3dB} = 350 W
  - Efficiency at P_{3dB} = 65%
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Pb-free and RoHS compliant

Typical RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty evaluation board for 1930 to 2020 MHz)
V_{DD} = 48 V, I_{DQ} = 150 mA, $V_{GS(PEAK)}$ = –5.5 V, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

	P_{OUT} (dBM)	Gain (dB)	Efficiency (%)	ACPR+ (dBc)	ACPR– (dBc)	OPAR (dB)
1930 MHz	47.5	15.9	59.7	–27.2	–27.4	8.6
1975 MHz	47.5	16	59.7	–27.1	–27.2	8.7
2020 MHz	47.5	16.1	61.5	–26.6	–26.6	8.1

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Rev. 02.1, 2022-09-18

DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage (main)	$V_{BR(DSS)}$	150	—	—	V	V_{GS} = –8 V, I_D = 10 mA
Drain-source Breakdown Voltage (peak)						
Drain-source Leakage Current (main)	I_{DSS}	—	—	3.1	mA	V_{GS} = -8 V, V_{DS} = 10 V
Drain-source Leakage Current (peak)				6.3		
Gate-source Leakage Current (main)	I_{GSX}	—	—	–5	mA	V_{GS} = -8 V, V_{DD} = 50 V
Gate-source Leakage Current (peak)				–10		
Gate Threshold Voltage (main)	$V_{GS(th)}$	–3.8	–3.1	–2.3	V	V_{DS} = 10 V, I_D = 18 mA
Gate Threshold Voltage (peak)						V_{DS} = 10 V, I_D = 36 mA

Recommended Operating Voltages

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	0	—	50	V	
Gate Quiescent Voltage	$V_{GS(Q)}$	-3.6	–2.9	-2.1		V_{DS} =48 V, I_D = 150 mA

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	125	V
Gate-source Voltage	V_{GS}	–10 to +2	
Operating Voltage	V_{DD}	55	
Gate Current (main)	I_G	18	mA
Gate Current (peak)		36	
Drain Current (main)	I_D	6.75	A
Drain Current (peak)		13.5	
Junction Temperature	T_J	275	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Product's qualification were performed at 225 °C. Operation at T_J (275 °C) reduces median time to failure.

Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	1.8	°C/W	T_{CASE} = 85°C, P_{DISS} = 75 W
Thermal Resistance (peak)		1.0		T_{CASE} = 85°C, P_{DISS} = 136 W

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty production test fixture)

V_{DD} = 48 V, I_{DQ} = 150 mA, P_{OUT} = 56.2 W avg, $V_{GS(PEAK)}$ = –5.5 V, f = 2020 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	12	13	—	dB
Drain Efficiency	η_D	38.5	42	—	%
Adjacent Channel Power Ratio	ACPR	—	–33	–29	dBc
Output PAR @ 0.01% CCDF	OPAR	7.3	7.8	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

Ordering Information

Type and Version	Order Code	Package Description	Shipping
GTRB204402FC/1 V1 R0	GTRB204402FC1V1-R0	H-37248C-4	Tape & Reel, 50 pcs
GTRB204402FC/1 V1 R2	GTRB204402FC1V1-R2	H-37248C-4	Tape & Reel, 250 pcs

Typical Performance (data taken in a production test fixture)

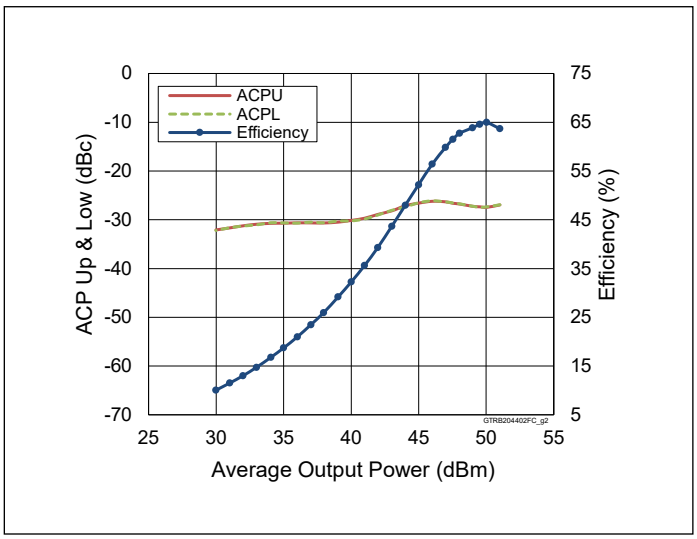


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(Main)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V,
f = 2020 MHz, 3GPP WCDMA signal,
PAR = 10 dB, BW = 3.84 MHz

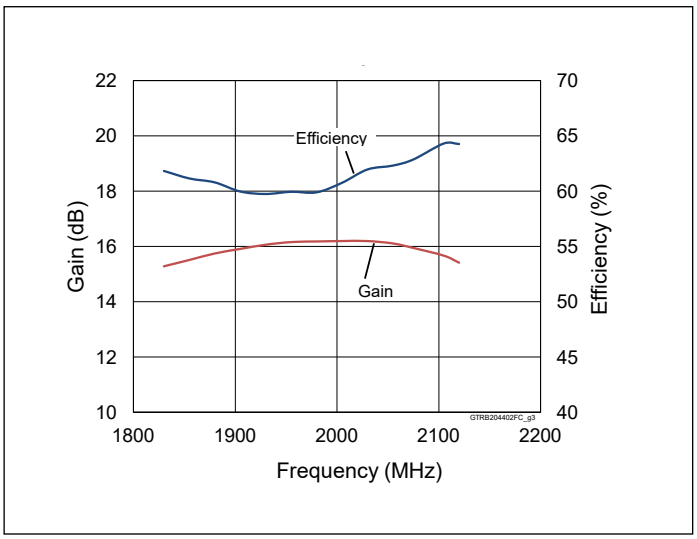


Figure 2. Single-carrier WCDMA Broadband

V_{DD} = 48 V, $I_{DQ(Main)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V,
P_{OUT} = 47.5 dBm, 3GPP WCDMA signal,
PAR = 10 dB

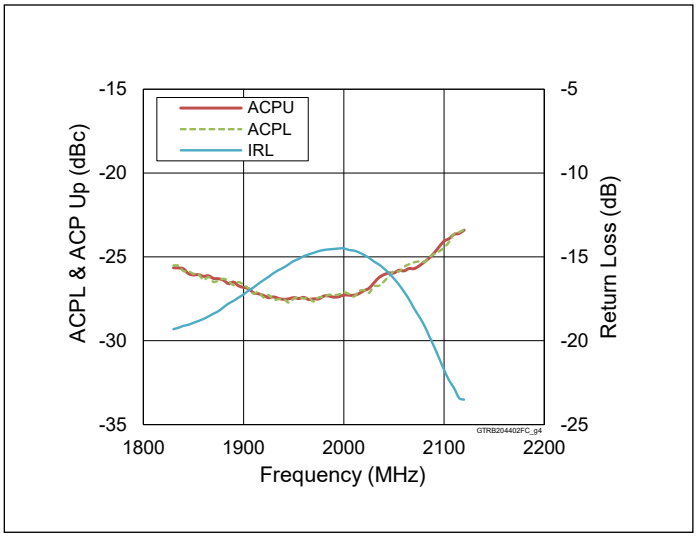


Figure 3. Single-carrier WCDMA Broadband

V_{DD} = 48 V, $I_{DQ(Main)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V,
P_{OUT} = 47.5 dBm, 3GPP WCDMA signal,
PAR = 10 dB

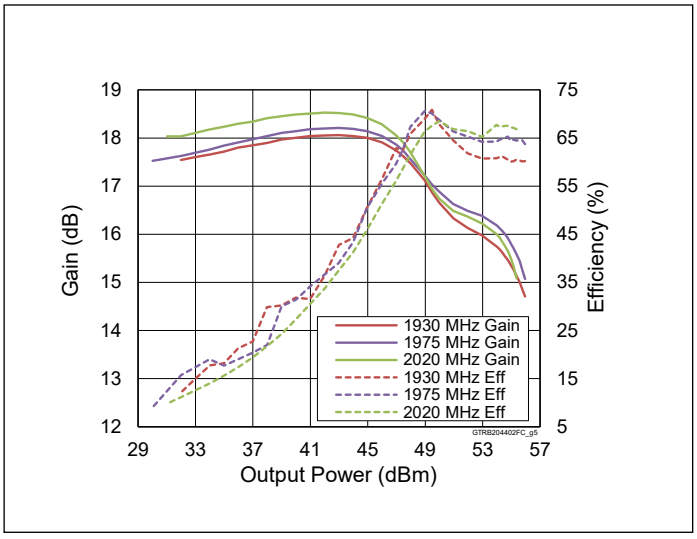


Figure 4. Pulse CW Performance

V_{DD} = 48 V, $I_{DQ(Main)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V

Typical Performance (cont.)

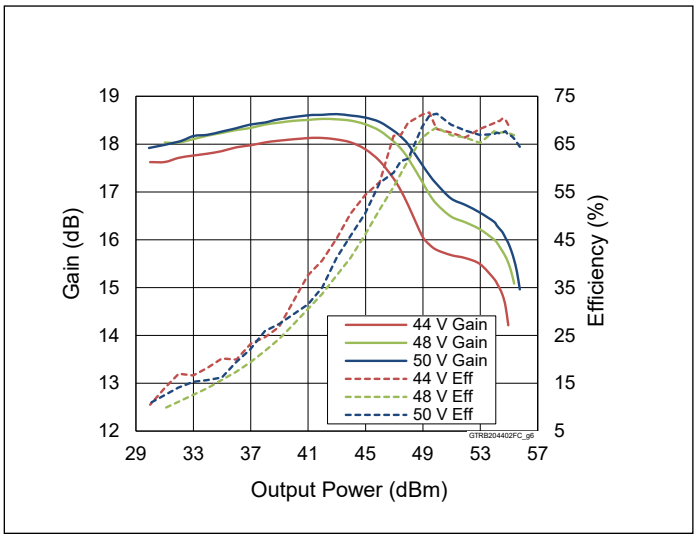


Figure 5. Pulsed CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V,
f = 2020 MHz

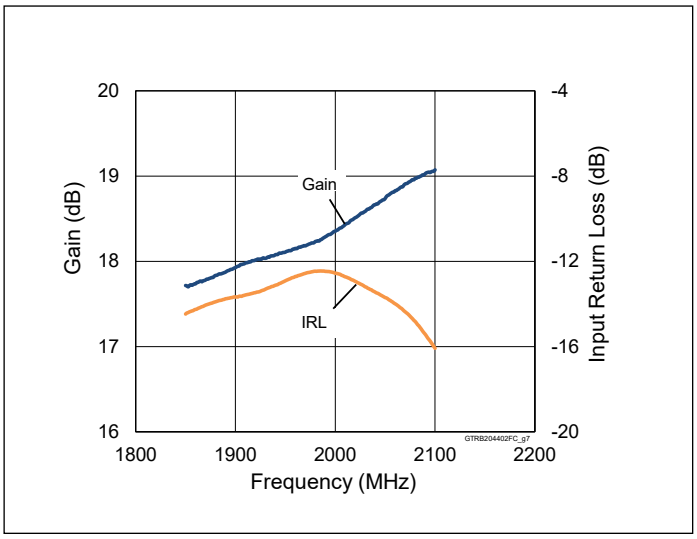


Figure 6. Small Signal CW Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(Main)}$ = 150 mA, $V_{GS(Peak)}$ = -5.5 V

Load Pull Performance

Main side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 48 V, I_{DQ} = 150 mA , class AB

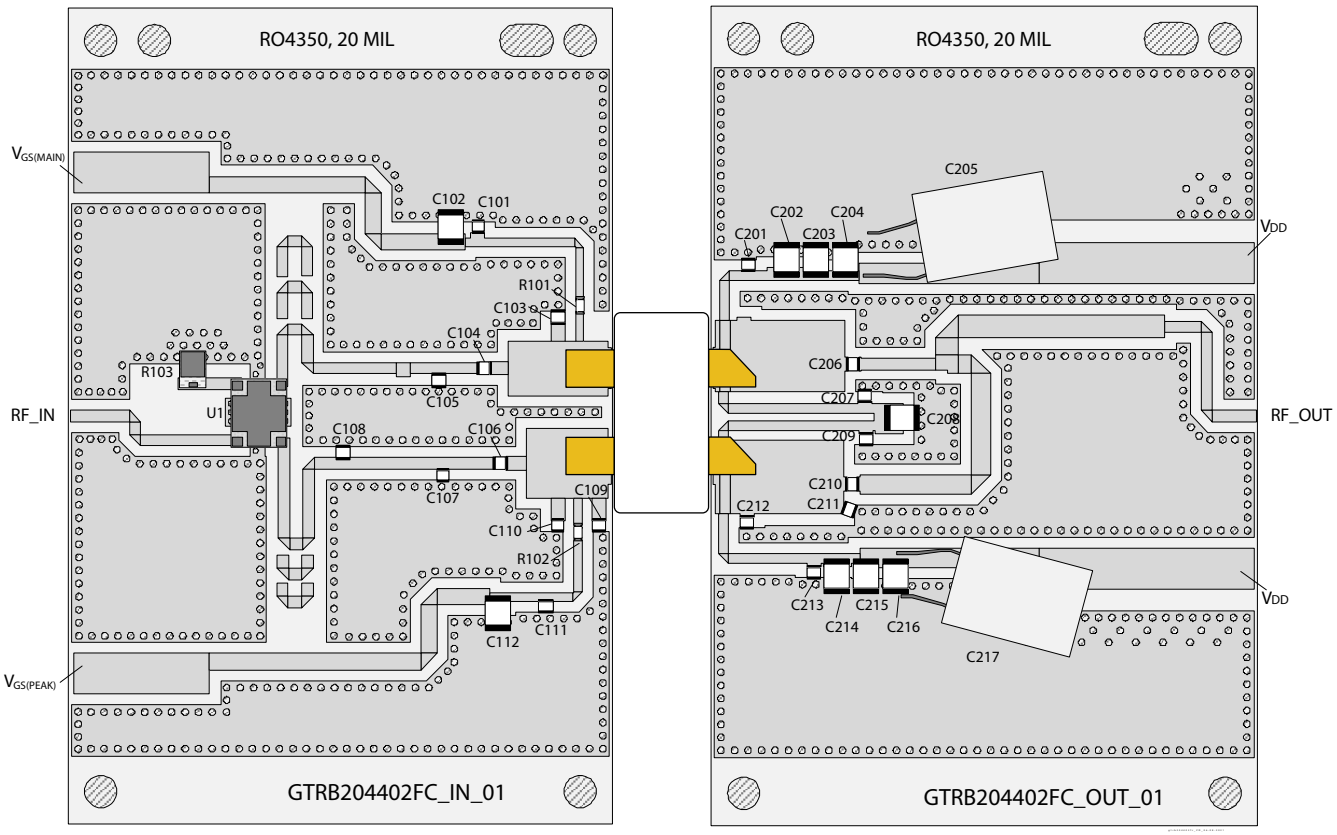
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Z_l [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
1930	5.31-j12.2	7.44-j9.43	17.43	52.66	184.5	74.1	9.59-j1.86	18.9	50.30	107.4	81.9
2025	8.49-j13.1	6.54-j10.39	17.5	52.70	186.2	71.0	7.77-j3.09	19.5	50.40	109.7	83.1

Peak side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 48 V, V_{GSPK} = –5.5 V, class C

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Z_l [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
1930	2.97-j7.14	2.43-j3.67	15.85	55.42	348.3	65.0	2.14-j1.18	15.7	52.53	179.1	78.1
2025	3.10-j8.80	1.92-j3.69	16.5	55.50	354.8	65.1	2.29-j1.96	16.4	53.41	219.3	76.7

Doherty Evaluation Board, 1930 – 2020 MHz

Evaluation Board Part Number	LTAGTRB204402FC1V1
PCB Information	Rogers 4350, 0.508mm [0.020”] thick, 2 oz. copper, ε_r = 3.66



Reference circuit assembly diagram (not to scale)

Components Information

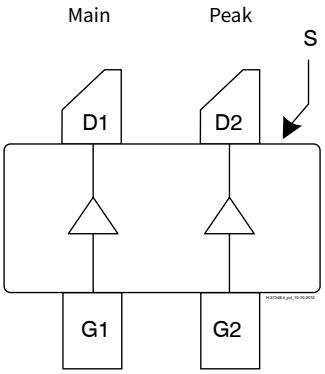
Component	Description	Manufacturer	P/N
Input			
C101, C104, C106, C111	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C102, C112	Capacitor, 100 V, 10 µF	Murata Electronics	GRM32EC72A106KE05L
C103	Capacitor, 1.6 pF	ATC	ATC600F1R6CT250XT
C105	Capacitor, 1.2 pF	ATC	ATC600F1R2CT250XT
C107	Capacitor, 0.8 pF	ATC	ATC600F0R8CT250XT
C108	Capacitor, 0.6 pF	ATC	ATC600F0R6CT250XT
C109	Capacitor, 1.8 pF	ATC	ATC600F1R8CT250XT
C110	Capacitor, 1.5 pF	ATC	ATC600F1R5CT250XT
R101, R102	Resistor, 9.1 ohms	Panasonic Electronic Components	ERJ-3GEYJ9R1V
R103	Resistor, 50 ohms	Richardson	C8A50Z4B
U1	Hybrid Coupler	Anaren	X3C19P1-03S
Output			
C201, C207, C209, C213	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C202, C203, C204, C208, C214, C215, C216	Capacitor, 100 V, 10 µF	Murata Electronics	GRM32EC72A106KE05L
C205, C217	Capacitor, 220 µF	Panasonic Electronic Components	EEE-FP1V221AP
C206	Capacitor, 2.7 pF	ATC	ATC600F2R7CT250XT
C210	Capacitor, 3.0 pF	ATC	ATC600F3R0CT250XT
C211	Capacitor, 0.8 pF	ATC	ATC600F0R8CT250XT
C212	Capacitor, 2.2 pF	ATC	ATC600F2R2CT250XT

Bias Sequencing

Bias ON
1. Ensure RF is turned off
2. Apply pinch-off voltage of –5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF
1. Turn RF off
2. Apply pinch-off voltage to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)

Lead connections for GTRB204402FC/1

Package Outline Specifications – Package H-37248C-4

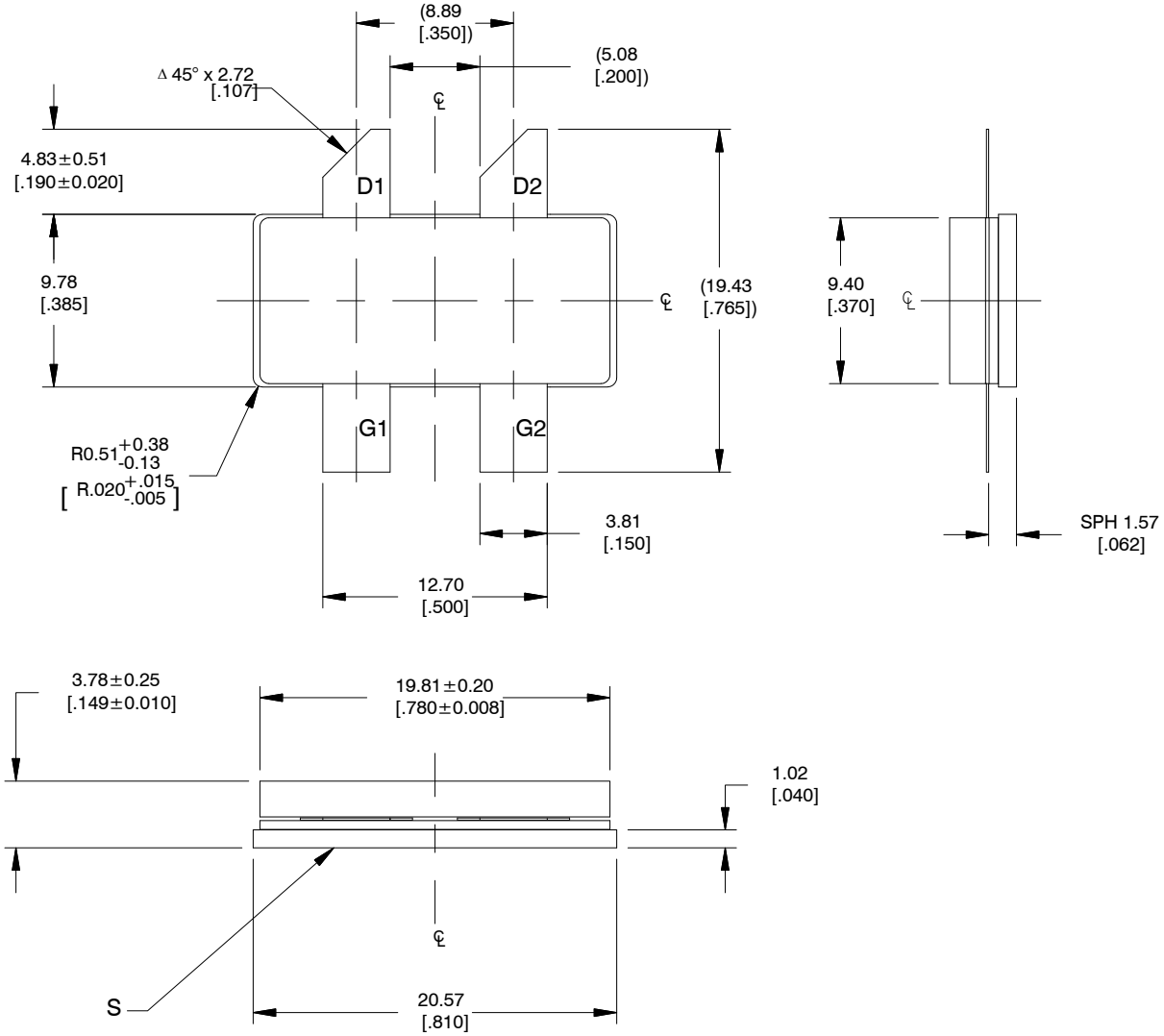


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source (flange)
5. Lead thickness: 0.13 ± 0.05 [.005 ± 0.002].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

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