

Transmit / Receive Module

15 - 18 GHz



ENGSD00083

Rev. V1

Features

- 15 to 18 GHz Band Coverage
- Gain: 23 dB RX / 20 dB TX
- Noise Figure: 3.25 dB
- OIP3: 16 dBm
- TX Saturated Output Power: 1.2 W
- Average PAE @ P_{SAT} : 30%
- Size:
 - 7 x 7 x 1.8 mm
 - (0.276" x 0.276" x 0.071")
- RoHS* Compliant



Applications

- Transmit & Receive Circuits
- Telecom Infrastructure
- SATCOM
- Commercial or Military Radar
- Test & Measurement Systems

Description

The ENGSD00083 is a Transmit/Receive module operating across 15 to 18 GHz. The module provides 23 dB gain in receive mode and 20 dB gain in transmit mode. In receive mode, the module offers typical noise figure of 3.25 dB. In the transmit mode, the module offers typical 1.2 W saturated output power and 30% average PAE. In terminated mode, the antenna port is terminated into 50 ohms. The module is packaged in a ceramic 7 x 7 mm QFN package.

Ordering Information

Part Number	Package
ENGSD00083	bulk

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications @ T_A = 25°C:

Receive Mode:

Freq. = 15 - 18 GHz, VD_LNA = +3.3 V, SW_V0 = +5 V, SW_V1 = -5 V, SW_V2 = +5 V

Parameter	Min	Typ	Max	Units
RX Gain	19	23	25	dB
Noise Figure	—	3.25	4.0	dB
OIP3	14	16	—	dBm
Output P1dB	7	10	—	dBm
RX Input Return Loss	14	17	—	dB
RX Output Return Loss	14	21	—	dB
VD_LNA Supply Current	35	45	55	mA

Transmit Mode:

Freq. = 15 - 18 GHz, VD1_PA = VD2_PA = +20 V, SW_V0 = -5 V, SW_V1 = +5 V, SW_V2 = +5 V

Parameter	Min	Typ	Max	Units
TX Gain	15	20	26	dB
Saturated Output Power	1.0	1.4	—	Watts
PAE at Psat	—	30, average	—	%
TX Input Return Loss	—	6	—	dB
TX Output Return Loss	—	6	—	dB
VD_PA Supply Current (Idq)	90	100	110	mA
VD_PA Supply Current (at Psat)	—	240	300	mA

Terminated Mode:

Freq. = 15 - 18 GHz, SW_V0 = +5 V, SW_V1 = +5 V, SW_V2 = -5 V

Parameter	Min	Typ	Max	Units
Terminated Return Loss	14	20	—	dB

Common Requirements:

Parameter	Min	Typ	Max	Units
Current (+5 V)	8	10	15	mA
Current (-5 V)	8	10	15	
SW_V0, SW_V1, SW_V2				
Switch Isolation	32	36	—	dB
Switching Time 50% CTRL to 90%/10% of detected RF	—	150	200	ns

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD1_PA, VD2_PA	18	20	22	V
VD_LNA	3.0	3.3	4.0	V
SW_V0, SW_V1, SW_V2	-5	-5 or +5	+5	V
VG1_PA, VG2_PA	-1.3	-1.8	-2.2	V
Operating Temperature	-40	+25	+85	°C

Switch Truth Table

State	SW_V0 (V)	SW_V1 (V)	SW_V2 (V)
TX Path ON	-5	+5	+5
RX Path ON	+5	-5	+5
Terminated	+5	+5	-5

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
VD1_PA, VD2_PA	+30 V
VD_LNA	+5 V
SW_V0, SW_V1, SW_V2	+7 V or -20 V
VG1_PA, VG2_PA	-6 V
RX RF Input Power	14 dBm
TX RF Input Power	22 Bm
Storage Temperature	-65°C to +125°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Transmit / Receive Module 15 - 18 GHz



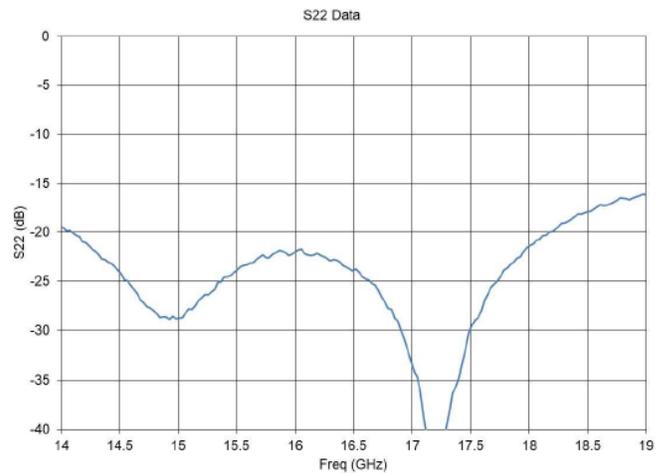
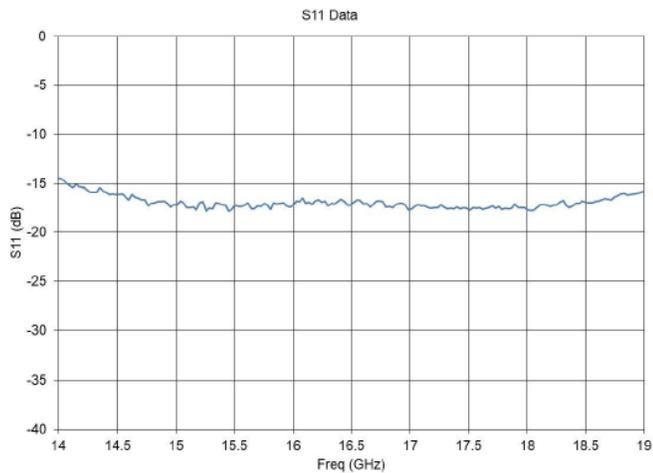
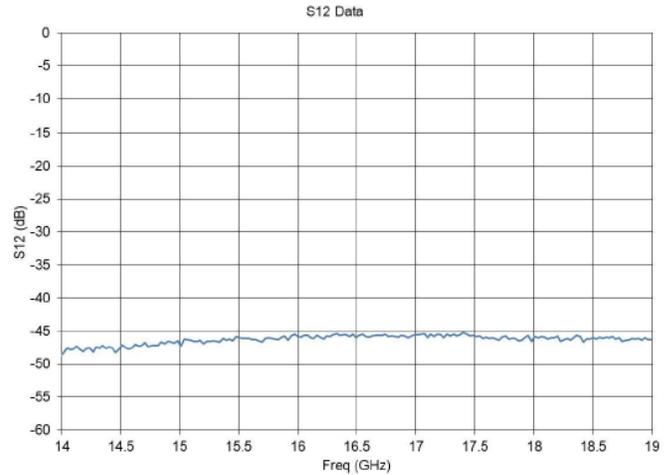
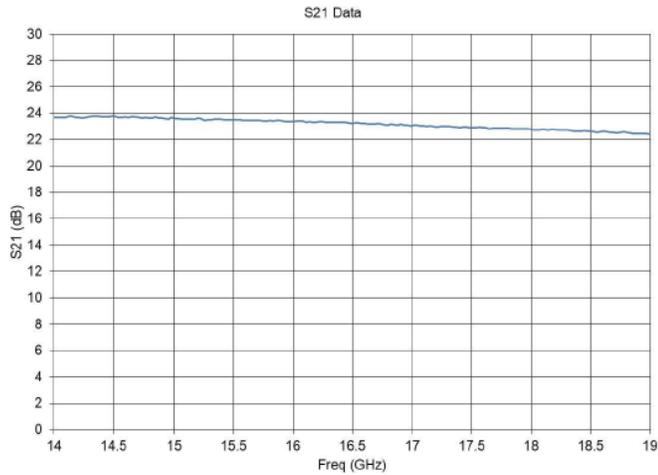
ENGSD00083

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Typical Performance - Receive Mode

Small Signal Gain, Reverse Isolation, Input/Output Return Loss:

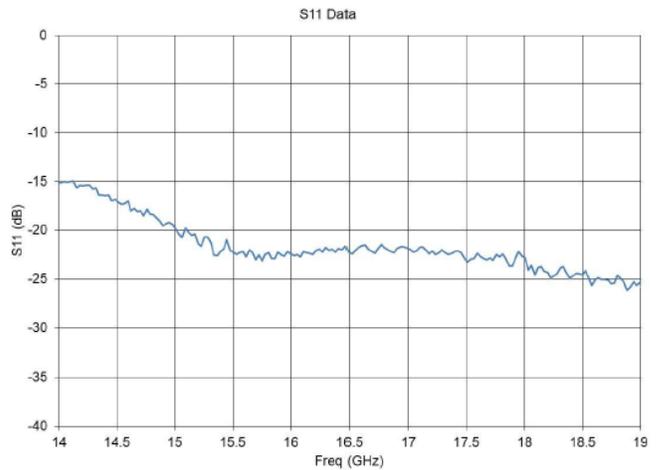
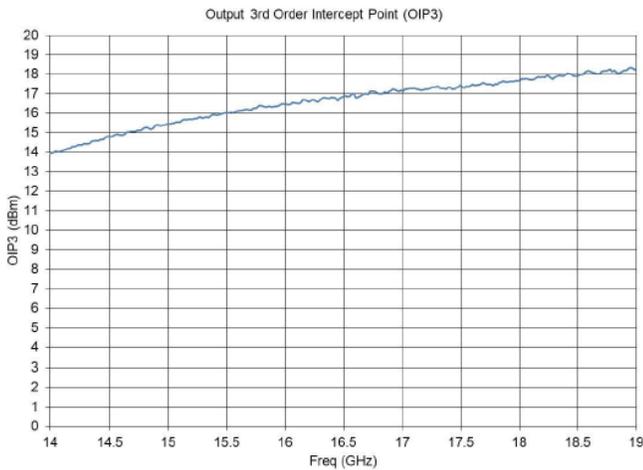
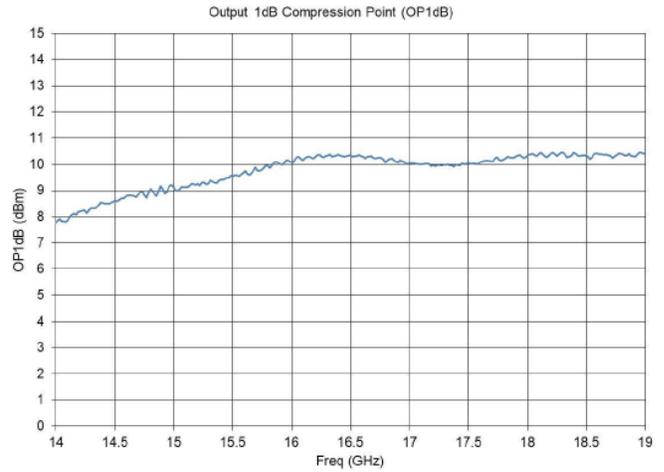
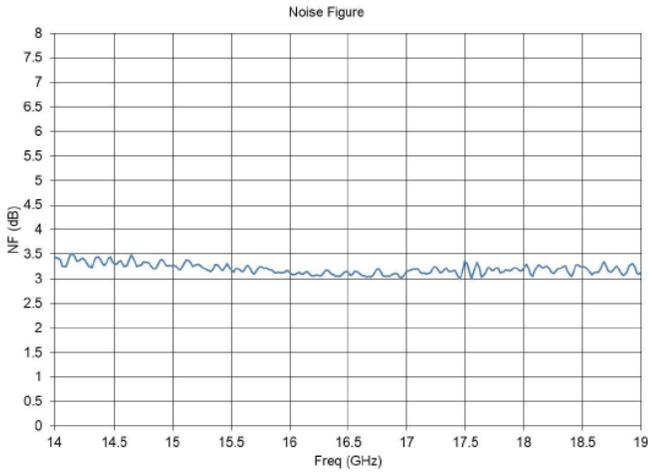
VD_LNA = +3.3 V, SW_V0 = +5 V, SW_V1 = -5 V, SW_V2 = +5 V, RX Idq = 45 mA



Typical Performance - Receive Mode

Noise Figure, OP1dB, OIP3, Terminated Mode Return Loss:

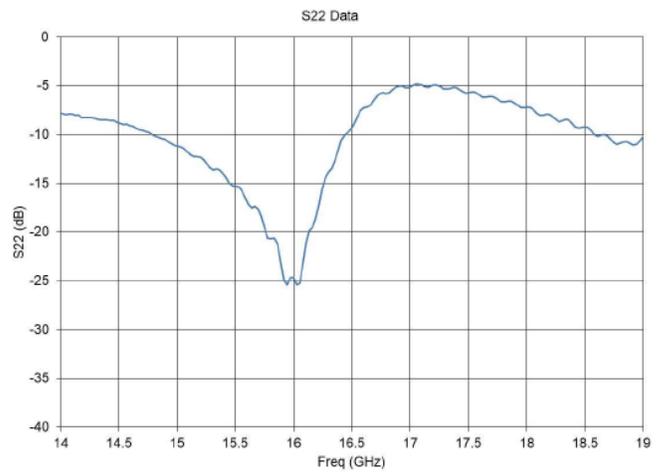
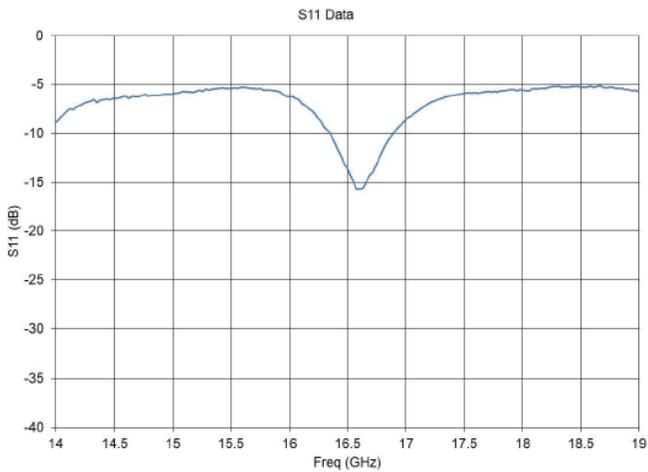
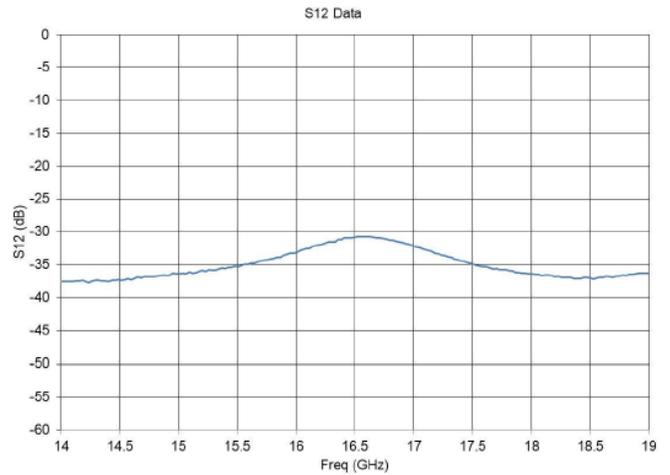
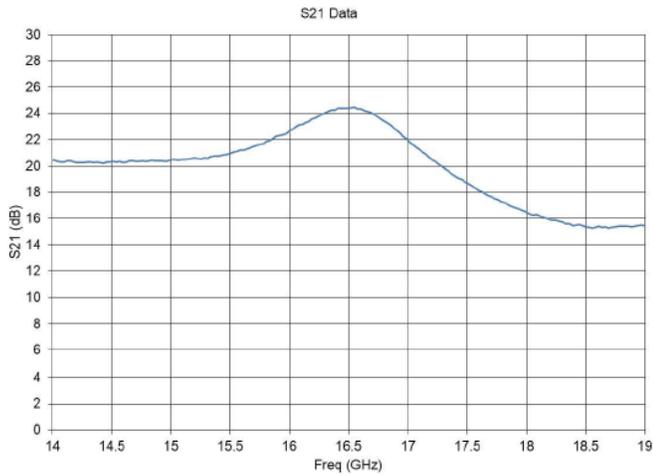
VD_LNA = +3.3 V, SW_V0 = +5 V, SW_V1 = -5 V, SW_V2 = +5 V, RX Idq = 45 mA



Typical Performance - Transmit Mode

Small Signal Gain, Reverse Isolation, Input/Output Return Loss:

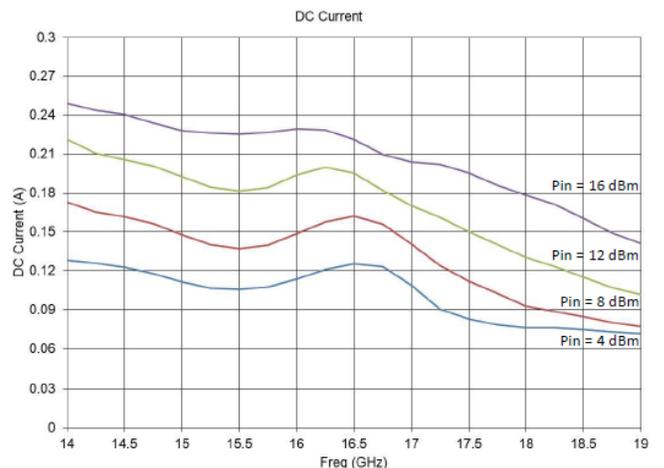
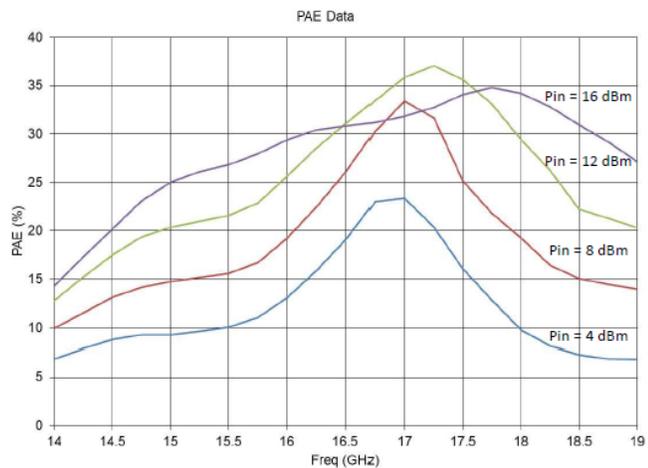
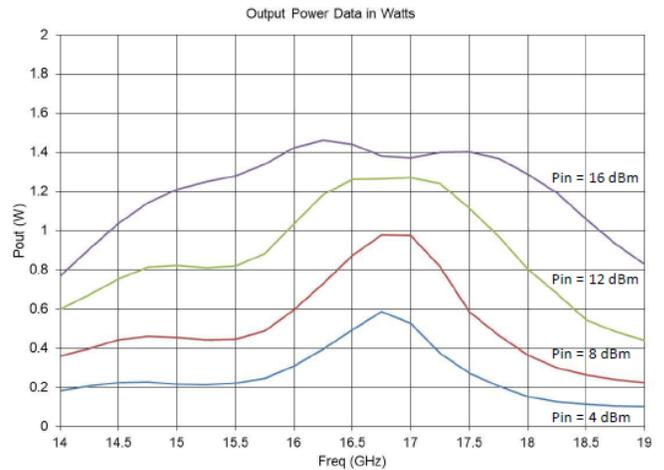
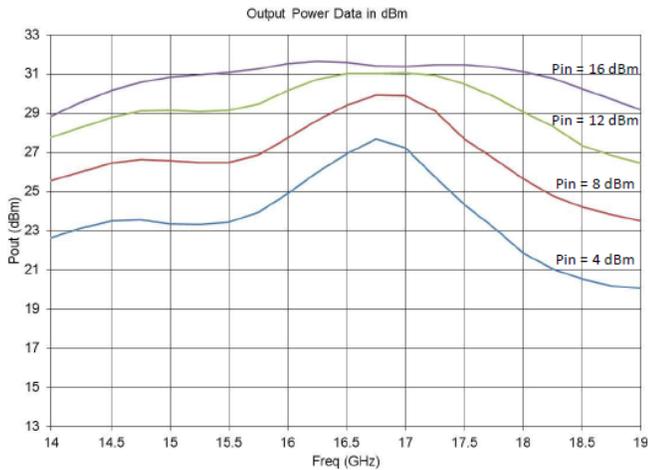
VD1_PA = VD2_PA = +20 V, SW_V0 = -5 V, SW_V1 = +5 V, SW_V2 = +5 V, TX Idq = 100 mA, VG1_PA = VG2_PA = -1.8 V



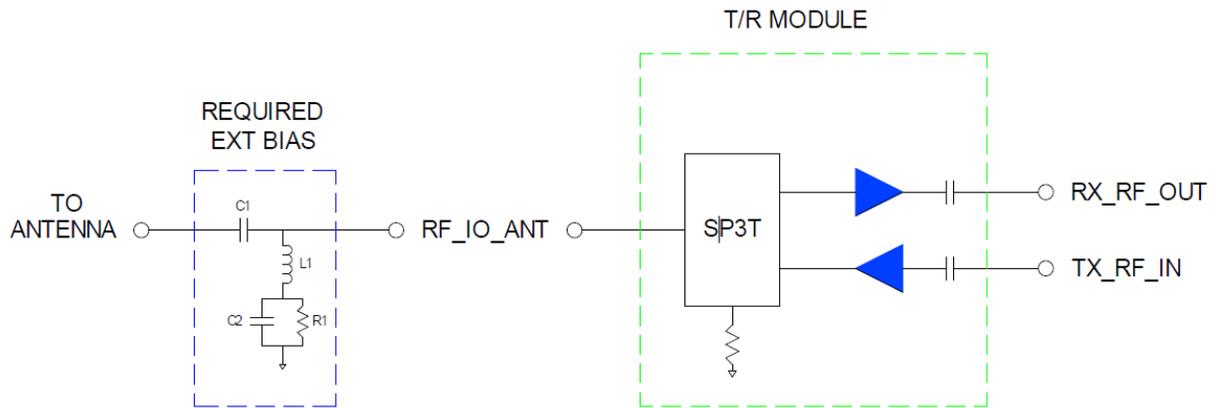
Typical Performance - Transmit Mode

Output Power, PAE, DC Current:

VD1_PA = VD2_PA = +20 V, SW_V0 = -5 V, SW_V1 = +5 V, SW_V2 = +5 V, TX Idq = 100 mA, VG1_PA = VG2_PA = -1.8 V



RF Block Diagram



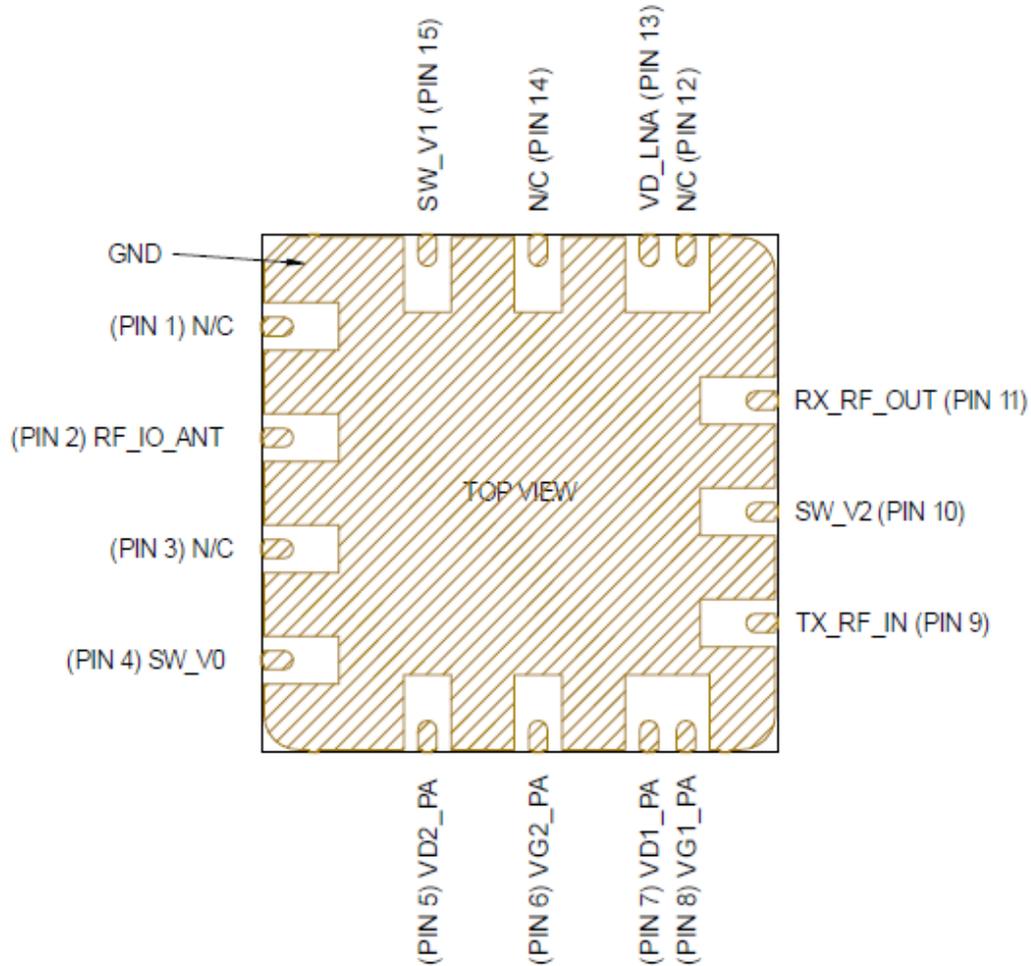
Recommended External Bias Components

Reference Designator	Part Number	Description	Value
C1	02013J1R0ABSTR	Capacitor, 0201	1 pF
C2	GRM033R71H101KA12D	Capacitor, 0201	100 pF
L1	0201DS-2N4XJEW	Inductor, 0201	2.4 nH
R1	ERJ-PA2D2000X	Resistor, 0402	200 ohms

Notes:

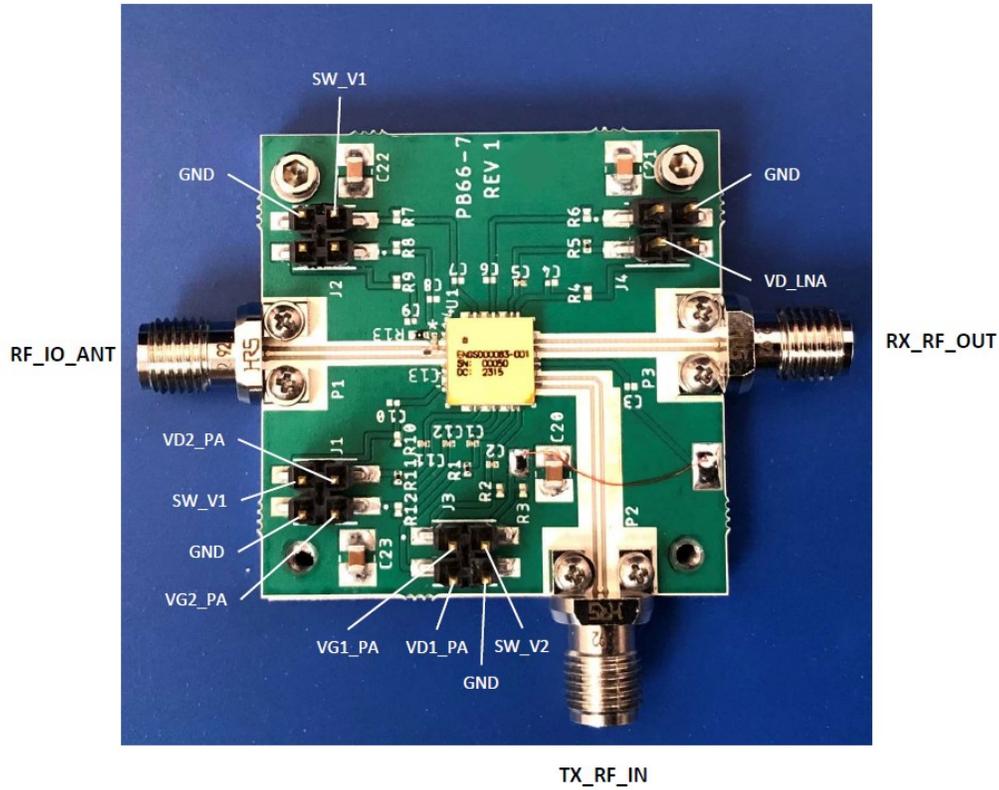
1. Add 4.7 μ F to 10 μ F capacitor to gate and drain lines if power supply capacitors are greater than 4 inches away at the next assembly.

Pinout Configuration



PACKAGE BOTTOM AS SEEN THROUGH THE TOP COVER

Evaluation Board Pinout Configuration



Notes:

1. Connect a 390 ohm resistor from the +5 V supply to SW_V0, SW_V1 or SW_V2 when in the +5 V state.
2. Mount evaluation board to a low thermal resistance heat sink.

T/R Module Biasing Procedure

To prevent inadvertent damage to the T/R module, the following bias procedure is recommended.

RX Mode Bias Up Procedure

1. Set +3.3 V power supply current limit to 0.08 A
2. Set SW_V0 = +5 V, SW_V1 = -5 V, SW_V2 = +5 V (use 390 Ω resistor from +5 V supply to SW_V0 and SW_V2)
3. Apply +3.3 V to VD_LNA
4. Turn on RF signal

RX Mode Bias Down Procedure

1. Turn off RF signal
2. Set VD_LNA to 0 V

TX Mode Bias Up Procedure

1. Set +20 V power supply current limit to 0.35 A
2. Set SW_V0 = -5 V, SW_V1 = +5 V, SW_V2 = +5 V (use 390 Ω resistor from +5 V supply to SW_V1 and SW_V2)
3. Apply -5 V to VG1_PA and VG2_PA
4. Apply +20 V to VD1_PA and VD2_PA
5. Adjust VG1_PA and VG2_PA to set PA Idq = 100 mA
6. Turn on RF signal

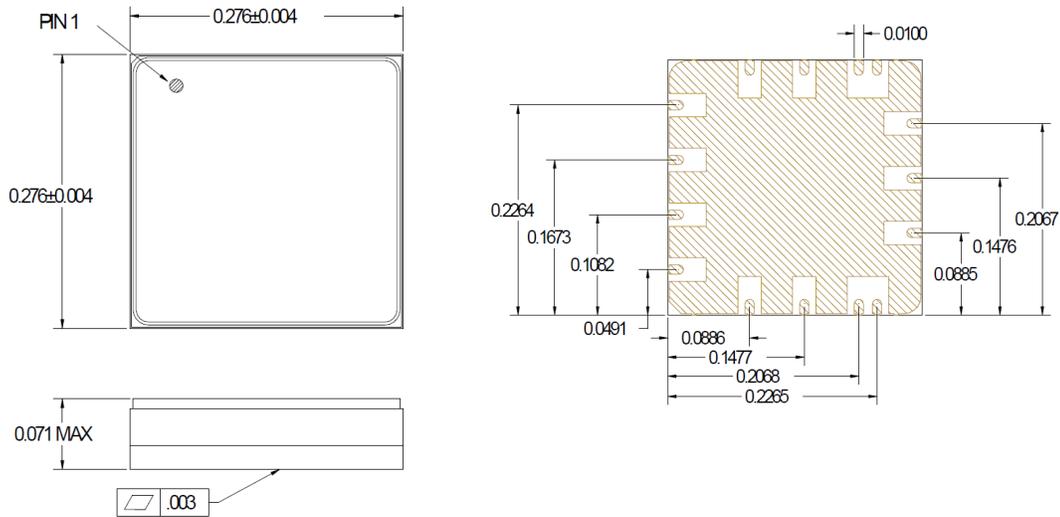
TX Mode Bias Down Procedure

1. Turn off RF signal
2. Set VD1_PA and VD2_PA to 0 V
3. Set VG1_PA and VG2_PA to 0 V

Terminated Mode Bias Procedure

1. Set SW_V0 = +5 V, SW_V1 = +5 V, SW_V2 = -5 V (use 390 Ω resistor from +5 V supply to SW_V0 and SW_V1)

Outline Drawing



Notes (unless otherwise specified):

1. Pads gold plated 40-60 microinches AU PER MIL-G- 45204 TYPE III
2. Do not exceed 280°C processing temperature
3. Final package gross leak hermetic. Optional fine leak hermetic to 1.0×10^{-7} ATM CC/EC AIR if requested
4. Contact factory for recommended board footprint

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