Wideband Low DC Power Low Noise Amplifier, DIE 2 - 18 GHz

ENGLA00182A
Rev. V1

Features

- Multiple Operating Bias Conditions
- Low DC Power:
  40 mW @ V_D = 1.5 V
  132 mW @ V_D = 3.3 V
- Low Noise Figure: 2 dB
- Gain: 15.0 - 17.5 dB
- Good I/O Return Loss: 10 / 15 dB
- Die Size:
  2.72 x 1.65 x 0.1 mm
  0.107 x 0.065 x 0.004 inch
- RoHS* Compliant

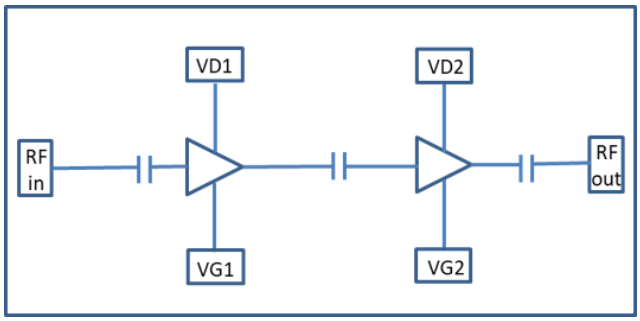
Applications

- Military & Commercial SATCOM
- Obsolescence Replacement
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test & Measurement Systems

Description

The ENGLA00182A is a wideband low DC power low-noise Amplifier (LNA) operating across 2 to 18 GHz with only 40 mA DC current at Vdd = 3.3 V. The amplifier offers 17.5 dB gain, 2 dB de-embedded noise figure, and >18-dBm output third-order intercept point (OIP3) across the band, at room temperature. The design is 50 ohm matched and includes on board bias circuitry. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds to external 50 ohm microstrip lines for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Ordering Information

Part Number	Package
ENGLA00182A	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:

Freq. = 2 - 18 GHz, T_A = +25°C, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	15.0	17.5	18.0
Noise Figure	De-embedded Input Loss	dB	—	2	3
Input Return Loss	—	dB	—	10	—
Output Return Loss	<12 GHz >12 GHz	dB	—	>15 10	—
Output P1dB	—	dBm	—	12	—
Output IP3	—	dBm	18	22	—
Supply Current	—	mA	—	40	—
Thermal Resistance	Channel to MMIC Backside; Backside @ 100°C	ºC/W	—	136	—

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Drain Voltage	1.5	3.3	4.0	V
Gate Voltage	-0.30	-0.17	+1	V
Drain Current	—	40	—	mA

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Drain Voltage	5 V
Gate Voltage	-2.5 V / +1.5 V
RF Input Power	17 dBm
Junction Temperature	+170°C
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

LNA can be operated with single drain voltage in the range of 1.5 V to 4 V

ENGLA00182A is a versatile Wideband Low DC Power LNA that can be operated at various bias conditions with various degrees of RF Performance: Low Noise or Low DC Power and depending on the application requirement appropriate bias condition can be chosen.

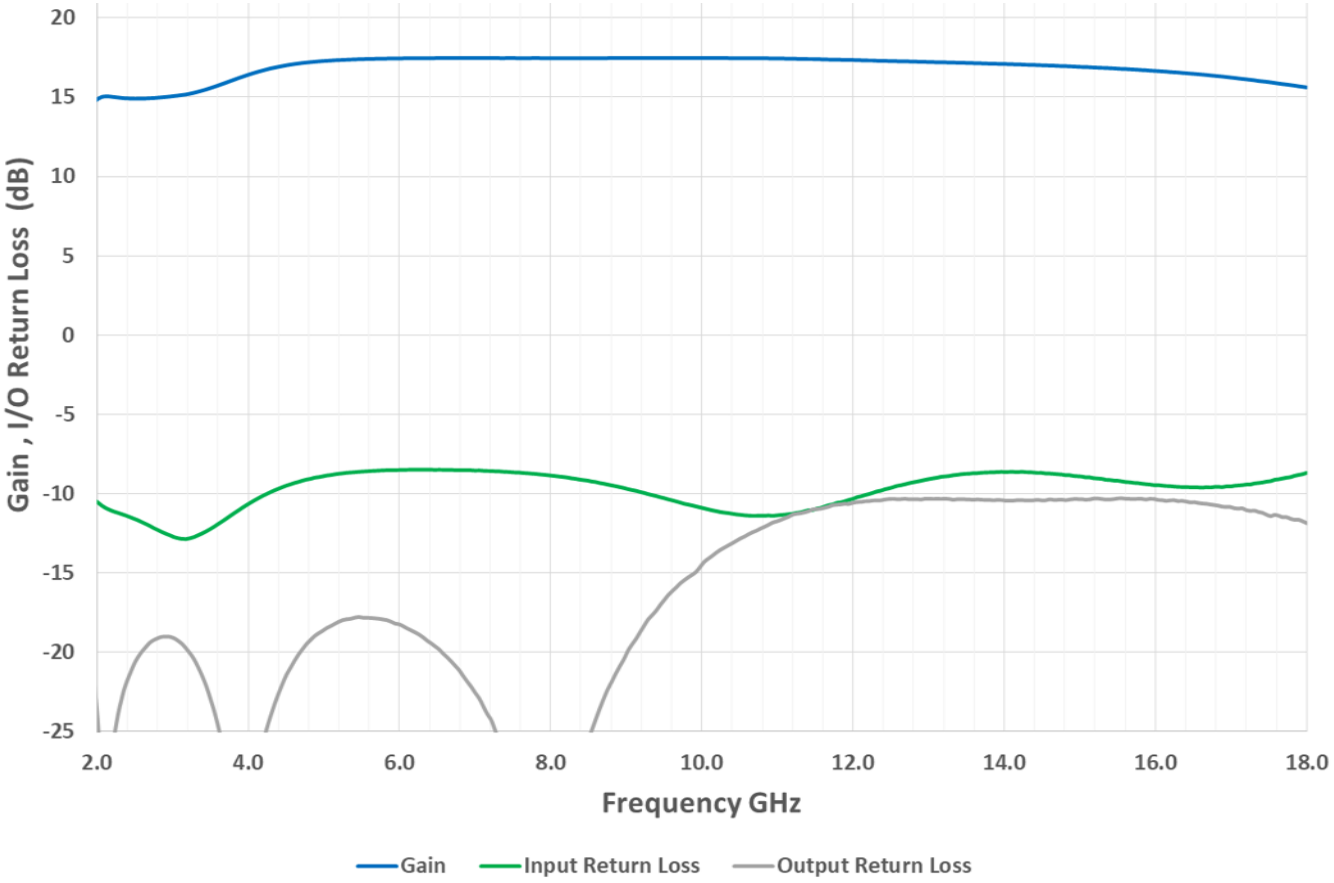
Suitable for Low Power T / R Modules

Following pages show Gain, I/O Return loss, Noise Figure and OIP3 at T = 25 ºC at Vdd = 1.5 V to 4 V

VD1	VG1	VG2	IDD
V	V	V	mA
1.5	0.25	-0.17	27
2	0.5	-0.17	32
3	1.0	-0.17	40
4	1.0	-0.17	41

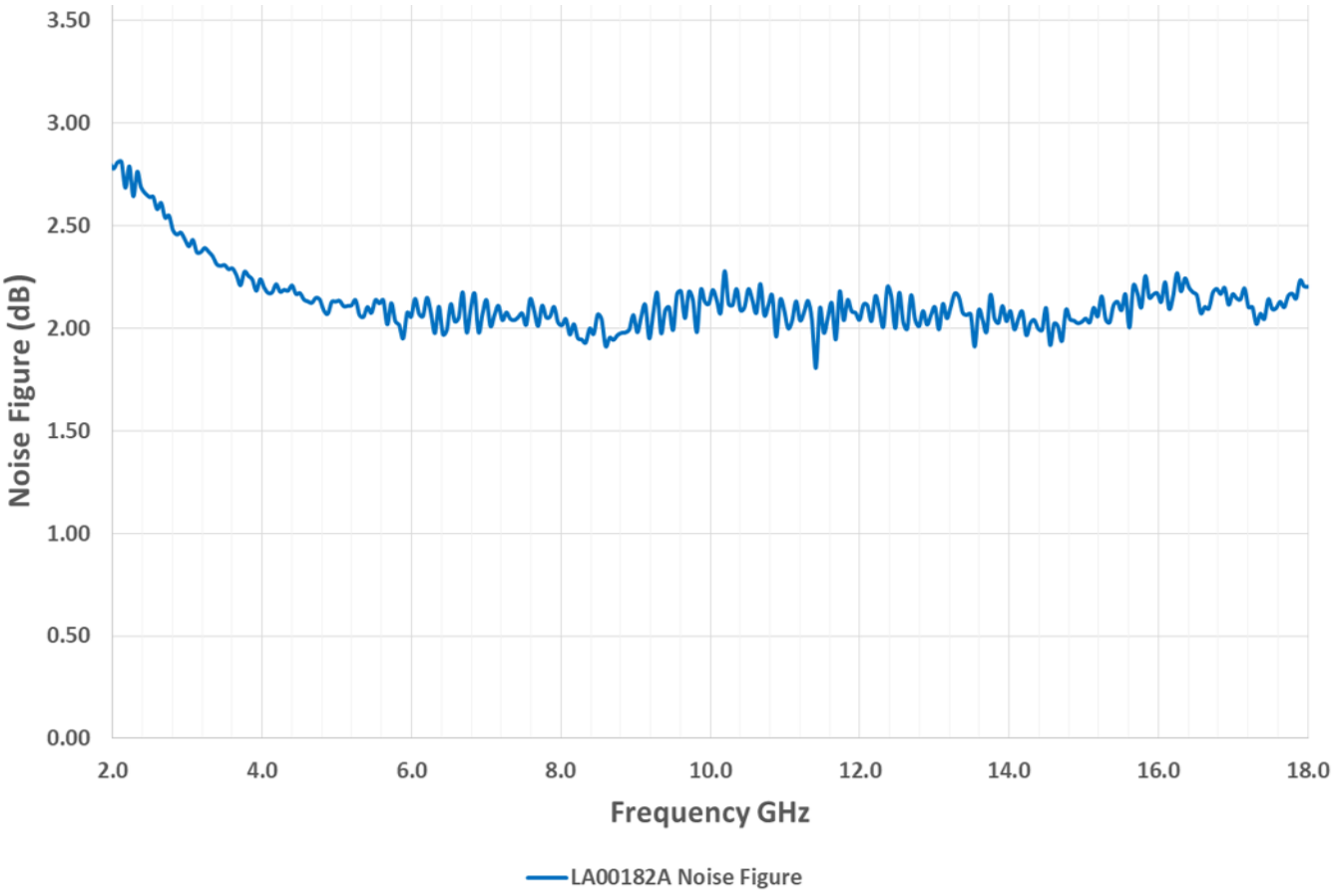
Measured RF Data: With Wirebonds and External Flare Line

Gain and In / Out Return Loss: T = 25 ºC, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA



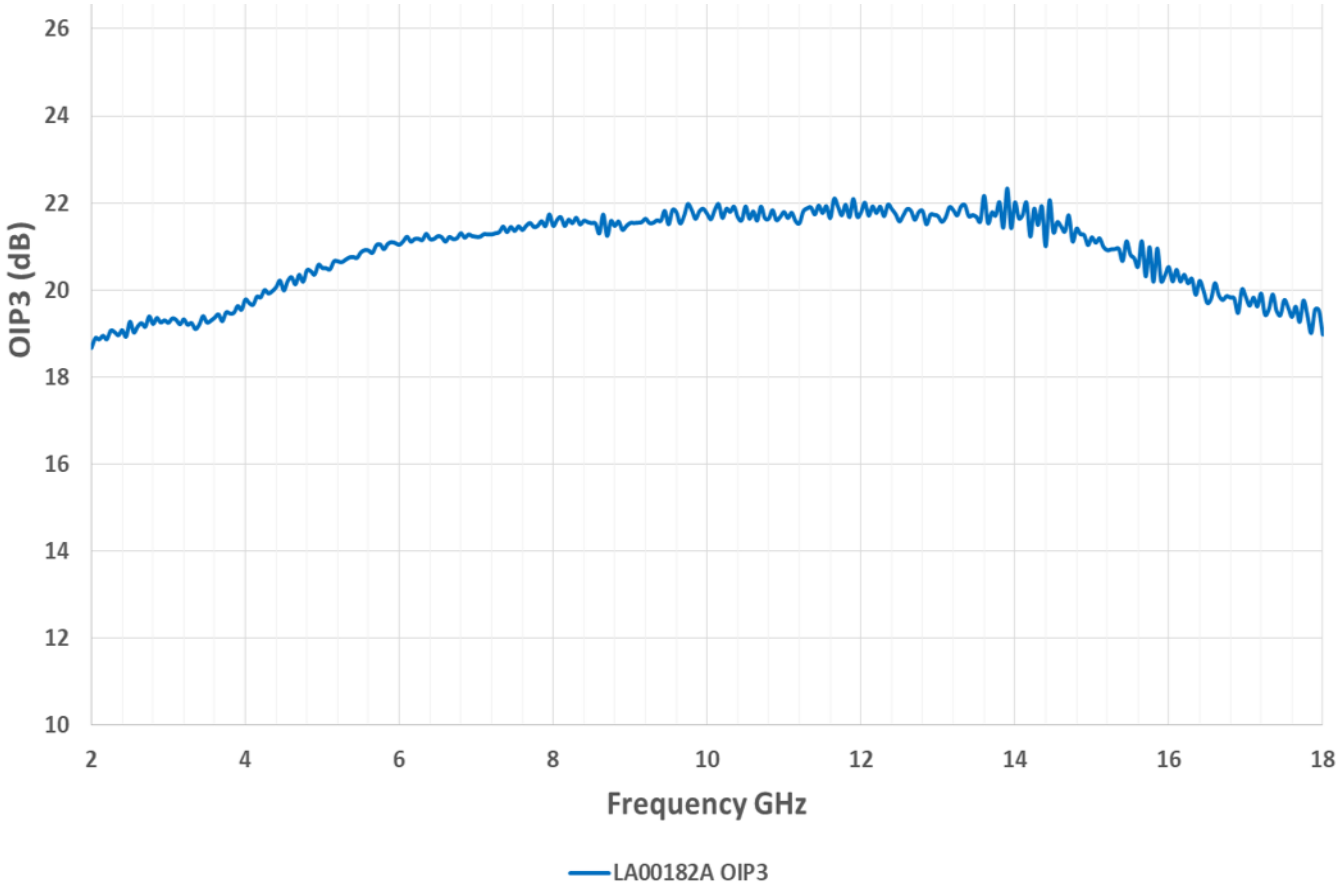
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Noise Figure: T = 25 ºC, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA (De-embedded Input Loss)



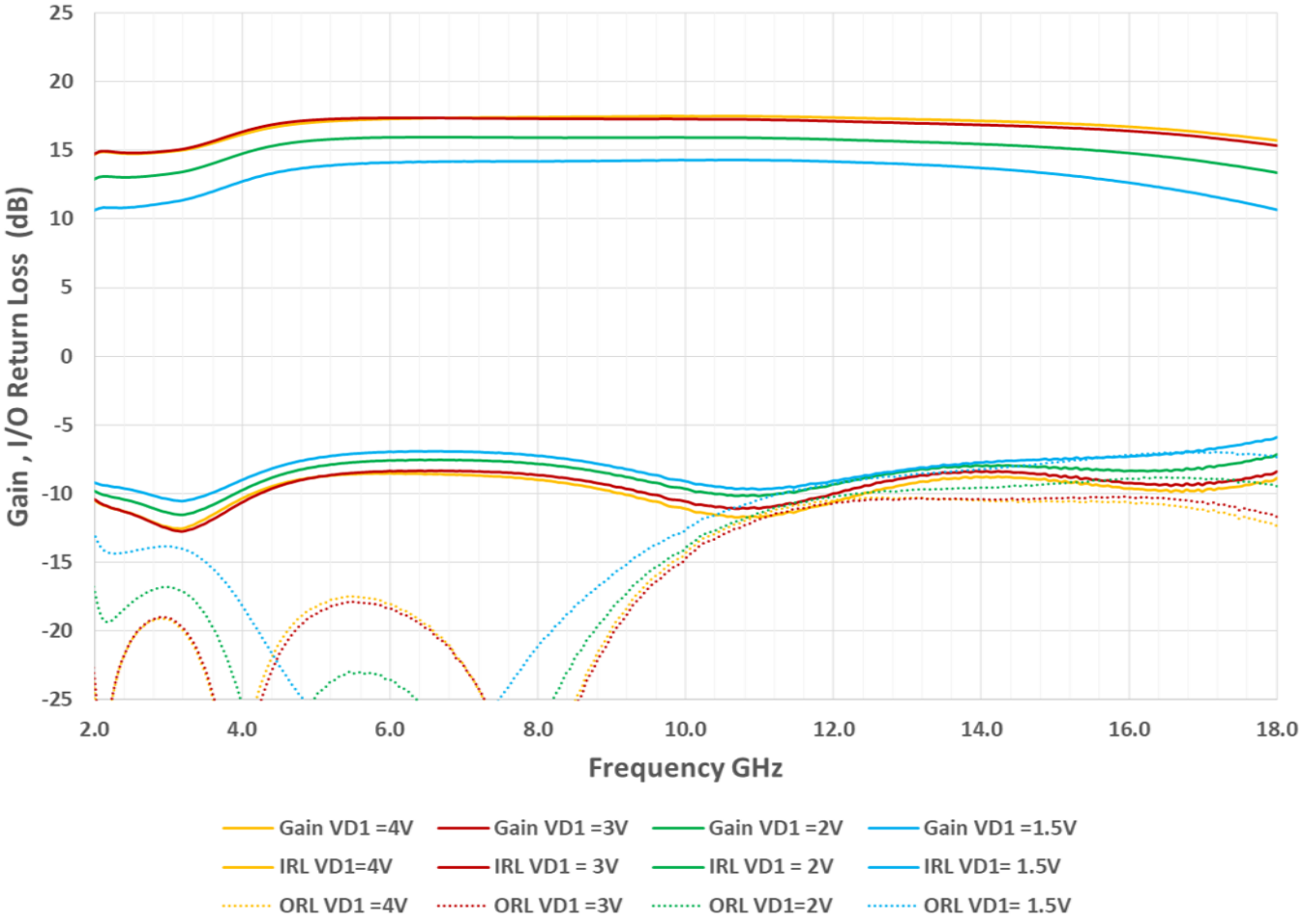
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Output Third-Order Intercept: T = 25 ºC, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA
RF input tone levels: -25 dBm per tone ; tone spacing: 100 MHz



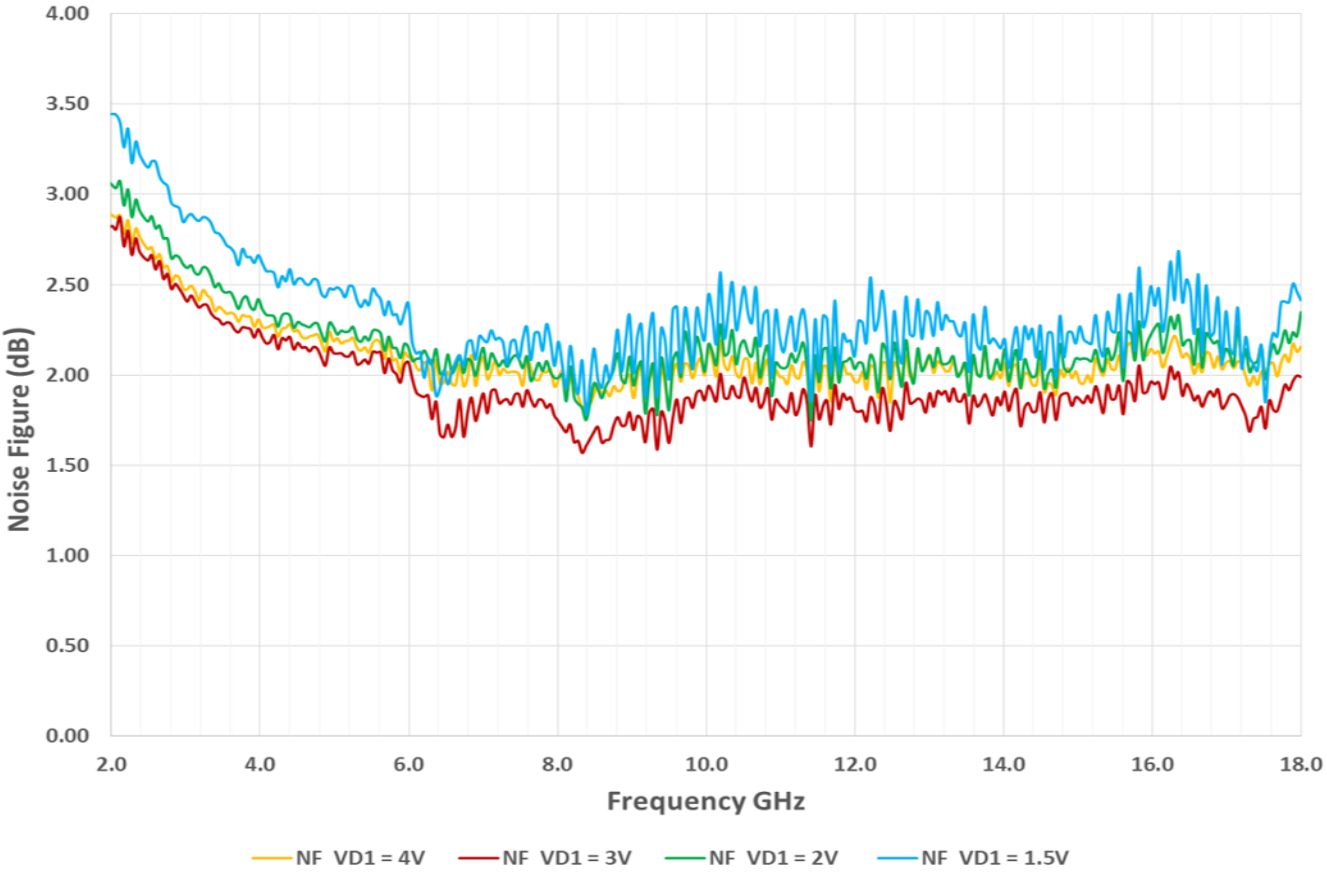
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Gain and In / Out Return Loss: Vdd = 1.5 V to 4 V



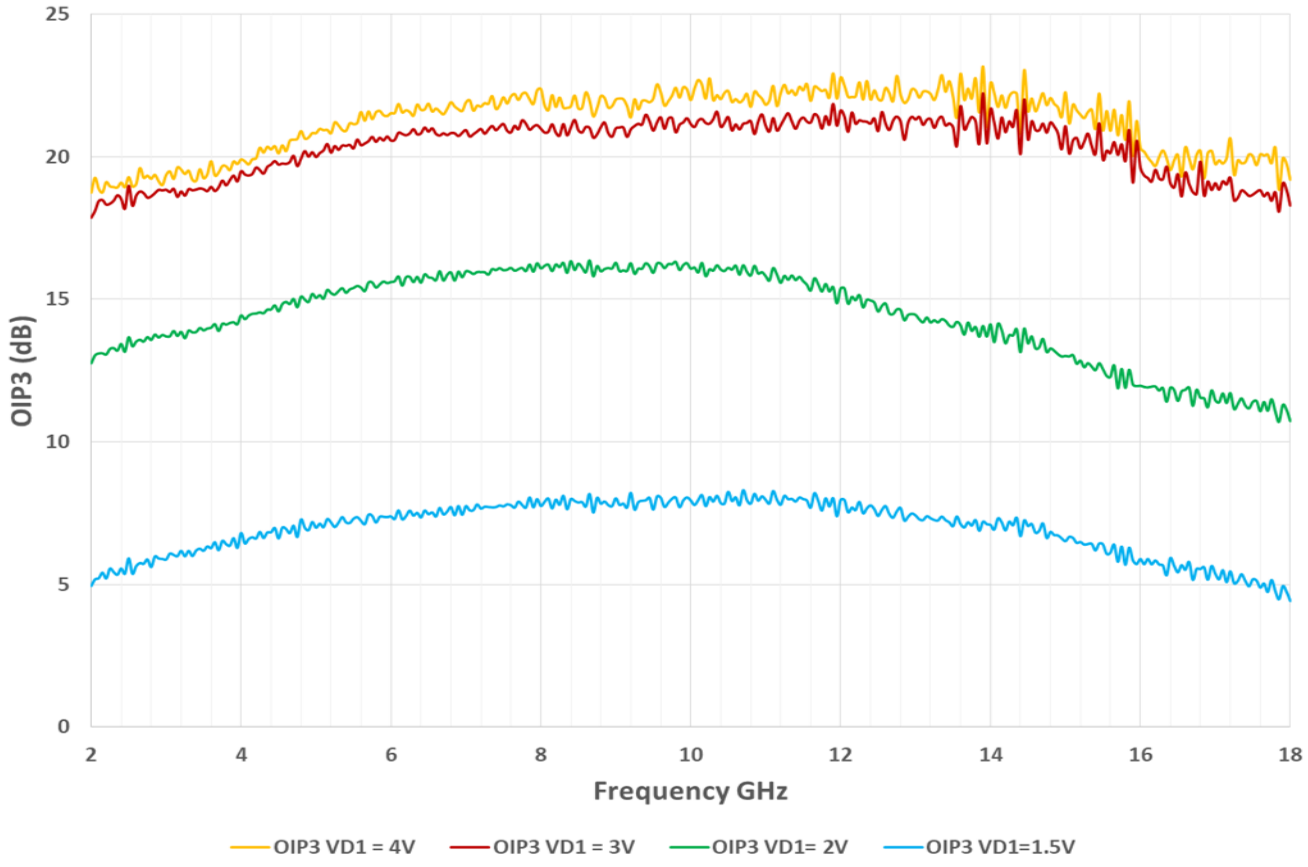
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Noise Figure (De-embedded Input Loss): Vdd = 1.5 V to 4 V



Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

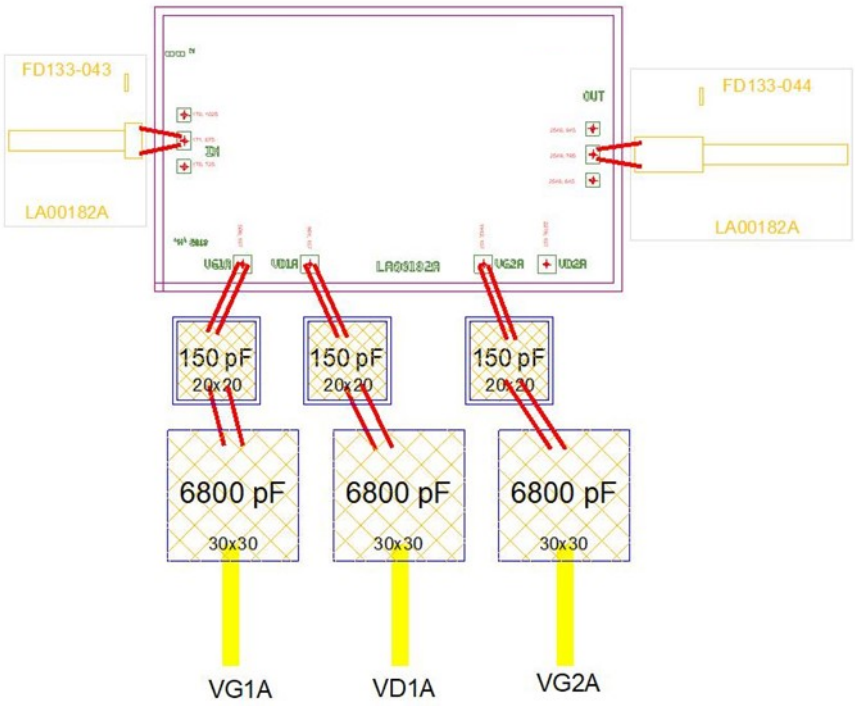
Third-Order Intercept Point: Vdd = 1.5 V to 4 V
RF input tone levels: -25 dBm per tone; tone spacing: 100 MHz



External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

Pad Flare Dimension	Flare Length x-dim, (µm)	Flare Width y-dim, (µm)	Wire Inductance (nH)	Wire Length (µm)	Wire Length (mils)	# of Wires
RF Input	100	200	0.115	230	9	2
RF Output	394	204	0.115	230	9	2



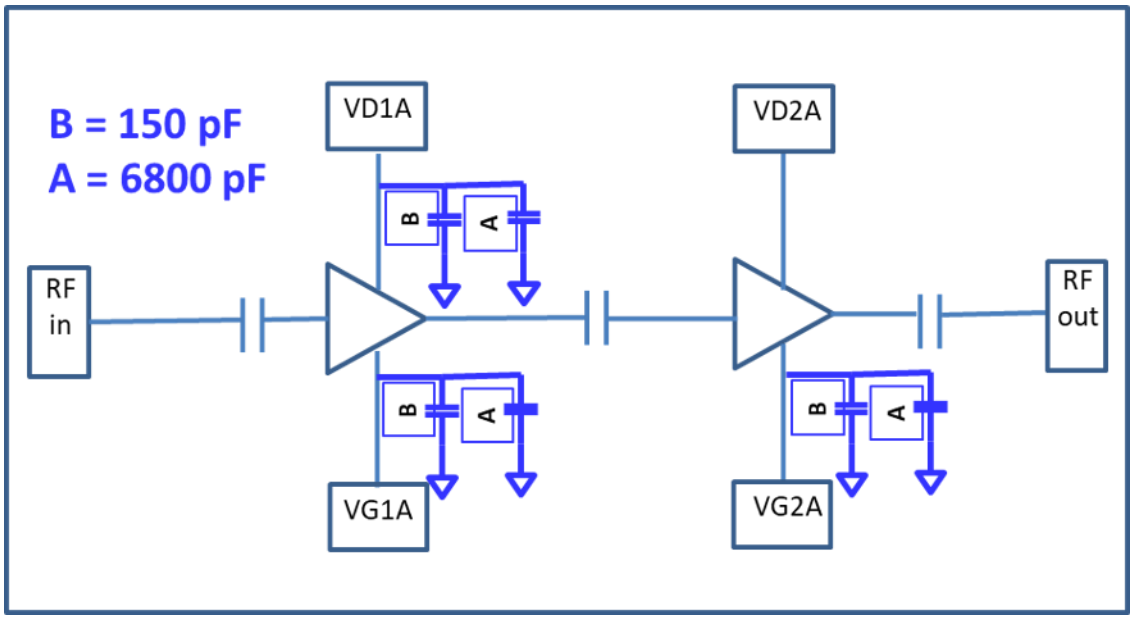
Notes:

1. To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.
2. Gold Wire Details:
   Diameter: 25.4 µm (1 mil)
   Spacing: 4 mils (~ 100 µm) typical
   Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)
3. Wire Length is total length if the wire were made perfectly straight.

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



VD2A Do Not Connect

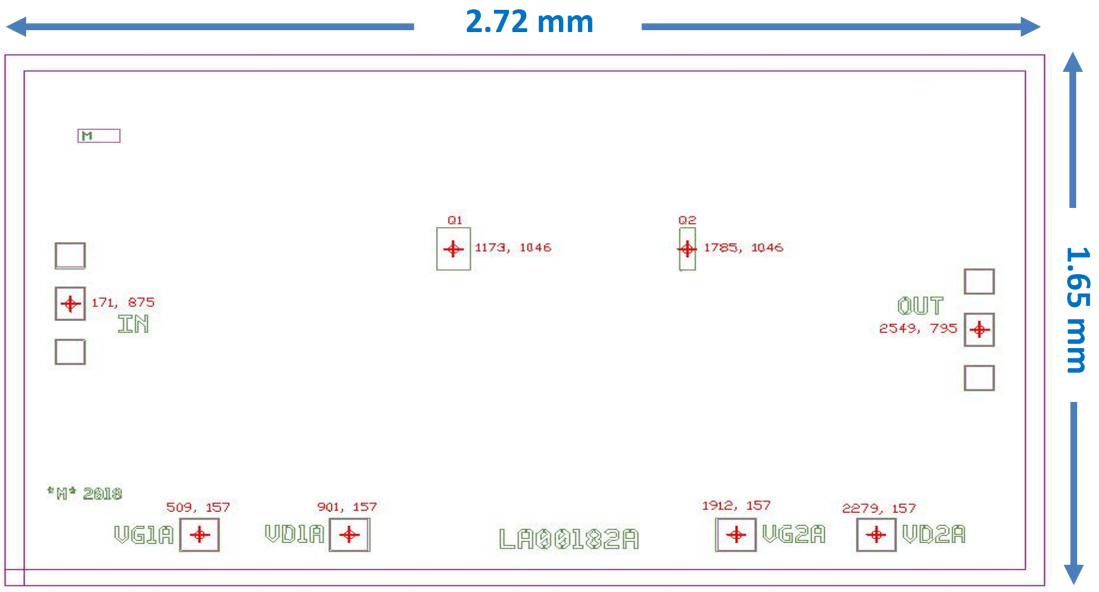
Bias Up Sequence:

1. Set Idd limit to 50mA
2. Set Gate Voltage (VG) = -2.0 V
3. Set Drain Voltage (VD) = 3.3 V
4. Adjust VG2 more positive until target current , then adjust VG1 specified in page 2
5. Turn ON RF Signal

Bias Down Sequence:

1. Turn OFF RF Signal
2. Reduce VG to -2.0 V , Idd should be 0 mA
3. Reduce VD to 0 V
4. Turn OFF DC Supplies

Outline Drawing



Pad Dimensions

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
IN	RF input (port 1)	171	875	6.7	34.4
VG1A	VG1 stage 1 gate bias	509	157	20.0	6.2
VD1A	VD1 stage 1 drain bias	901	157	35.5	6.2
VG2A	VG2 stage 2 gate bias	1912	157	75.3	6.2
VD2A	VD2 No Connect	2279	157	89.7	6.2
OUT	RF output (port 2)	2549	795	100.4	31.3

Notes:
All dimensions are given in both µm and mils.
Substrate thickness: 100 µm (0.004”).
Backside metallization is gold.
Bond pad metallization is gold.