

CMPA601C025D

6 - 12 GHz, 40 W GaN HPA

Description

The CMPA601C025D is a 40 W MMIC HPA utilizing the high performance, 0.25 um GaN on SiC production process. The CMPA601C025D operates from 6 - 12 GHz and supports both defense and commercial-related radar and electronic warfare applications. The CMPA601C025D achieves 40 W of saturated output power with 25 dB of large signal gain and typically 30% power-added efficiency under CW operation.

The CMPA601C025D provides superior, broadband performance allowing customers to improve SWaP-C benchmarks in their next-generation systems.



Figure 1. CMPA601C025D

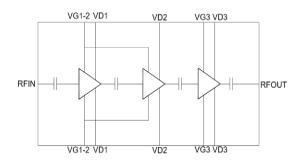


Figure 2. Functional Block Diagram

Features

- P_{SAT}: 40 W
- PAE: 30%
- LSG: 25 dB
- S21: 37 dB
- S11: <-5 dBS22: <-5 dB
- CW operation

Applications

- Military and commercial radar
- Electronic warfare
- Test instrumentation
- General broadband amplifiers

Note:

Features are typical performance across frequency under 25 °C operation. Please reference performance charts for additional information.





Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain Voltage	V _D	V	28	
Gate Voltage	V_{G}	V	-10, +2	
Drain Current	I _D	A	7.1	
Gate Current	I _G	mA	15	
Input Power	P _{IN}	dBm	26	CW
Dissipated Power	P _{DISS}	W	120	85 °C
Storage Temperature	T _{STG}	°C	-65, +150	
Mounting Temperature	T _J	°C	260	30 Seconds
Junction Temperature	T _J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	5:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	V _D	V	28	
Gate Voltage	V _G	V	-2.8	
Drain Current	l _{DQ}	A	2	
Input Power	P _{IN}	dBm	22	
Case Temperature	T _{CASE}	°C	-40 to 85	

RF Specifications¹

Test conditions unless otherwise noted: $V_D = 28 \text{ V}$, $I_{DO} = 2400 \text{ mA}$, PW = 10 us, DC = 0.1%, $T_{BASE} = 25 ^{\circ}\text{C}$

Parameter	Units	Frequency	Min.	Typical	Max.	Conditions
Frequency	GHz		6		12	
		6	45.5	47		
Output Power	dBm	10	45.5	47		$P_{IN} = 19 \text{ dBm}$
		12	45.5	47		
		6	23	30		
Power-Added Efficiency	%	10	23.3	32		$P_{IN} = 19 \text{ dBm}$
		12	23.7	31		
		6		28		
LSG	dB	10		28		$P_{IN} = 19 \text{ dBm}$
		12		28		
		6	29.8	35		
Small-Signal Gain (S21)	dB	10	30.2	35		$P_{IN} = 10 \text{ dBm}$
		12	27.8	35		
Input Return Loss	dB			-10		
Output Return Loss	dB			-8		

Note:

¹Above RF specifications are screened at on-wafer probe under short pulse operation. Subsequent data plots in this document represent fixture performance under CW operation as noted.



Large Signal Performance versus Temperature

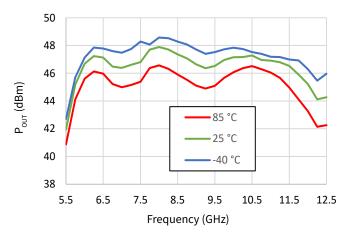


Figure 3. P_{OUT} v. Frequency v. Temperature

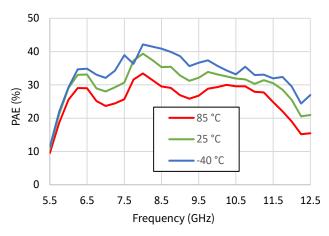


Figure 4. PAE v. Frequency v. Temperature

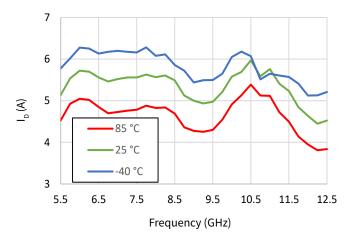


Figure 5. I_D v. Frequency v. Temperature

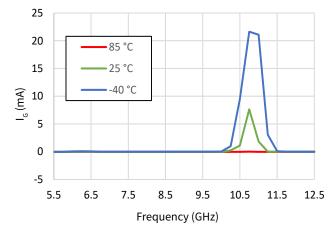


Figure 6. I_G v. Frequency v. Temperature

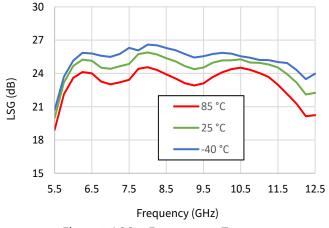


Figure 7. LSG v. Frequency v. Temperature



Large Signal Performance versus V_D

Test conditions unless otherwise noted: $V_D = 28 \text{ V}$, $I_{DQ} = 2000 \text{ mA}$, CW, $P_{IN} = 22 \text{ dBm}$, $T_{BASE} = 25 \, ^{\circ}\text{C}$, frequency = 9.5 GHz

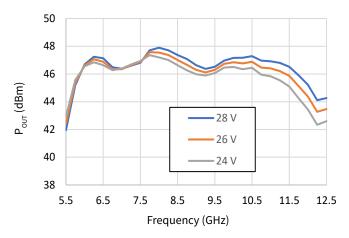
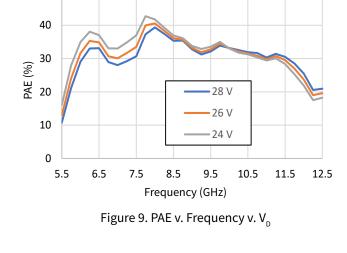


Figure 8. P_{OUT} v. Frequency v. V_{D}



50

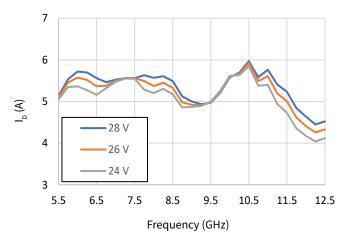


Figure 10. I_D v. Frequency v. V_D

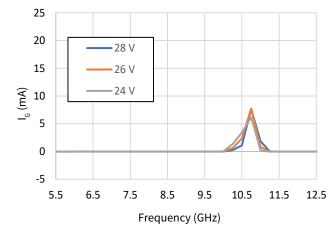


Figure 11. I_G v. Frequency v. V_D

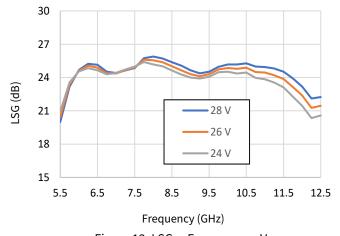


Figure 12. LSG v. Frequency v. V_D



Large Signal Performance versus I_{pq}

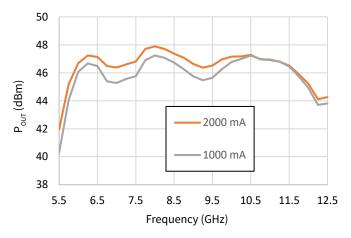


Figure 13. P_{OUT} v. Frequency v. I_{DO}

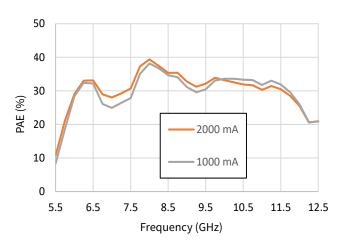


Figure 14. PAE v. Frequency v. I

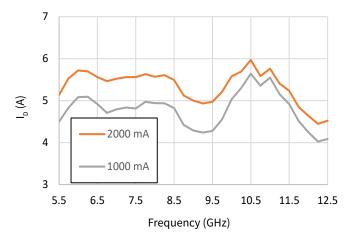


Figure 15. I_D v. Frequency v. I_{DO}

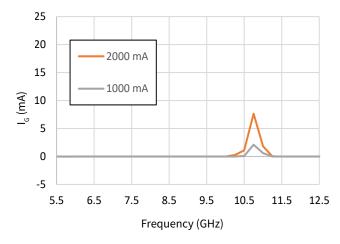


Figure 16. I_G v. Frequency v. I_{DO}

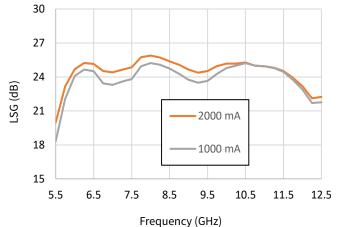


Figure 17. LSG v. Frequency v. I_{DO}



Drive-Up versus Frequency

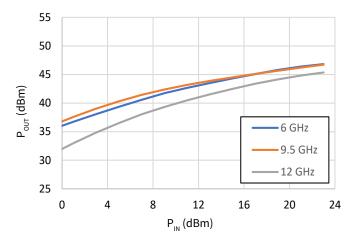


Figure 18. P_{OUT} v. P_{IN} v. Frequency

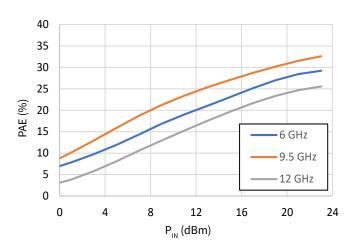


Figure 19. PAE v. P_{IN} v. Frequency

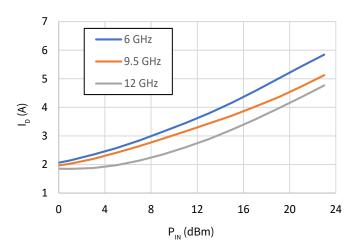


Figure 20. I_D v. P_{IN} v. Frequency

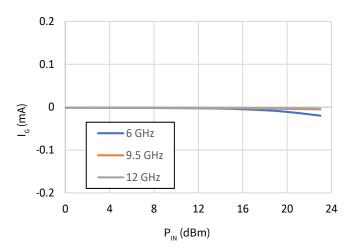


Figure 21. I_G v. P_{IN} v. Frequency

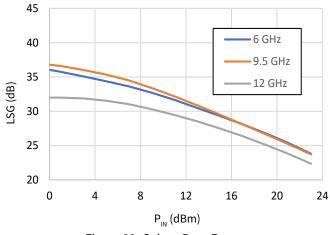


Figure 22. Gain v. P_{IN} v. Frequency



Drive-Up versus Temperature

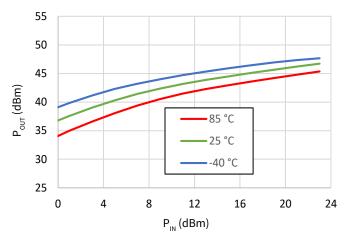


Figure 23. P_{OUT} v. P_{IN} v. Temperature

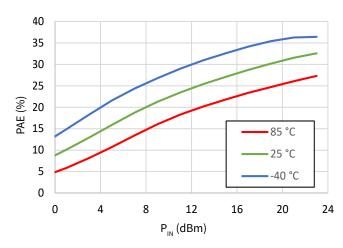


Figure 24. PAE v. P_{IN} v. Temperature

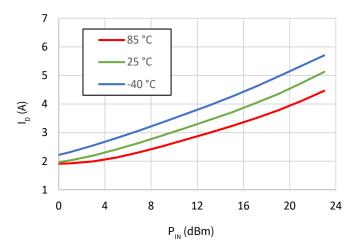


Figure 25. I_D v. P_{IN} v. Temperature

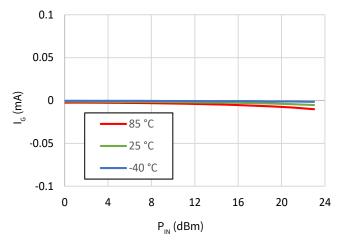


Figure 26. I_G v. P_{IN} v. Temperature

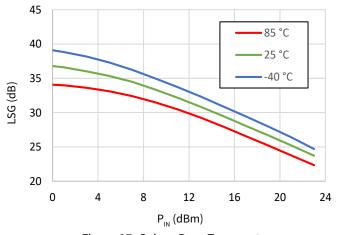


Figure 27. Gain v. P_{IN} v. Temperature

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Drive-Up versus V_D

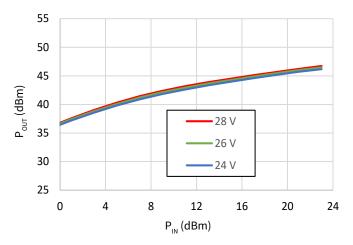


Figure 28. P_{OUT} v. P_{IN} v. V_{D}

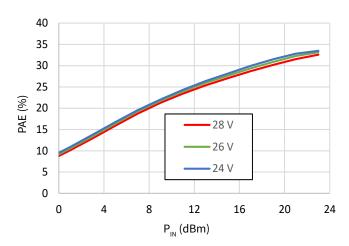


Figure 29. PAE v. P_{IN} v. V_{D}

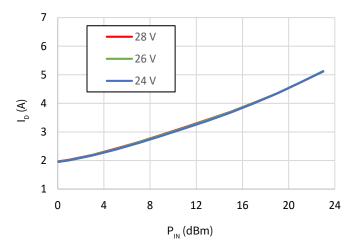


Figure 30. I_D v. P_{IN} v. V_D

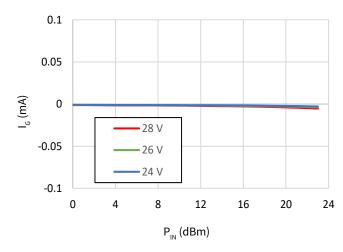


Figure 31. I_G v. P_{IN} v. V_D

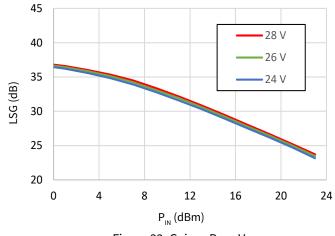


Figure 32. Gain v. P_{IN} v. V_D



Drive-Up versus I_{DQ}

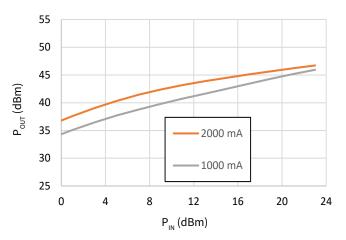


Figure 33. P_{OUT} v. P_{IN} v. I_{DO}

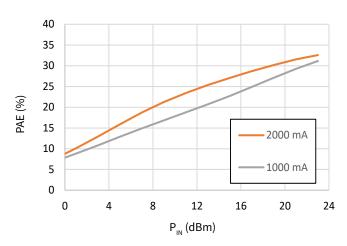


Figure 34. PAE v. P_{IN} v. I_{DO}

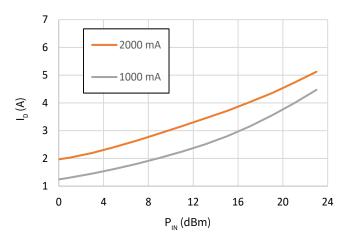


Figure 35. I_D v. P_{IN} v. I_{DQ}

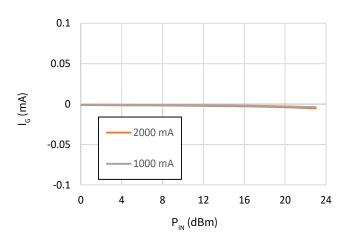


Figure 36. I_G v. P_{IN} v. I_{DO}

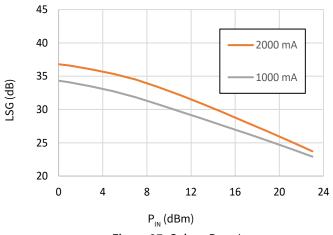


Figure 37. Gain v. P_{IN} v. I_{DQ}



Small Signal v. Temperature and V_D

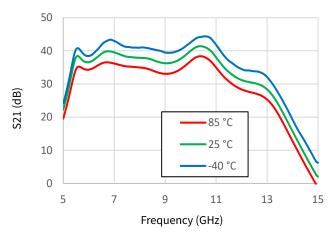


Figure 38. S21 v. Frequency v. Temperature

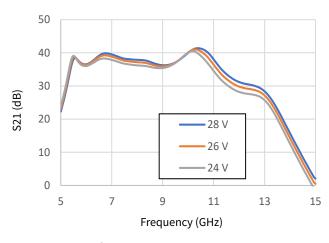


Figure 39. S21 v. Frequency v. V_D

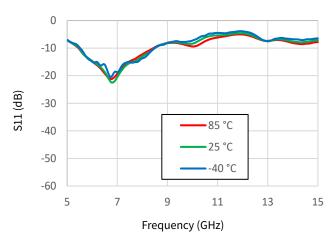


Figure 40. S11 v. Frequency v. Temperature

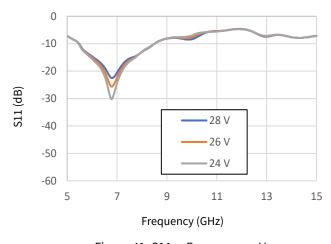


Figure 41. S11 v. Frequency v. V_D

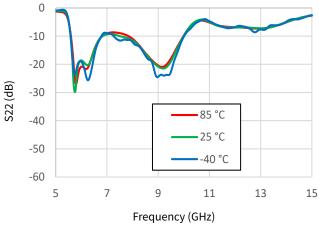


Figure 42. S22 v. Frequency v. Temperature

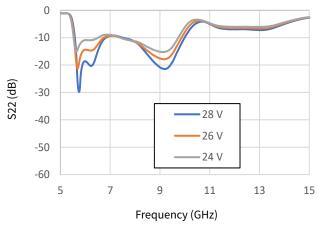


Figure 43. S22 v. Frequency v. V_D



Small Signal v. I_{DQ}

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 2000 mA, P_{IN} = -30 dBm, T_{BASE} = 25 °C

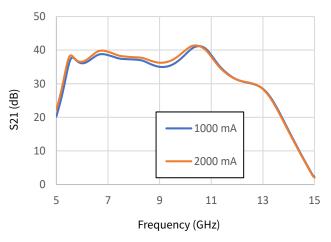


Figure 44. S21 v. Frequency v. I_{DO}

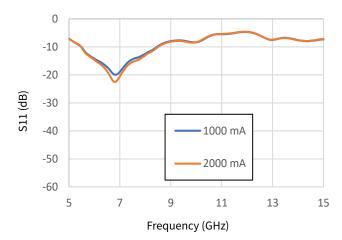


Figure 45. S11 v. Frequency v. I_{DO}

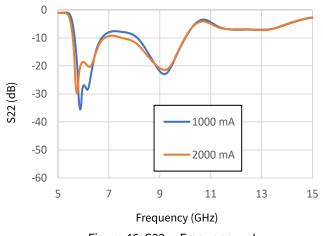


Figure 46. S22 v. Frequency v. I_{DQ}

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Harmonics

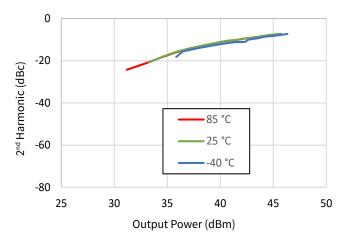


Figure 47. 2f v. P_{OUT} v. Temperature, 6 GHz

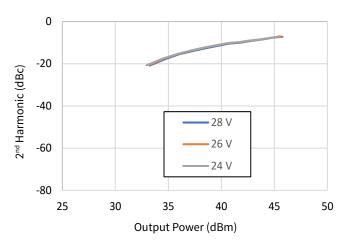


Figure 48. 2f v. P_{OUT} v. V_{D} , 6 GHz

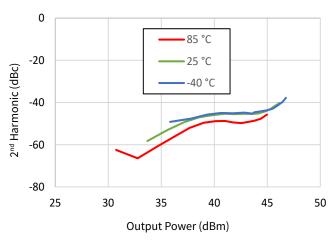


Figure 49. 2f v. P_{OUT} v. Temperature, 9.5 GHz

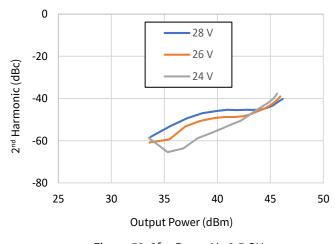
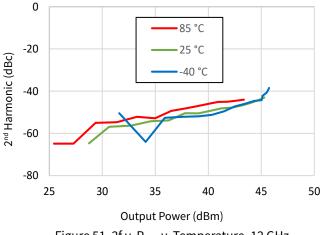
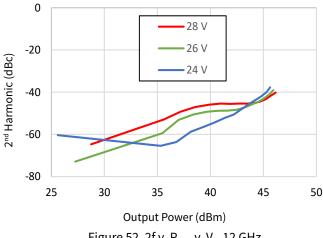


Figure 50. 2f v. P_{OUT} v. V_{D} , 9.5 GHz





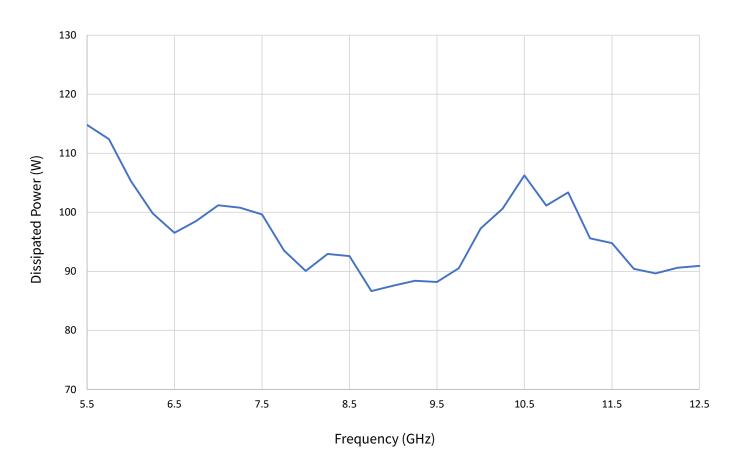


Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T _J	116.5 °C	Freq = 9 GHz, $V_D = 28 \text{ V}$, $I_{DO} = 2 \text{ A}$, $I_{DRIVE} = 4.28 \text{ A}$, $P_{IN} = 22 \text{ dBm}$,
Thermal Resistance, Junction to Back of Die	R _{euc}	0.36 °C/W	$P_{OUT} = 45.1 \text{ dBm}, P_{DISS} = 87.6 \text{ W}, T_{BASE} = 85 \text{ °C}, CW$

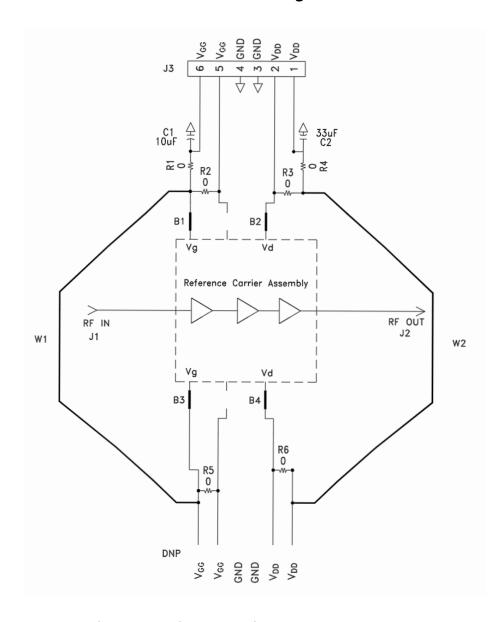
Power Dissipation vs Frequency (T_{CASE} = 85 °C)

Dissipated Power vs Frequency





CMPA601C025D-AMP Evaluation Board Schematic Drawing

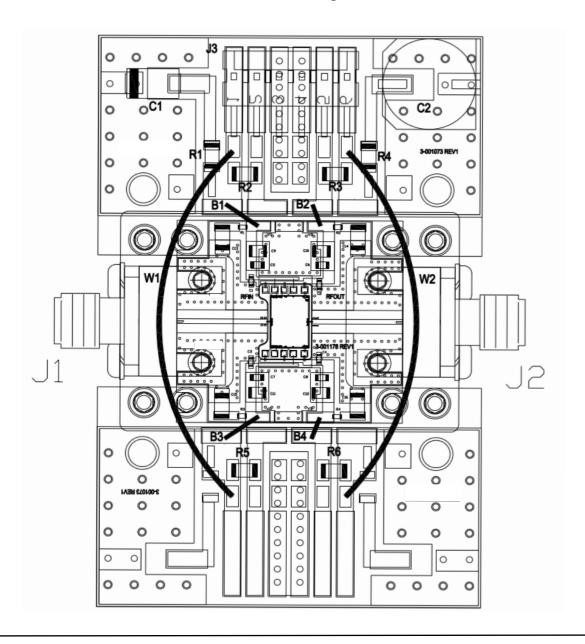


CMPA601C025D-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
J1, J2	CONNECTOR SMA JACK (FEMALE) END LAUNCH	2
J3	6-PIN DC HEADER, RIGHT ANGLE	1
R1 - R6	RESISTOR, 0 OHMS, 1206	6
C1	CAPACITOR, 10 UF, TANTALUM	1
C2	CAPACITOR, 33 UF, ELECTROLYTIC	1
B1 - B4	JUMPER WIRE	4
W1 - W2	WIRE, BLACK, 22 AWG (~2")	2



CMPA601C025D-AMP Evaluation Board Assembly Drawing



Bias On Sequence

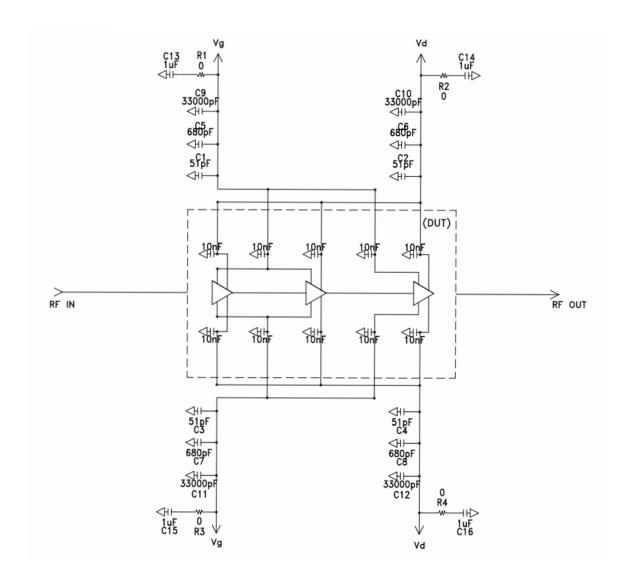
- Ensure RF is turned-off
- Apply pinch-off voltage of -5 V to the gate (V_c)
- Apply nominal drain voltage (V_D)
- Adjust V₆ to obtain desired quiescent drain current (I_{DO})
- Apply RF

Bias Off Sequence

- Turn RF off
- Apply pinch-off to the gate ($V_g = -5 \text{ V}$) Turn off drain voltage (V_D)
- Turn off gate voltage (V_G)



CMPA601C025D-AMP Carrier Schematic Drawing

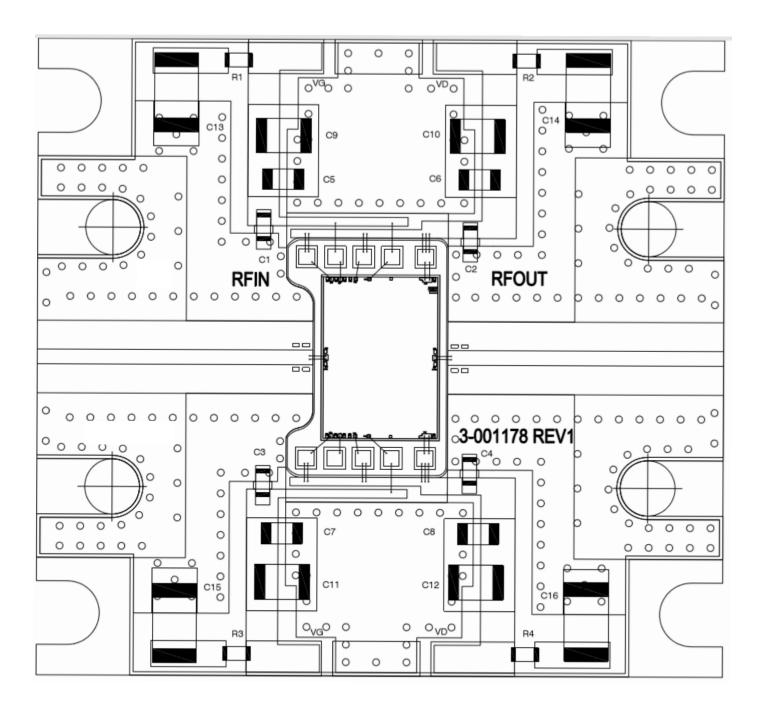


CMPA601C025D-AMP Carrier Bill of Materials

Reference Designator	Description	Qty
C1 - C4	CAPACITOR, 51 pF, 5%, 0402, AVX	4
C5 - C8	CAPACITOR, 680 pF, 5%, 0603, Vishay	4
C9 - C12	CAPACITOR, 33000 pF, 0805, 100 V, X7R	4
C13 - C16	CAPACITOR, 1 uF, +/-15%, 100 V, 1206, X7R	4
R1 - R4	RESISTOR, 0402, 0 OHMS	4

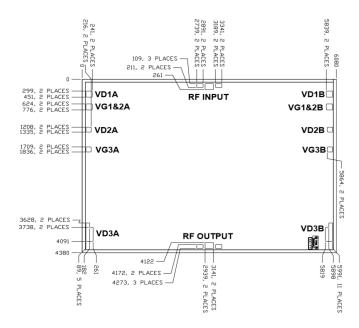


CMPA601C025D-AMP Carrier Assembly Drawing





Product Dimensions (Units in microns)



Overall Die Size 4380 x 6080 (+0/-50) microns, Die Thickness 100 (+/-10) microns. All Gate and Drain Pads Must be Wire Bonded for Electrical Connection.

Function	Description	Pad Size (um)	Note
RF IN	RF-Input Pad. Matched to 50 ohms. The DC Impedance ~ 0 ohm Due Matching Circuit	152 x 202	4
VD1_A	Drain Supply for Stage 1A. V _D = 28 V	152 x 152	1
VD1_B	Drain Supply for Stage 1B. V _D = 28 V	152 x 152	1
VG1 & 2_A	Gate Control for Stage 1 & 2A. V _G = -2.0 to -3.5 V	152 x 152	1, 2
VG1 & 2_B	Gate Control for Stage 1 & 2B. V _G = -2.0 to -3.5 V	152 x 152	1, 2
VD2_A	Drain Supply for Stage 2A. V _D = 28 V	127 x 127	1
VD2_B	Drain Supply for Stage 2B. V _D = 28 V	127 x 127	1
VG3_A	Gate Control for Stage 3A. V _G = -2.0 to -3.5 V	127 x 127	1, 3
VG3_B	Gate Control for Stage 3B. V _G = -2.0 to -3.5 V	127 x 127	1, 3
VD3_A	Drain Supply for Stage 3A. V _D = 28 V	-	1
VD3_B	Drain Supply for Stage 3B. V _D = 28 V	-	1
RF OUT	RF Output Pad. Matched to 50 ohms	152 x 202	4

Notes:

Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Test Methodology
Human Body Model	НВМ	TBD	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	JEDEC JESD22 C101-C

 $^{^{\}mbox{\tiny 1}}$ Attach by pass capacitor to pads per application circuit.

 $^{^2}$ VG1 & 2_A and VG1 & 2_B are connected internally so it would be enough to connect either one for proper orientation.

³ VG3_A and VG3_B are connected internally so it would be enough to connect either one for proper orientation.

⁴The RF input and output pad have a ground-signal-ground with a nominal pitch of 250 um. The RF ground pads are 100 x 100 microns.



Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA601C025D	6 - 12 GHz, 40 W GaN MMIC	1 Each	CHPROD COLLO
CMPA601C025D-AMP	Evaluation Board W/PA	1 Each	



Notes & Disclaimer

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