CMPA1H1J050F

17.3 – 18.4 GHz, 60 W GaN HPA

Description

The CMPA1H1J050F is a 60W package MMIC HPA utilizing the high performance, 0.15um GaN on SiC production process. The CMPA1H1J050F operates from 17.3-18.4 GHz and supports Direct Broadcast Satellite communications. The CMPA1H1J050F achieves 60 W of saturated output power with 25 dB of large signal gain and typically 30% power-added efficiency under CW operation.

Packaged in a 17.5 x 24 mm bolt-down, flange package, the CMPA1H1J050F provides superior RF performance and thermal management allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Figure 1. CMPA1H1J050F

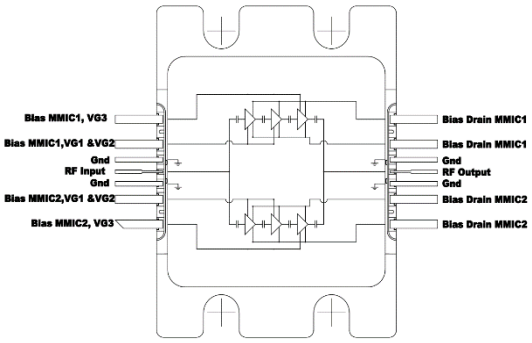


Figure 2. Functional Block Diagram

Features

- Psat: 60 W
- PAE: 30 %
- LSG: 25 dB
- S21: 30 dB
- S11: -10 dB
- S22: -6 dB
- CW operation

Applications

- Direct Broadcast Satcom

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional information.

RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	84	
Drain Voltage	V_D	V	28	
Gate Voltage	V_G	V	10, +2	
Drain Current	I_D	A	12.8	
Gate Current	I_G	mA	24.6	
Input Power	P_{in}	dBm	26	
Dissipated Power	P_{diss}	W	160	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	320	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	3:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	28	
Gate Voltage	Vg	V	-1.9	
Drain Current	Idq	mA	700	
Input Power	Pin	dBm	23	CW
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		17.3		18.4	
Output Power	dBm	17.3		47.0		
		17.8		48.5		
		18.4		48.0		
Power-added Efficiency	%	17.3		30		
		17.8		32		
		18.4		32		
LSG	dB	17.3		24.0		
		17.8		25.5		
		18.4		25.0		
Small-Signal Gain	dB	17.3		30		Pin = -20 dBm
		17.8		30		
		18.4		30		
Input Return Loss	dB			10		Pin = -20 dBm
Output Return Loss	dB			6		Pin = -20 dBm

Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 3: Pout v. Frequency v. Temperature

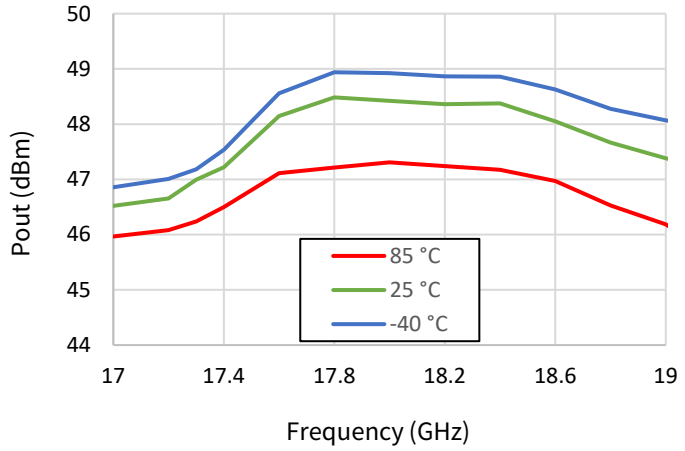


Figure 4: PAE v. Frequency v. Temperature

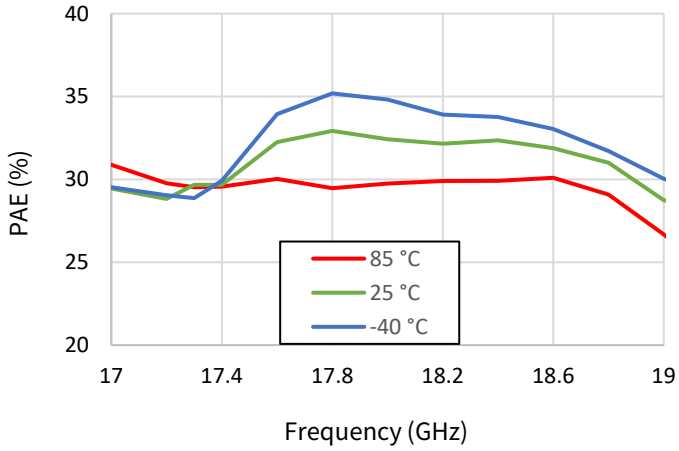


Figure 5: Id v. Frequency v. Temperature

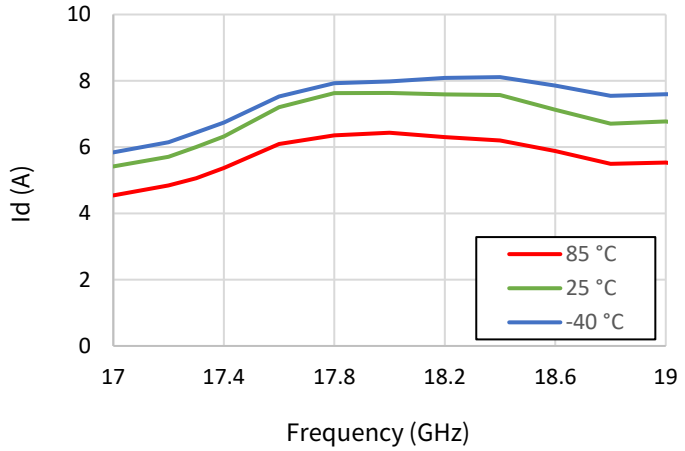


Figure 6: Ig v. Frequency v. Temperature

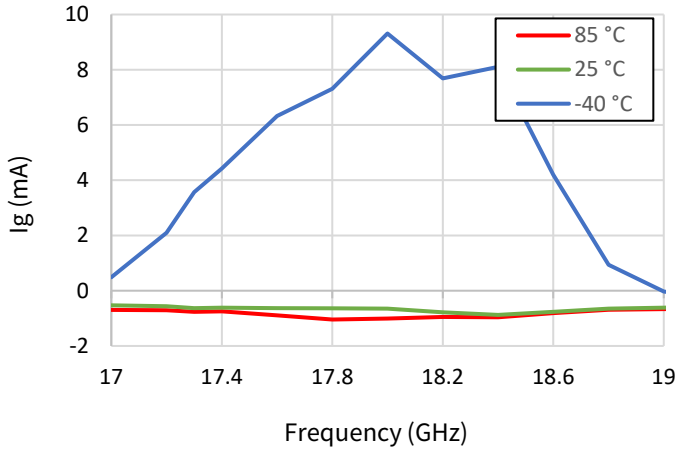
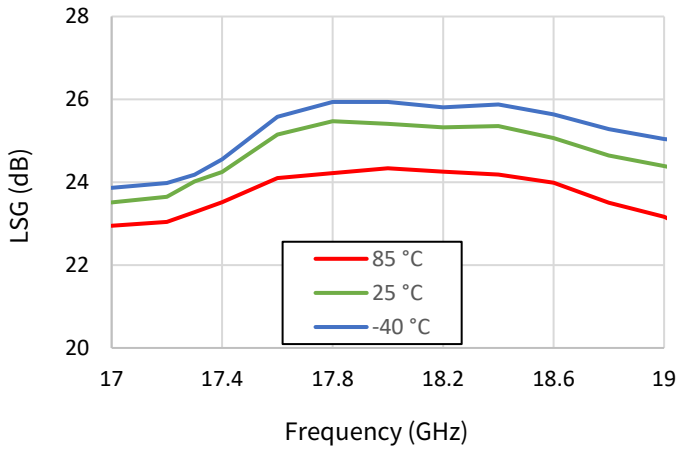


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 8: Pout v. Frequency v. Vd

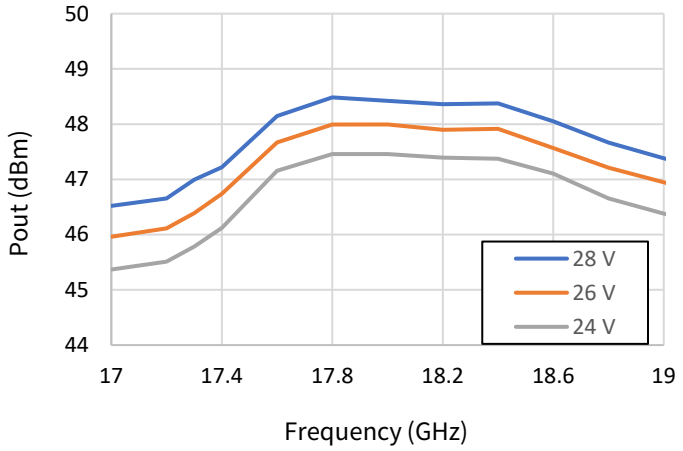


Figure 9: PAE v. Frequency v. Vd

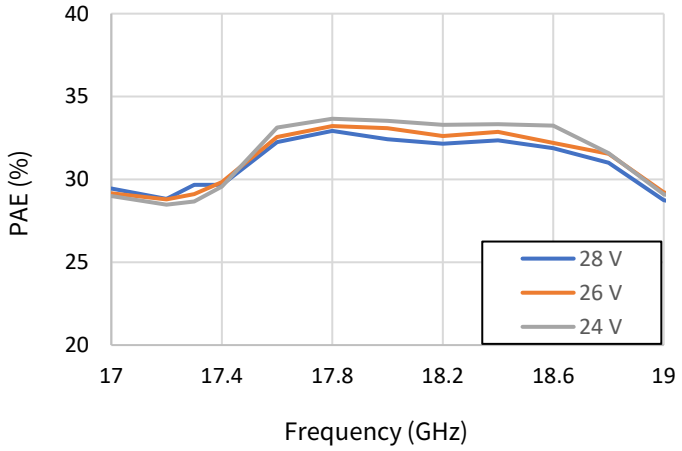


Figure 10: Id v. Frequency v. Vd

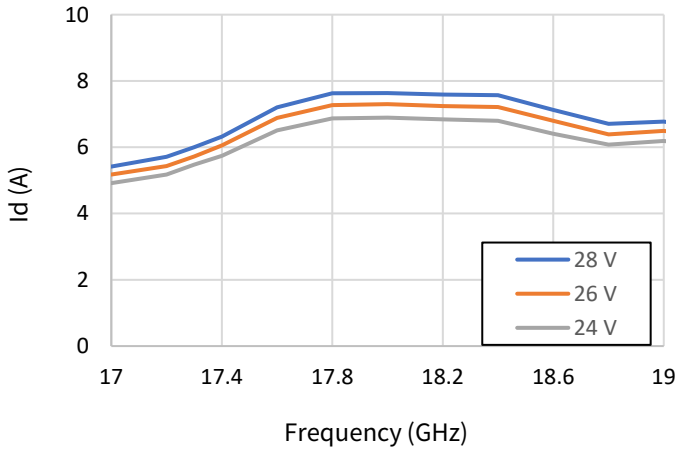


Figure 11: Ig v. Frequency v. Vd

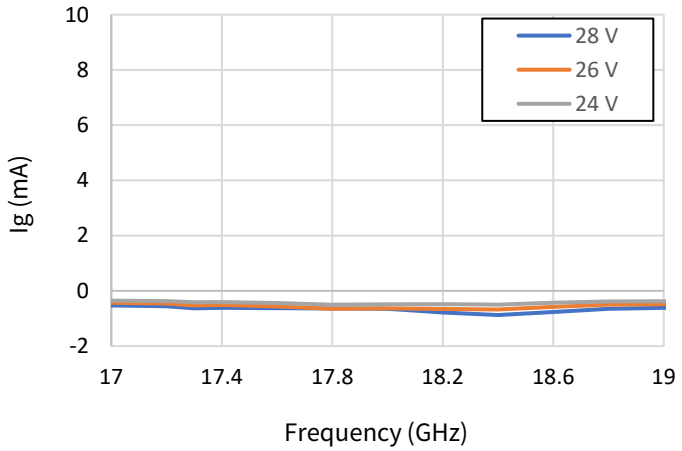
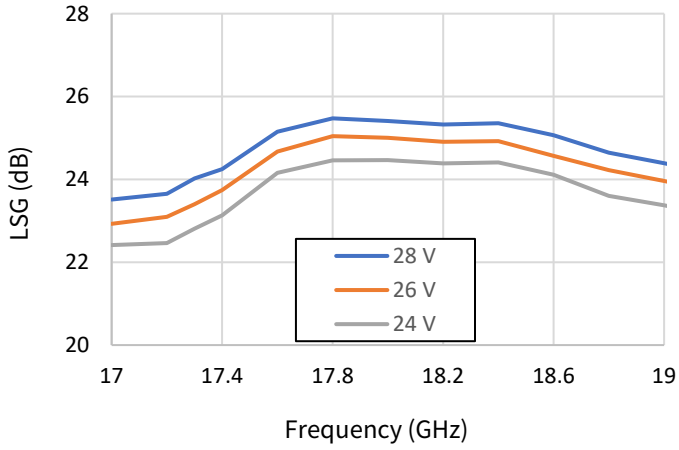


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 13: Pout v. Frequency v. Idq

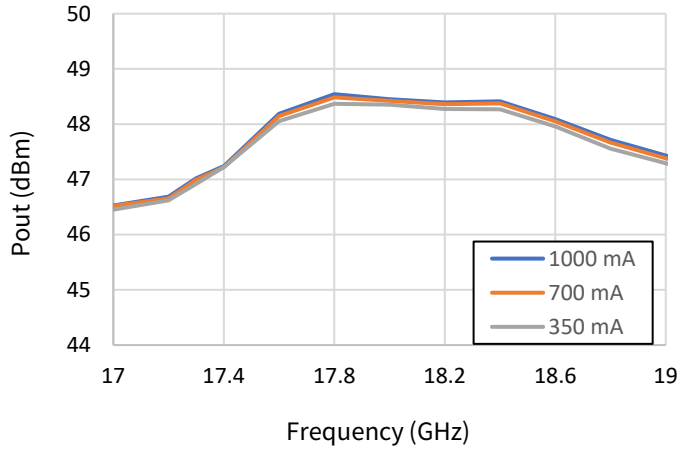


Figure 14: PAE v. Frequency v. Idq

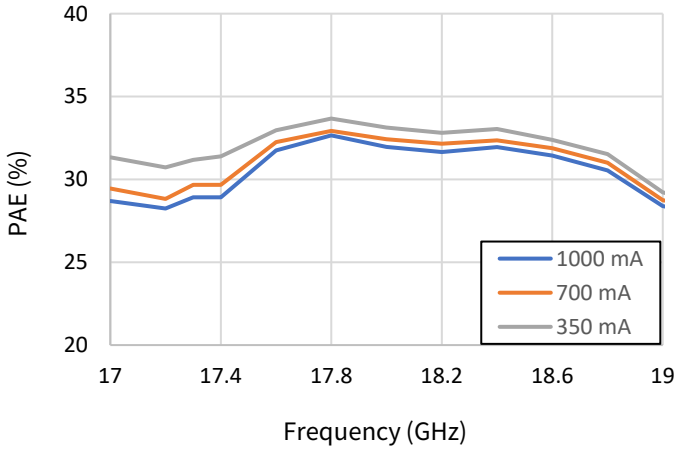


Figure 15: Id v. Frequency v. Idq

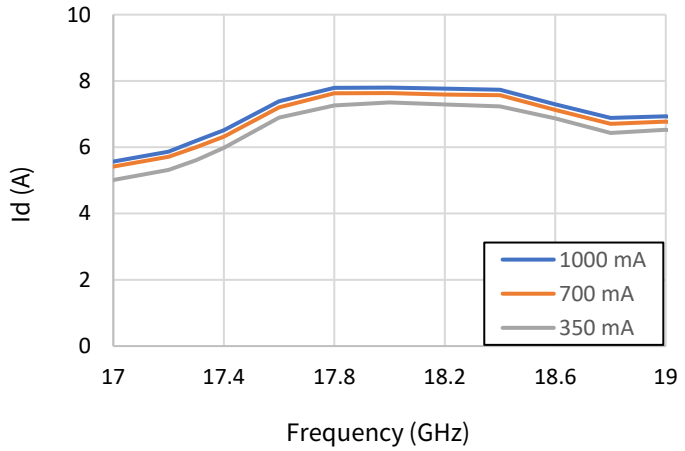


Figure 16: Ig v. Frequency v. Idq

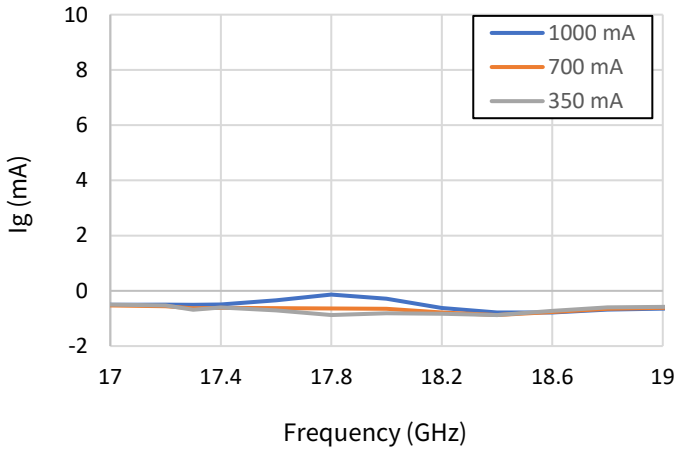
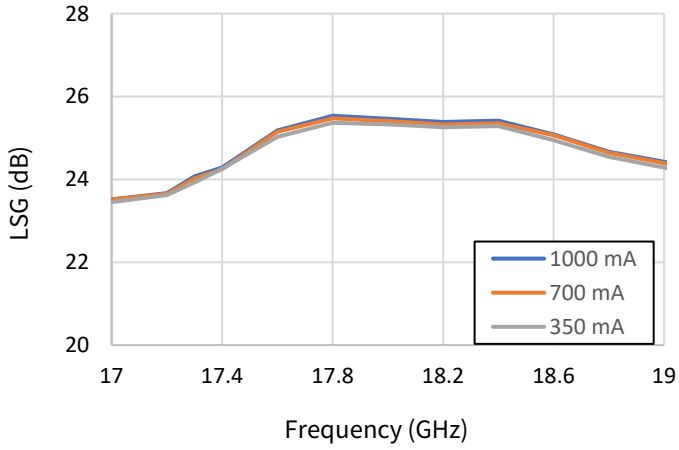


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 18: Pout v. Pin v. Frequency

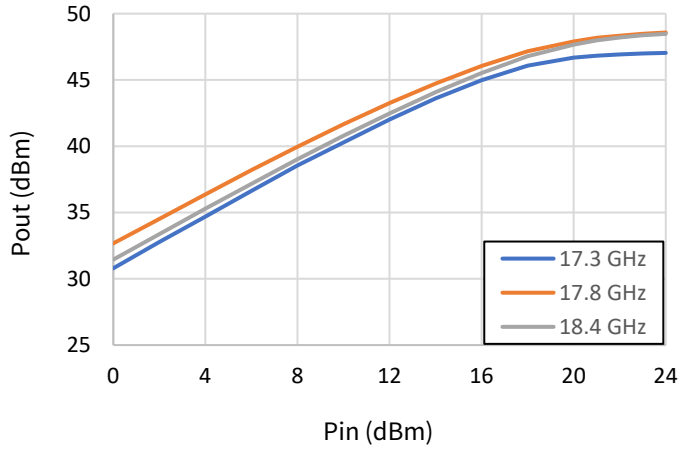


Figure 19: PAE v. Pin v. Frequency

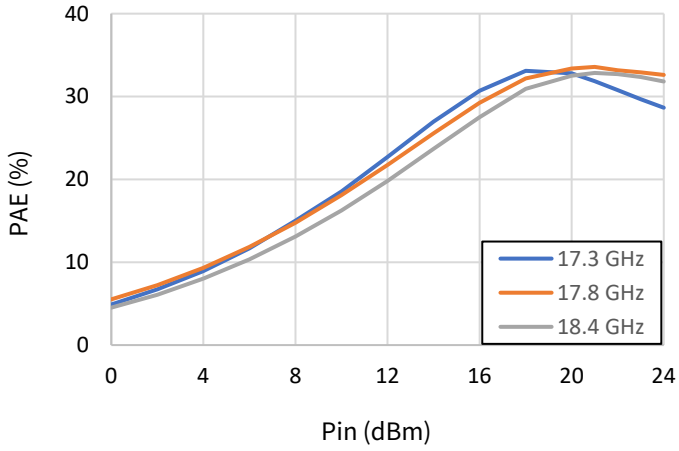


Figure 20: Id v. Pin v. Frequency

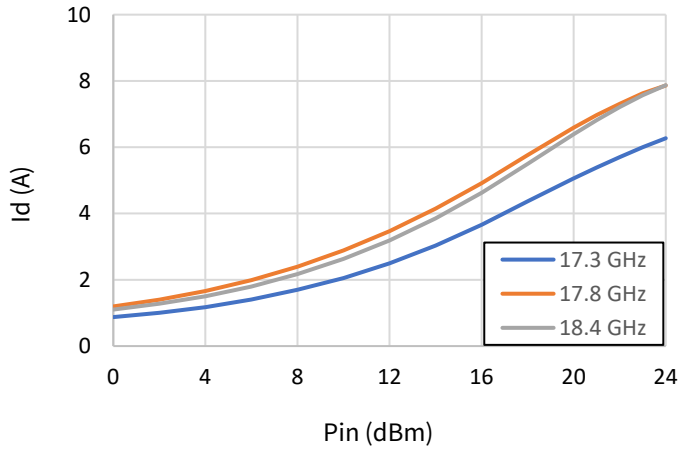


Figure 21: Ig v. Pin v. Frequency

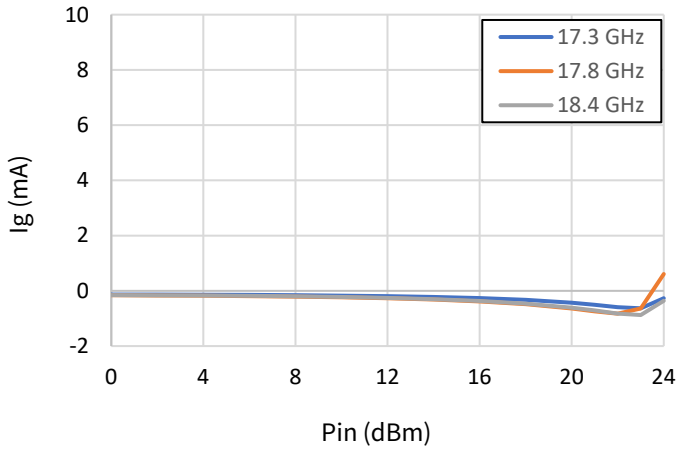
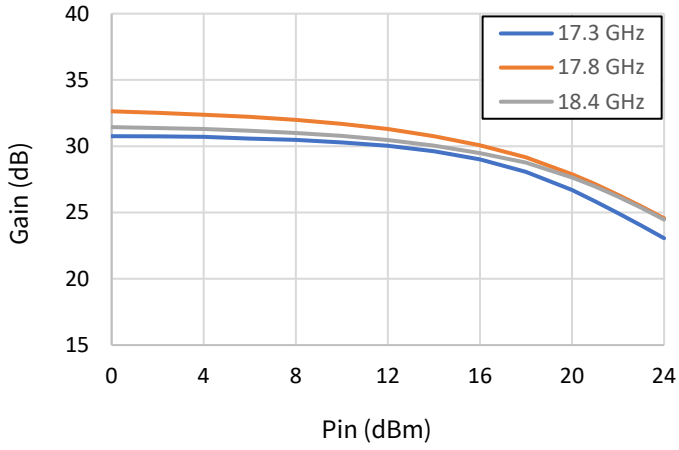


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 23: Pout v. Pin v. Temperature

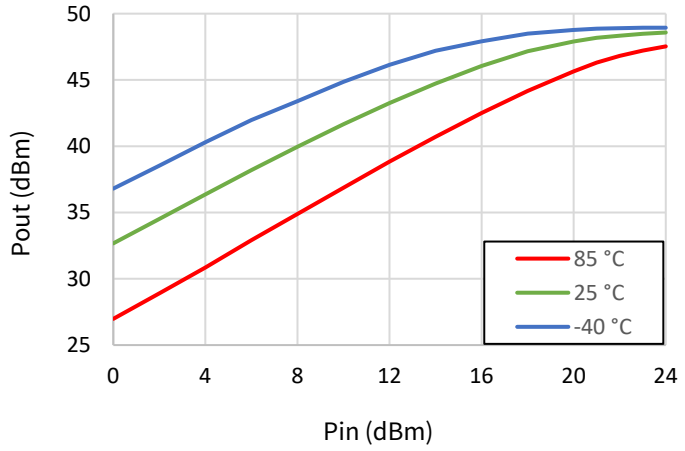


Figure 24: PAE v. Pin v. Temperature

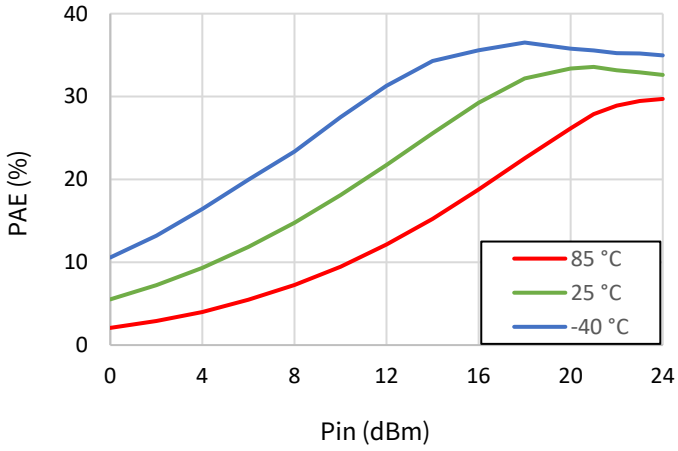


Figure 25: Id v. Pin v. Temperature

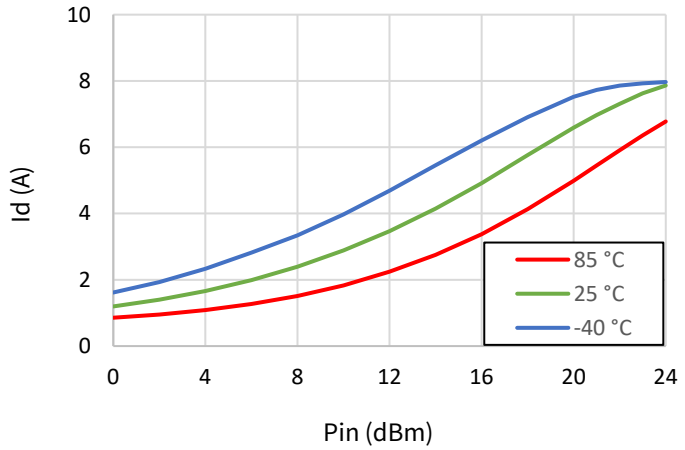


Figure 26: Ig v. Pin v. Temperature

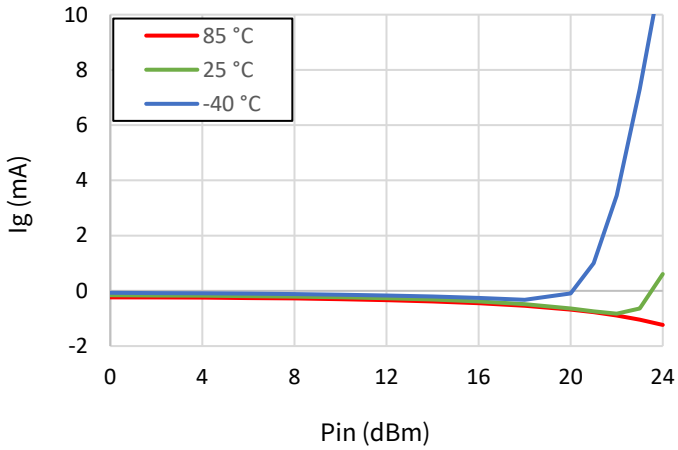
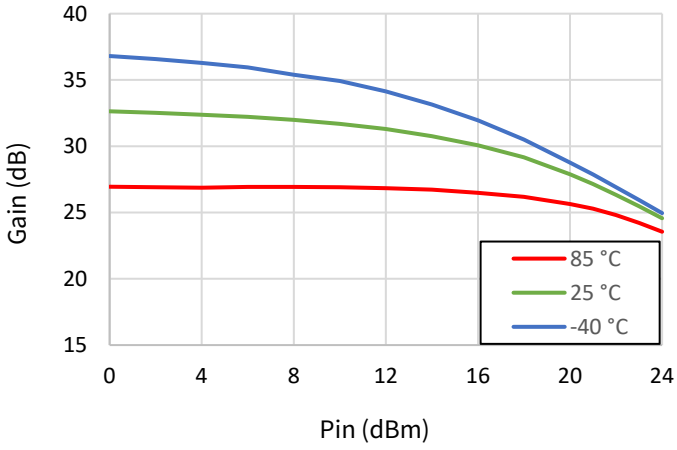


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 28: Pout v. Pin v. Vd

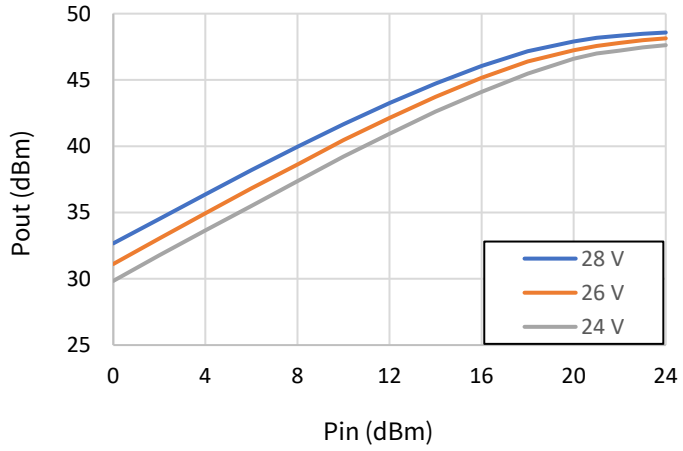


Figure 29: PAE v. Pin v. Vd

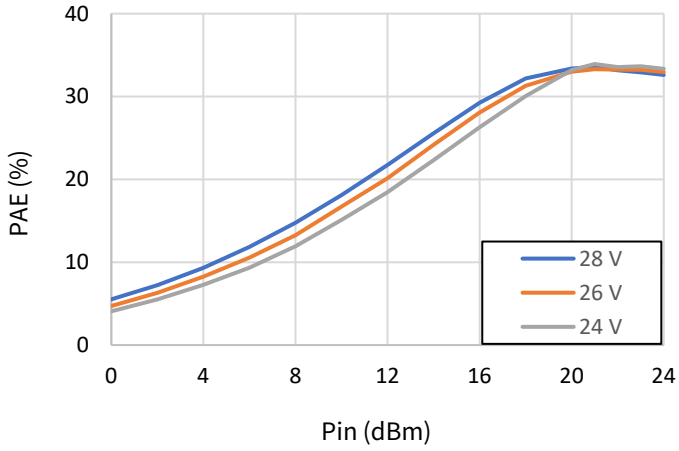


Figure 30: Id v. Pin v. Vd

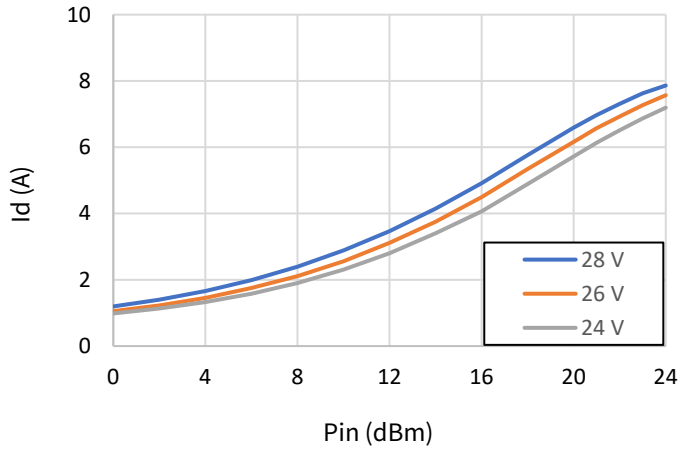


Figure 31: Ig v. Pin v. Vd

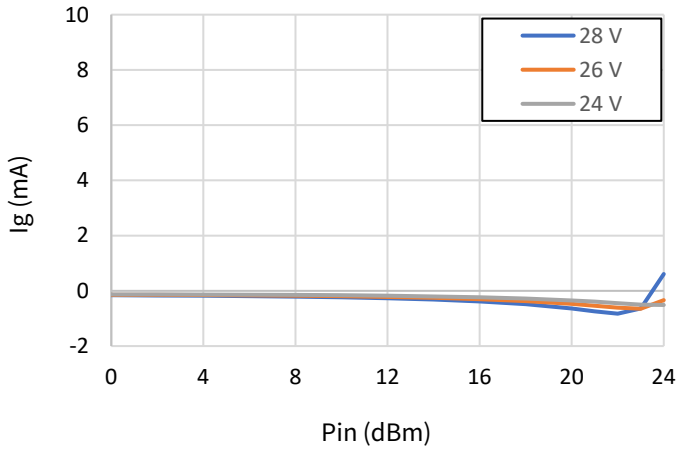
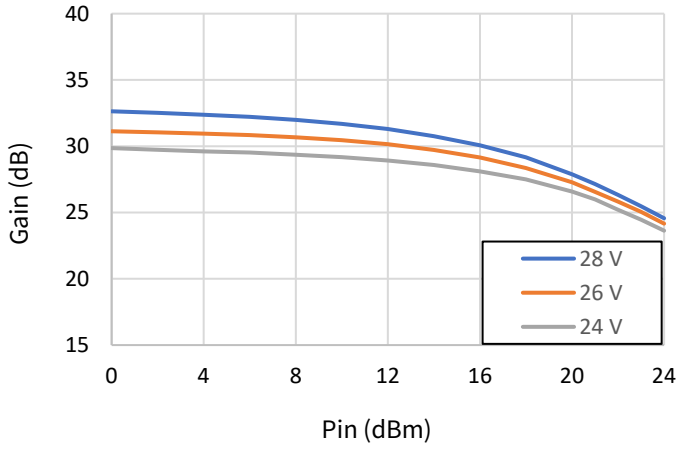


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = 23 dBm, T_{base}=25 °C, Frequency: 17.8GHz

Figure 33: Pout v. Pin v. Idq

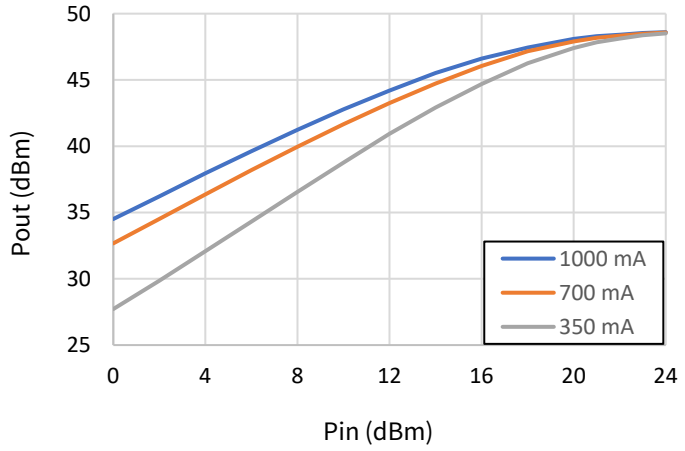


Figure 34: PAE v. Pin v. Idq

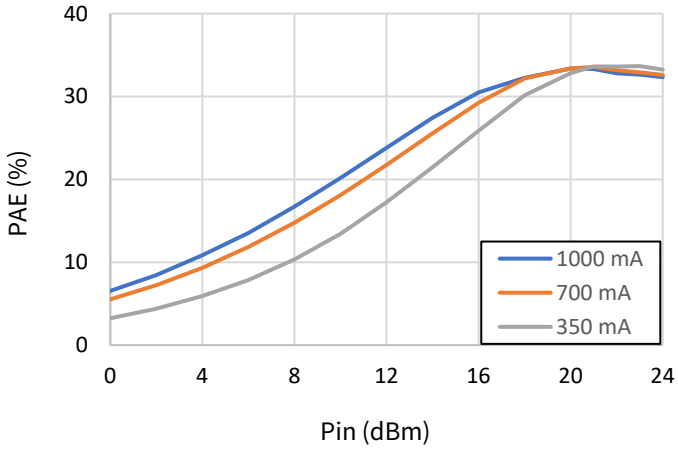


Figure 35: Id v. Pin v. Idq

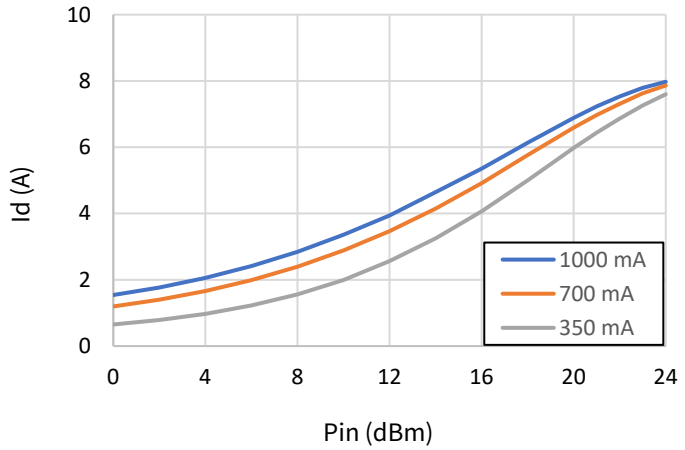


Figure 36: Ig v. Pin v. Idq

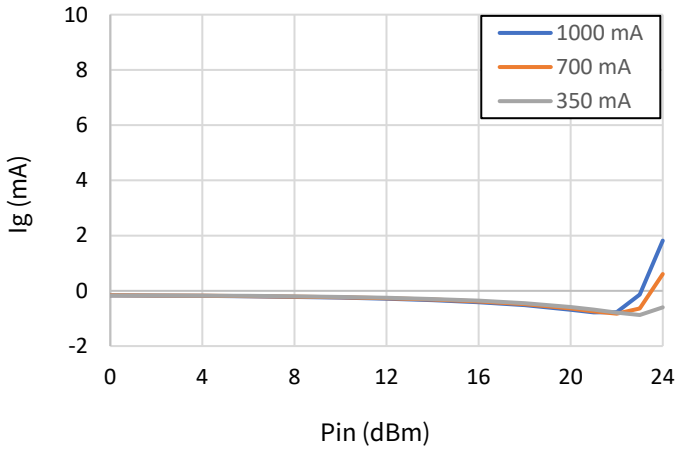
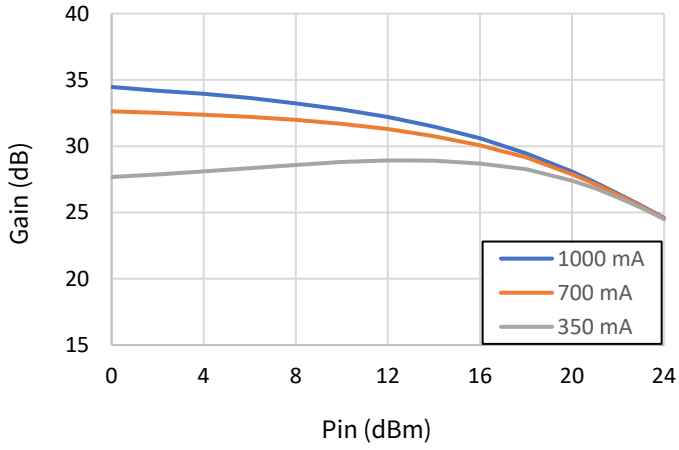


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = -20 dBm, T_{base}=25 °C

Figure 38: S21 v. Frequency v. Temperature

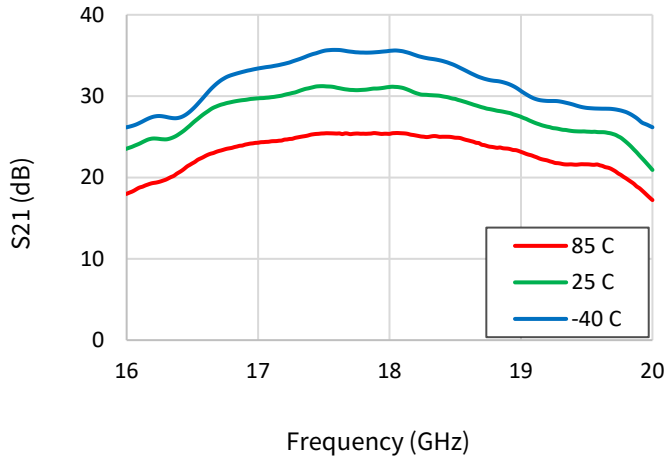


Figure 39: S21 v. Frequency v. Vd

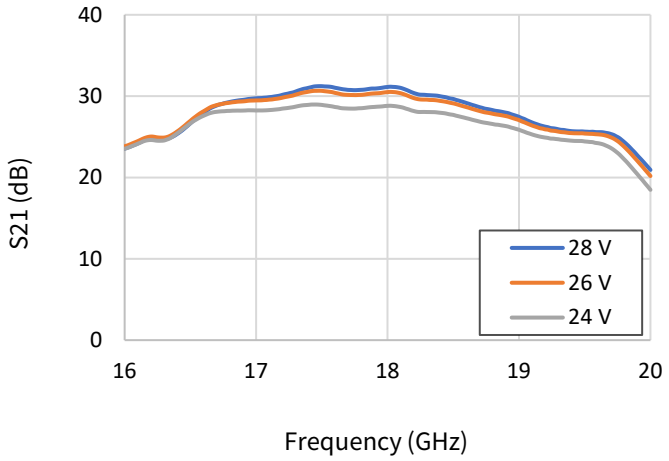


Figure 40: S11 v. Frequency v. Temperature

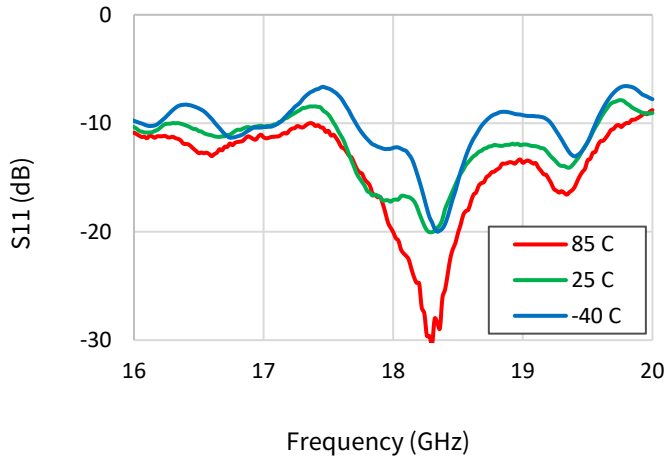


Figure 41: S11 v. Frequency v. Vd

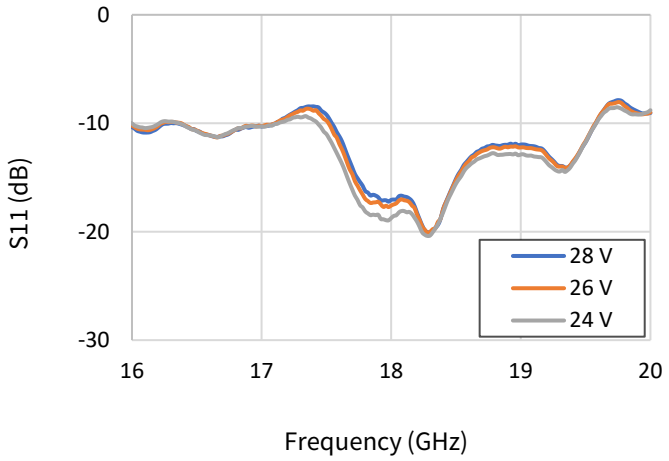


Figure 42: S22 v. Frequency v. Temperature

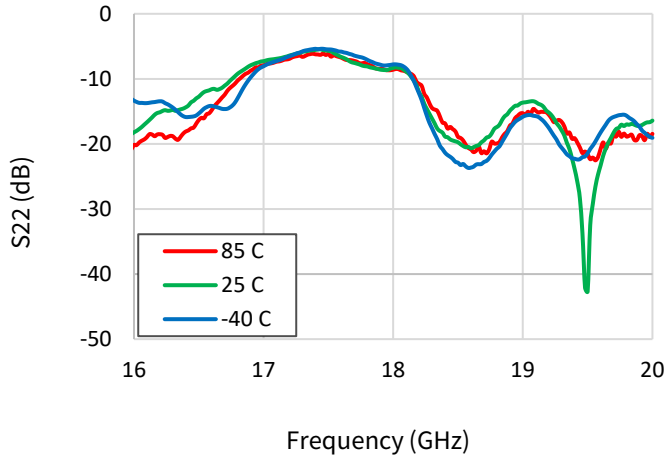
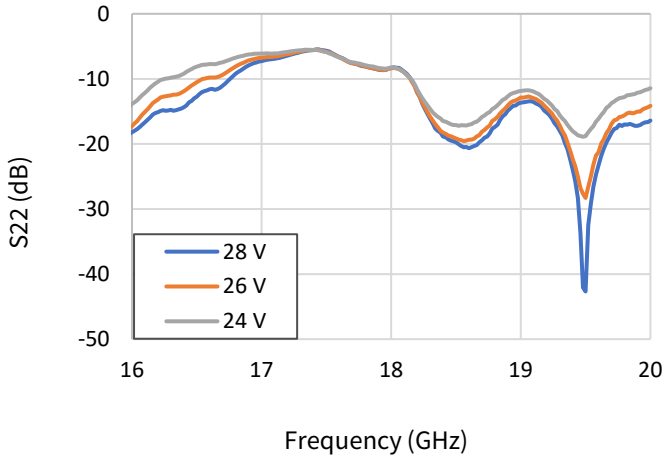


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pin = -20 dBm, T_{base}=25 °C

Figure 44: S21 v. Frequency v. Idq

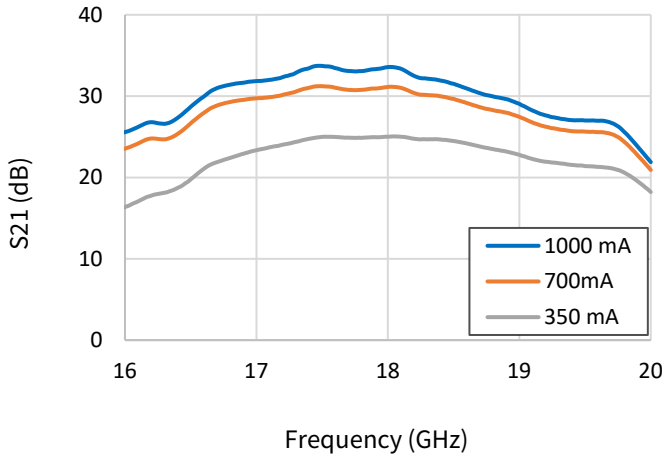


Figure 45: S11 v. Frequency v. Idq

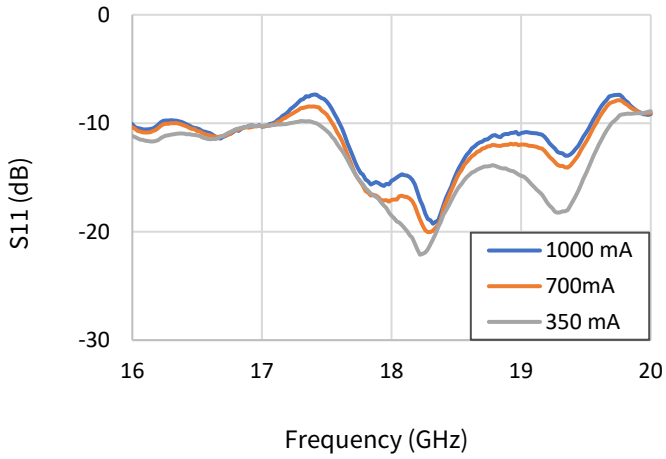
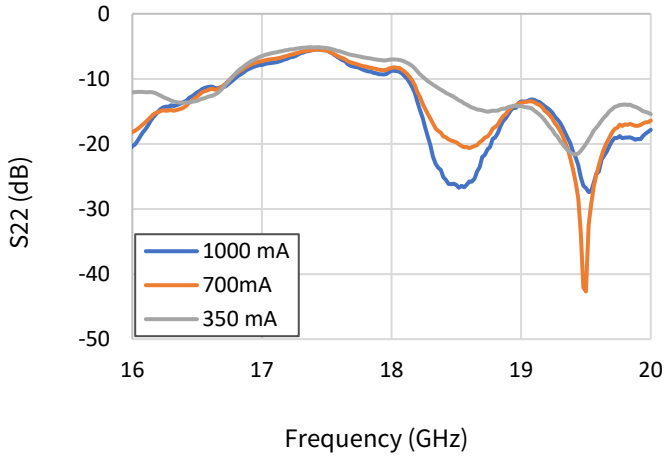


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=0.7A, CW, Pout/tone = 41 dBm, Frequency = 17.8 GHz, Tone Spacing = 1MHz, T_{base}=25 °C

Figure 47: IM3 v. Pout/tone v. Frequency

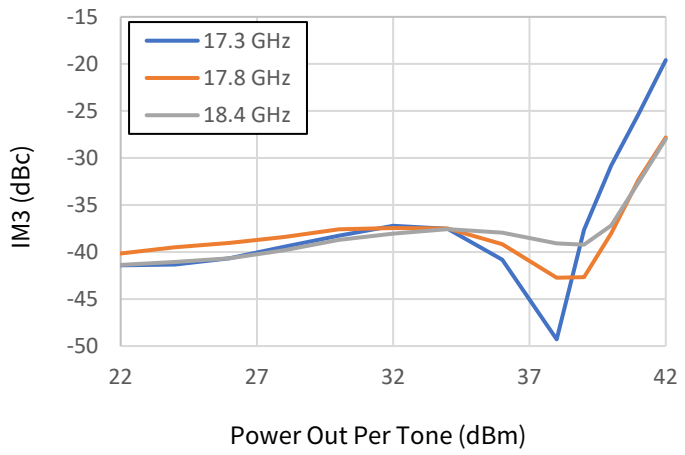


Figure 48: IM5 v. Pout/tone v. Frequency

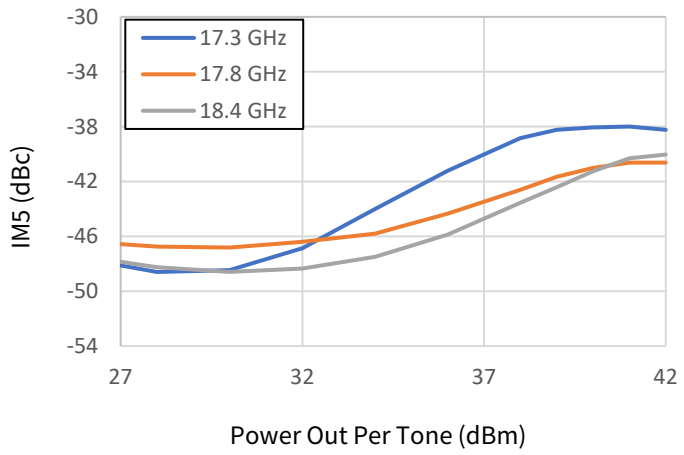


Figure 49: IM3 v. Pout/tone v. Temperature

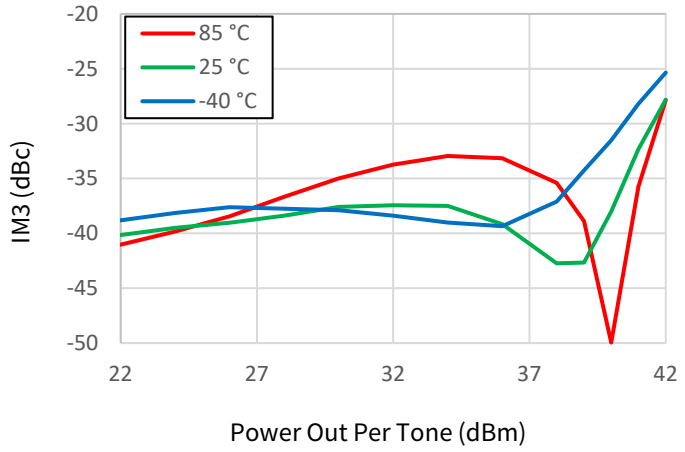


Figure 50: IM5 v. Pout/tone v. Temperature

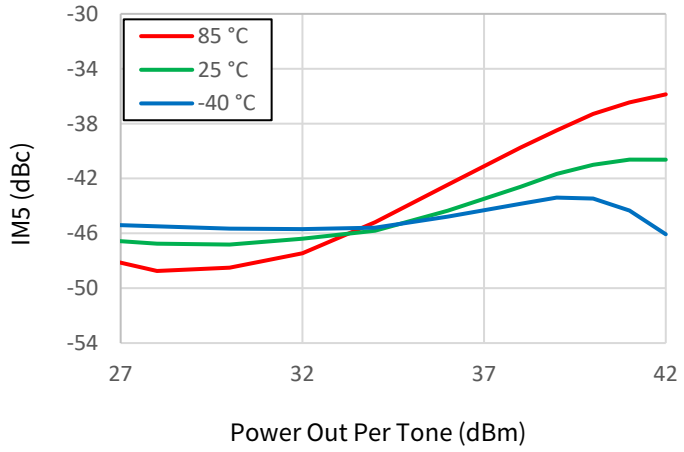


Figure 51: IM3 v. Pout/tone v. Idq

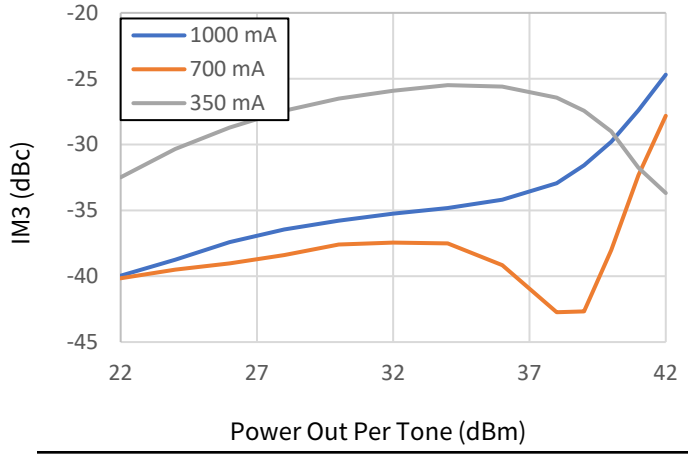
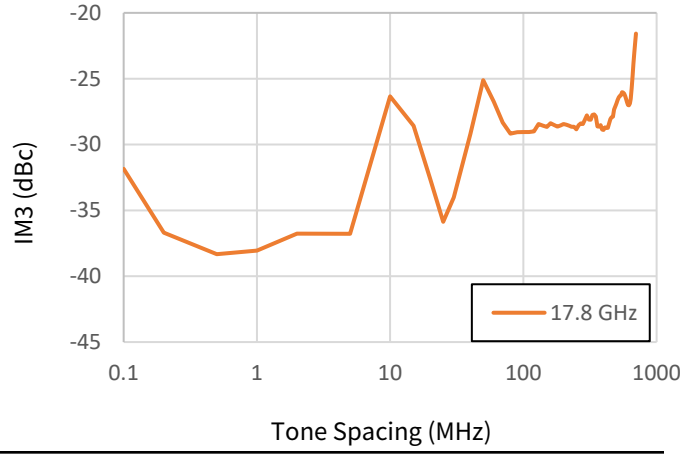


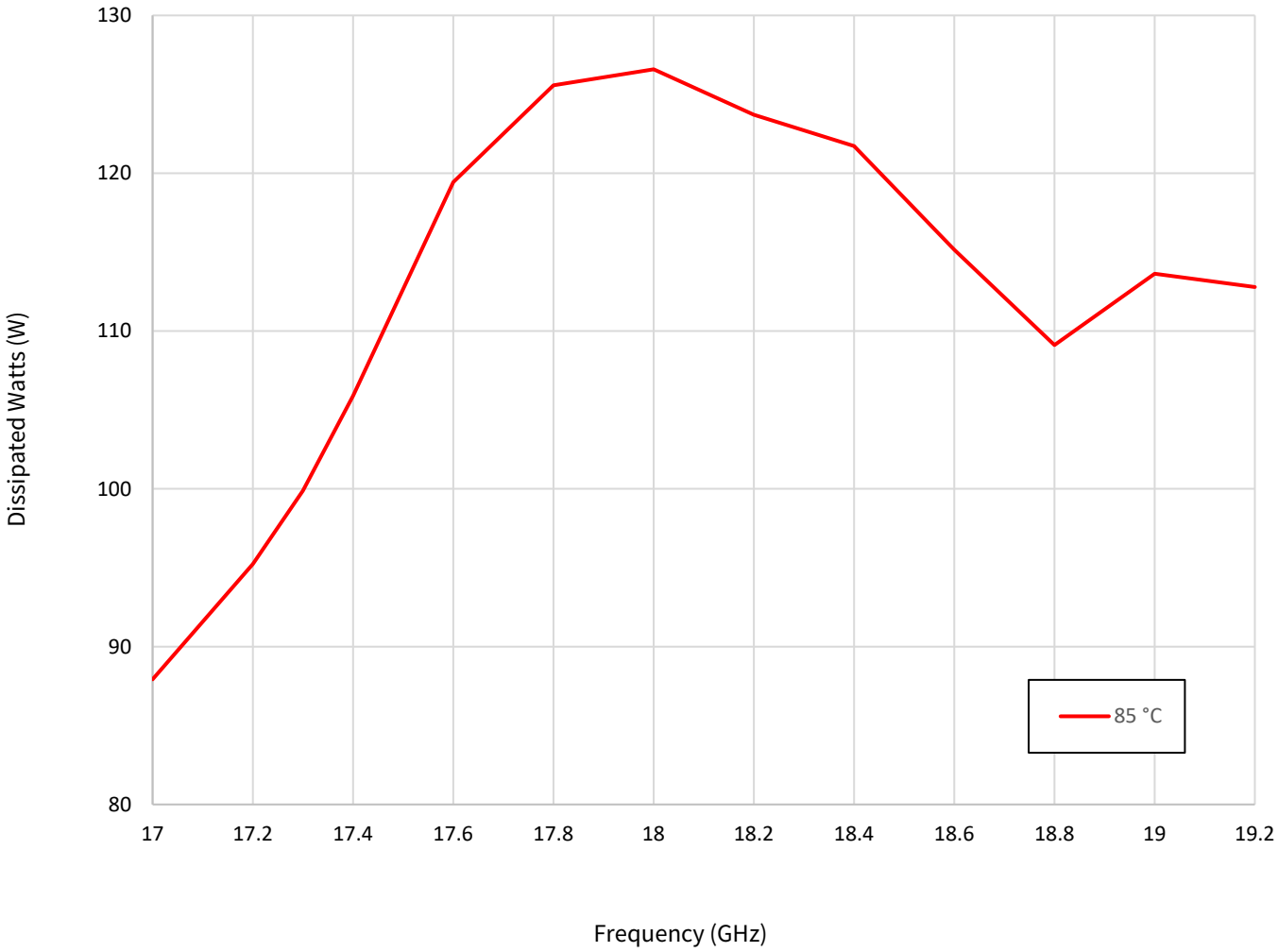
Figure 52: IM3 v. Tone Spacing v. Frequency



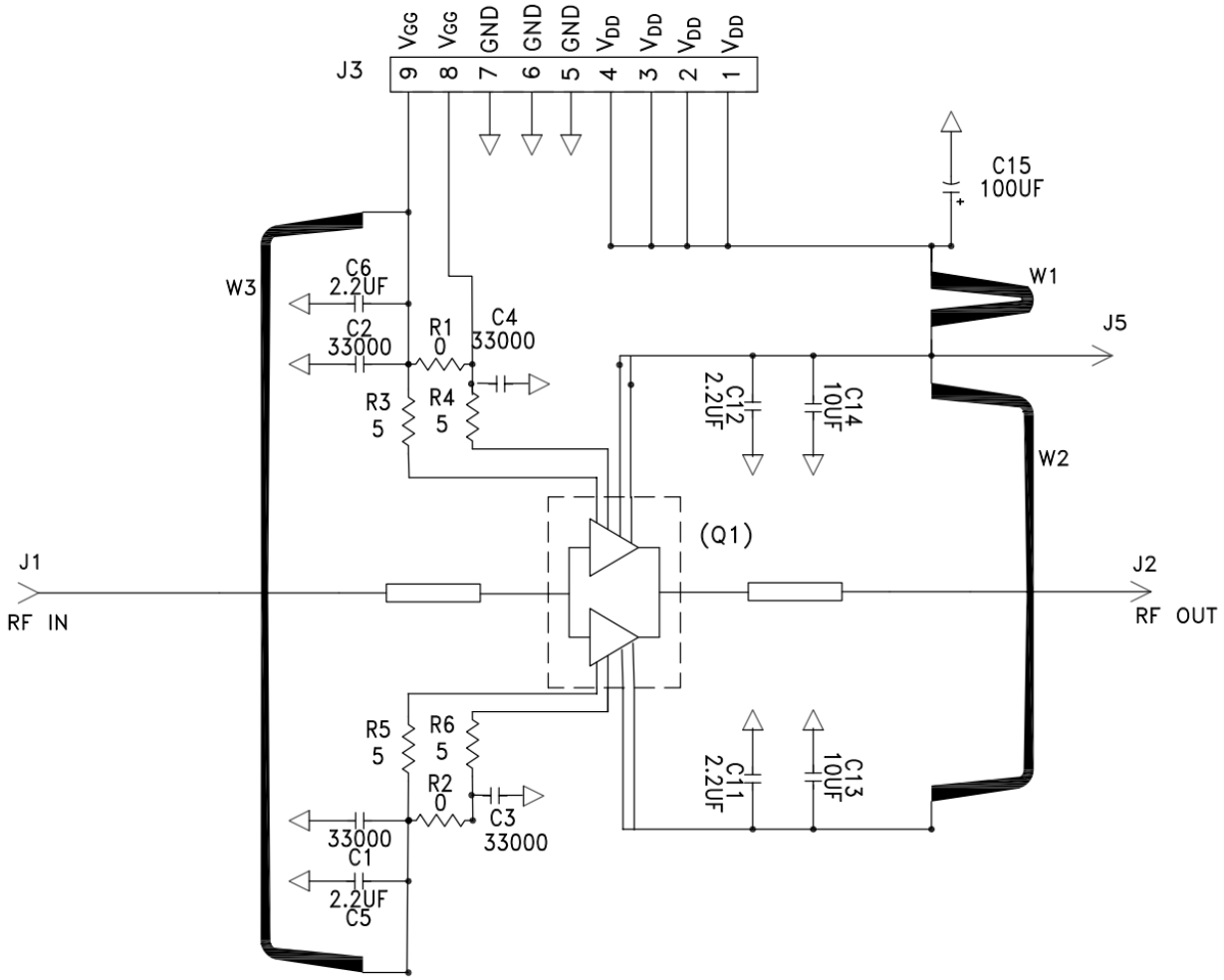
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	215.3	Freq = 17.8 GHz, V_d = 28 V, I_{dq} = 700 mA, I_{drive} = 6.35 A, P_{in} = 23 dBm, P_{out} = 47.2 dBm, P_{diss} = 125.3 W, T_{case} = 85°C, CW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.04	

Power Dissipation v. Frequency (Tcase = 85°C)



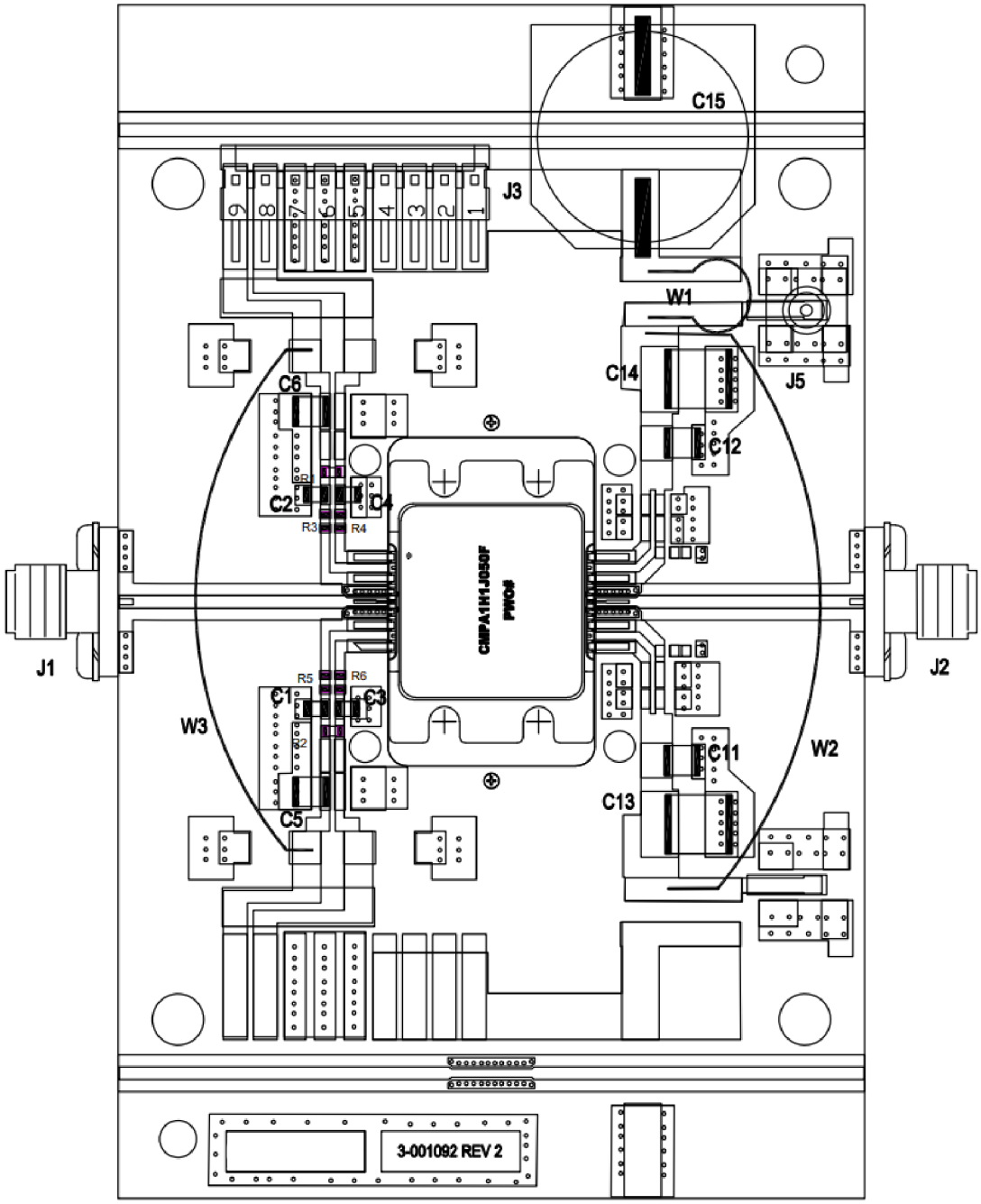
CMPA1H1J050F-AMP Evaluation Board Schematic Drawing



CMPA1H1J050F-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
C1,C3,C2,C4	CAP, 33000PF, 0805,100V, X7R	4
C5,C6,C11,C12	CAP, 2.2UF, 100V, 10%, X7R, 1210	4
C13,C14	CAP, 10UF, 100V, 10%, X7R, 2220	2
C15	CAP, 100 UF, 20%, 160V, ELEC	1
W1, W2, W3	WIRE, 18 AWG ~ 1.75”	3
J1,J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J5	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	1
Q1	CMPA1H1J050F, MMIC	1
-	PCB, ROGERS 6035 HTC, 2.5x4.0x0.020 IN	1
-	BASEPLATE, CU, 2.5 X 4.0 X 0.5 IN	1
-	2-56 SOC HD SCREW 1/4 SS	4
-	#2 SPLIT LOCKWASHER SS	4
R1,R2	RES,1/16W,0603,1%,0 OHMS	2
R3,R4,R5,R6	RES,1/16W,0603,1%,5.1 OHMS	4

CMPA1H1J050F-AMP Evaluation Board Assembly Drawing



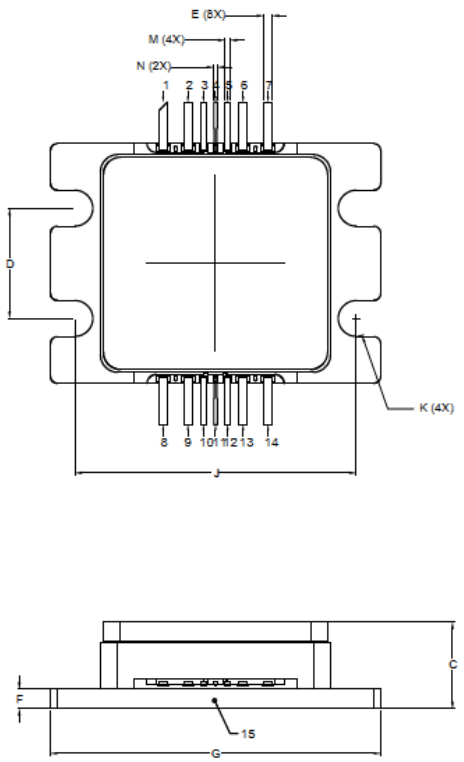
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

Product Dimensions



NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.679	0.691	17.25	17.55
B	0.003	0.006	0.076	0.152
C	0.234	0.261	5.94	6.63
D	0.307	0.323	7.80	8.20
E	0.016	0.032	0.406	0.813
F	0.047	0.063	1.194	1.600
G	0.936	0.954	23.77	24.23
H	0.912	0.930	23.16	23.62
J	0.795	0.811	20.19	20.60
K	ø0.094	ø0.110	ø2.39	ø2.79
L	0.062	0.078	1.575	1.981
M	0.006	0.022	0.152	0.559
N	0.004	0.018	0.102	0.457

PIN	DESC.	PIN	DESC.
1	Bias MMIC2, Gate St3	8	Bias Drain MMIC 2
2	Bias MMIC2, Gate St1&ST2	9	Bias Drain MMIC 2
3	GND	10	GND
4	RF IN	11	RF OUT
5	GND	12	GND
6	Bias MMIC1, Gate St1&ST2	13	Bias Drain MMIC 1
7	Bias MMIC1, Gate St3	14	Bias Drain MMIC 1

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA1H1J050F	17.3 – 18.4 GHz, 60W GaN MMIC		
CMPA1H1J050F-AMP	Evaluation Board w/ PA	1 Each	

Notes & Disclaimer

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