CMPA1842040F

1.8 – 4.2 GHz, 45 W GaN HPA

Description

The CMPA1842040F is a 45W MMIC HPA utilizing the high performance, 0.15um GaN on SiC production process. The CMPA1842040F operates from 1.8-4.2 GHz and supports electronic warfare applications. The CMPA1842040F achieves 45 W of saturated output power with 24 dB of large signal gain and typically 45% power-added efficiency under CW operation.

Packaged in a 15x15 mm bolt-down, flange package, the CMPA1842040F provides superior thermal management and RF performance over a more targeted narrow bandwidth allowing customers to improve SWaP-C benchmarks in their next-generation systems.

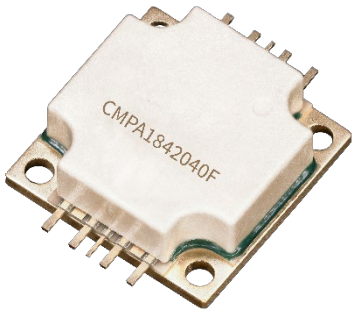


Figure 1. CMPA1842040F

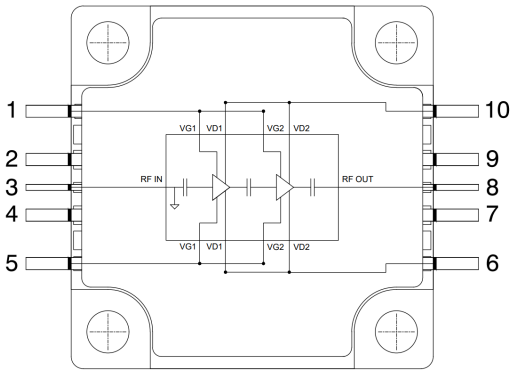


Figure 2. Functional Block Diagram

Features

- Psat: 45 W
- PAE: 45 %
- LSG: 24 dB
- S21: 26 dB
- S11: -10 dB
- S22: -8 dB
- CW operation
- Cu-based, flange package

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional information.

Applications

- Electronic Warefare

RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	84	
Drain Voltage	V_D	V	28	
Gate Voltage	V_G	V	-10, +2	
Drain Current	I_D	A	4.8	
Gate Current	I_G	mA	12.5	
Input Power	P_{in}	dBm	23	
Dissipated Power	P_{diss}	W	78	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	260	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	5:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	28	
Gate Voltage	Vg	V	-2.2	
Drain Current	Idq	mA	550	
Input Power	Pin	dBm	22	CW
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		1.8		4.2	
Output Power	dBm	1.8		46		
		3		46.5		
		4.2		46.5		
Power-added Efficiency	%	1.8		55		
		3		46		
		4.2		40		
LSG	dB	1.8		24		
		3		24.5		
		4.2		24.5		
Small-Signal Gain (S21)	dB	1.8		26		Pin = -20 dBm
		3		27		
		4.2		26		
Input Return Loss	dB			-10		Pin = -20 dBm
Output Return Loss	dB			-8		Pin = -20 dBm

Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 3: Pout v. Frequency v. Temperature

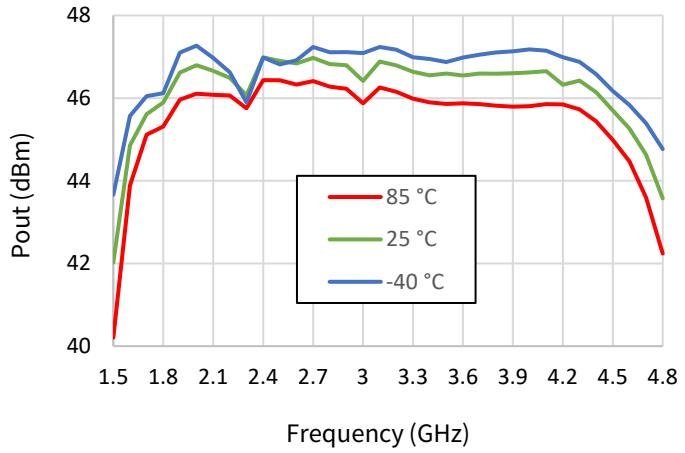


Figure 4: PAE v. Frequency v. Temperature

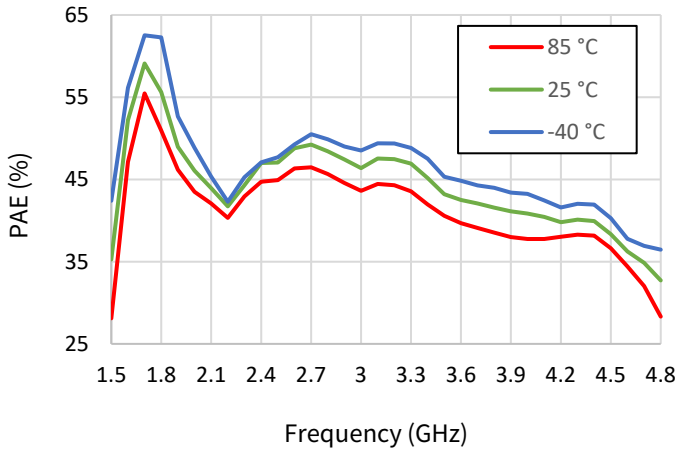


Figure 5: Id v. Frequency v. Temperature

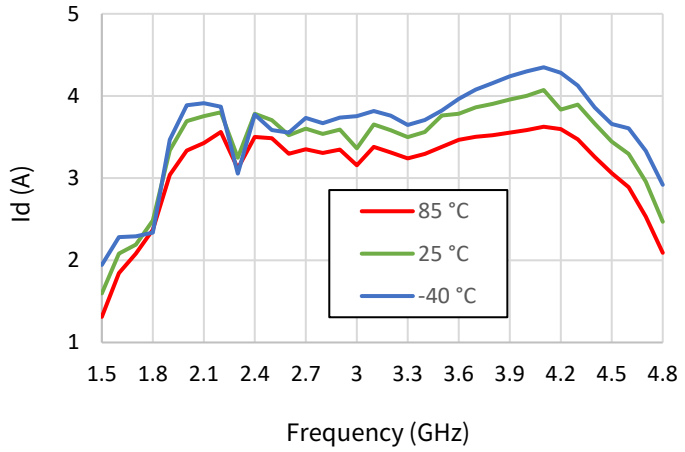


Figure 6: Ig v. Frequency v. Temperature

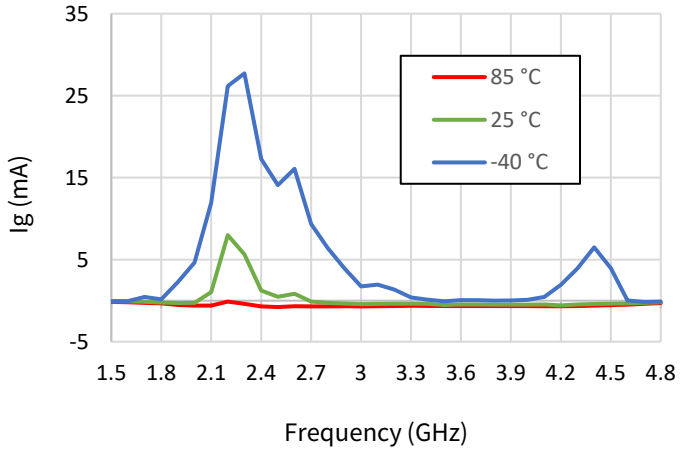
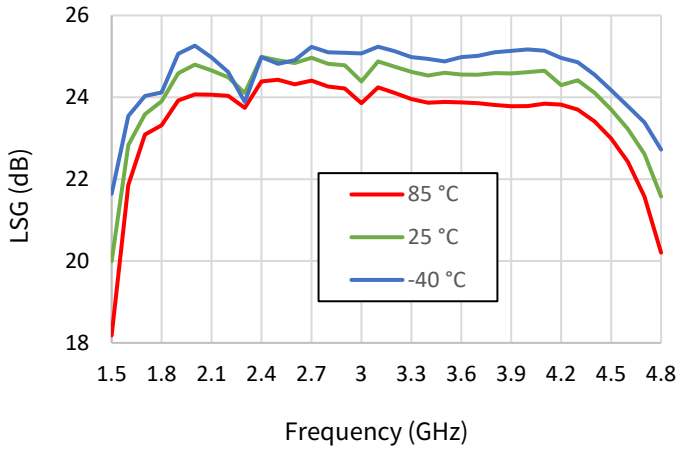


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 8: Pout v. Frequency v. Vd

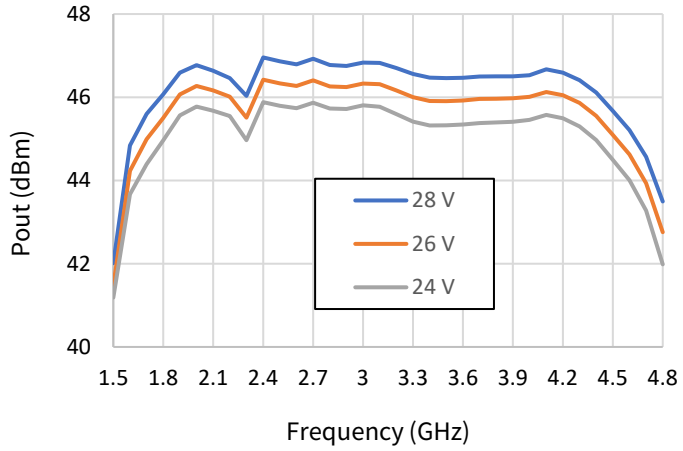


Figure 9: PAE v. Frequency v. Vd

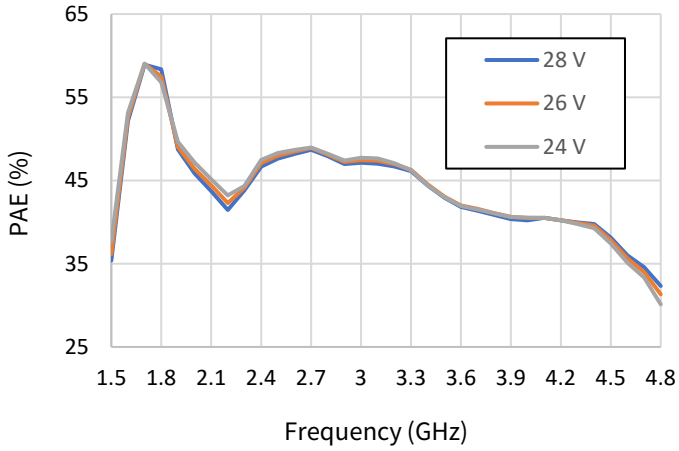


Figure 10: Id v. Frequency v. Vd

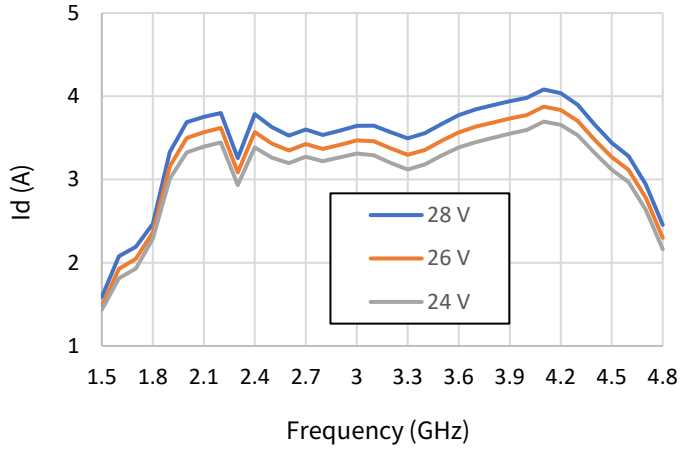


Figure 11: Ig v. Frequency v. Vd

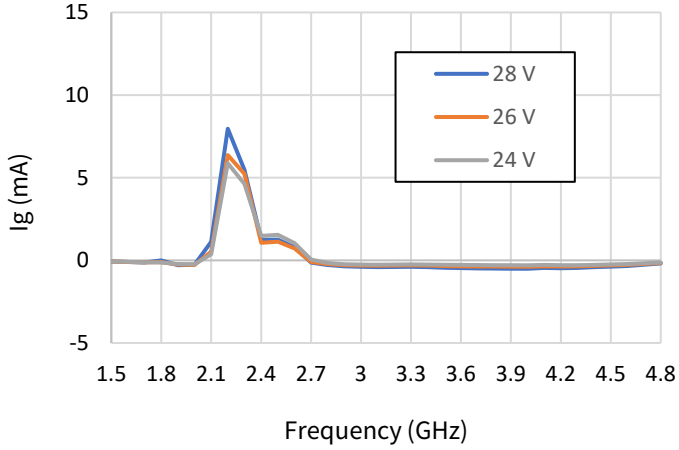
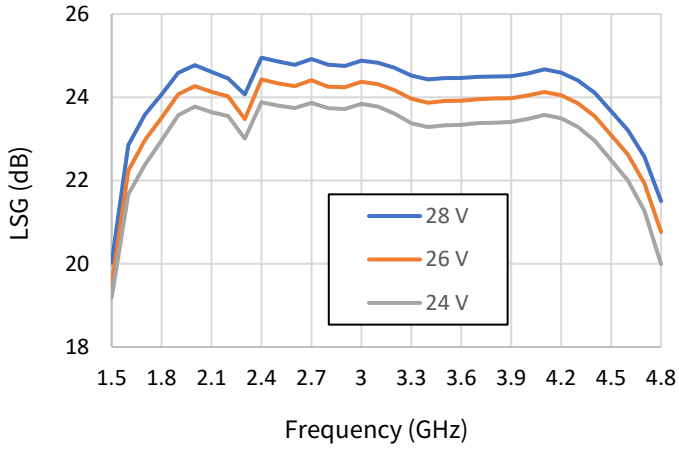


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 13: Pout v. Frequency v. Idq

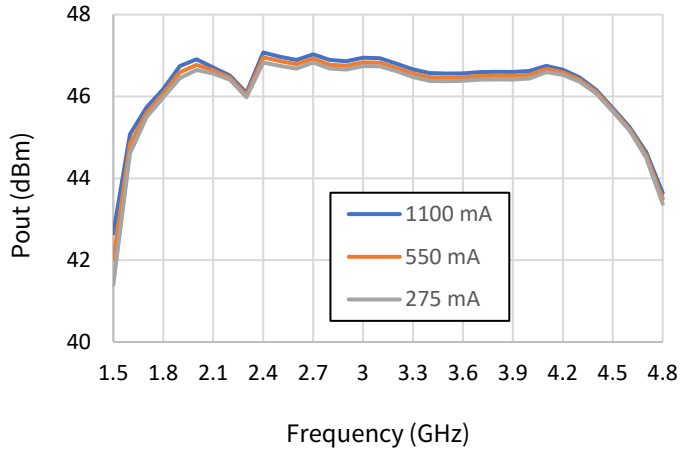


Figure 14: PAE v. Frequency v. Idq

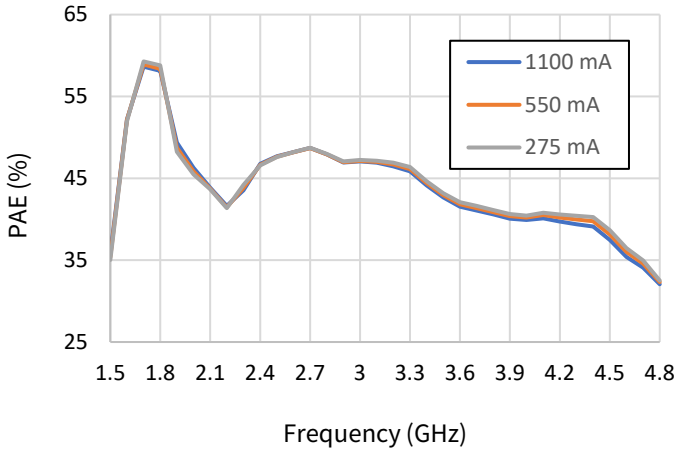


Figure 15: Id v. Frequency v. Idq

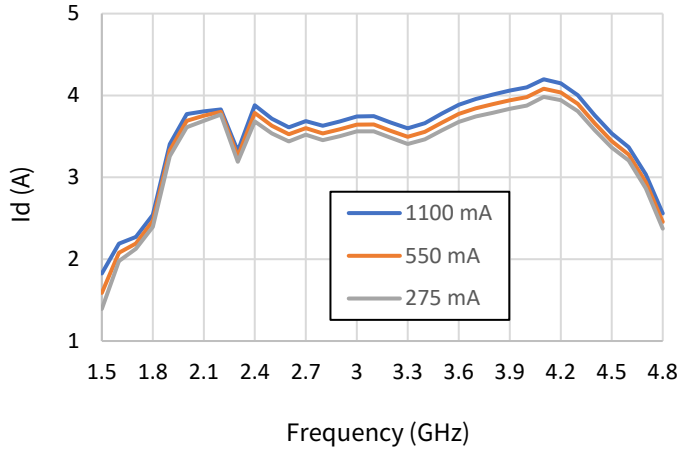


Figure 16: Ig v. Frequency v. Idq

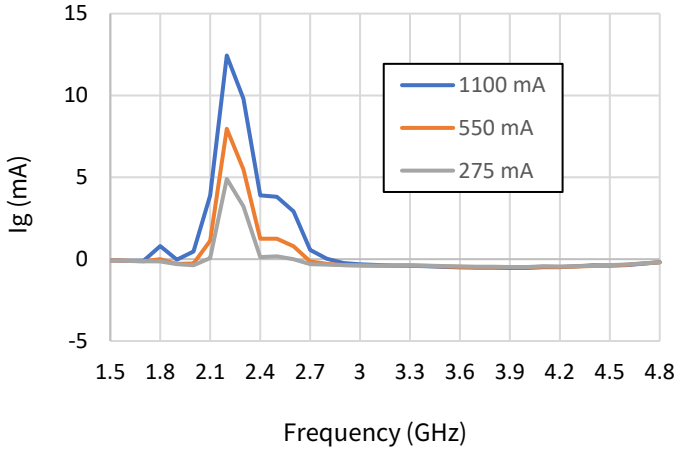
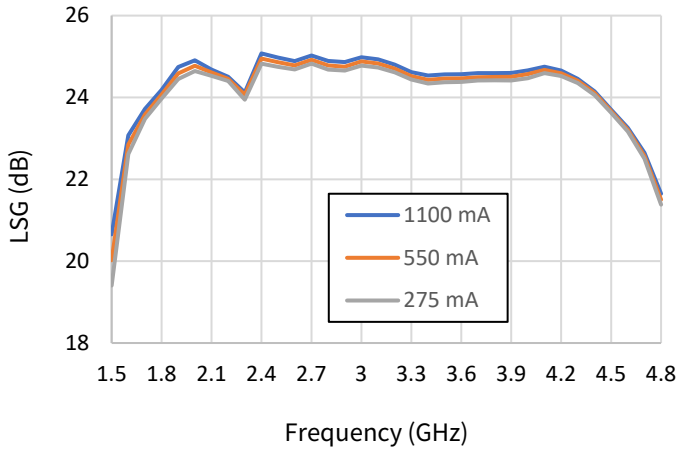


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 18: Pout v. Pin v. Frequency

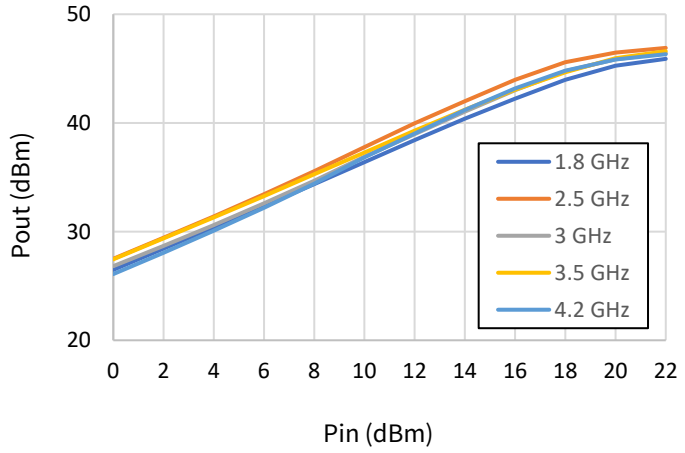


Figure 19: PAE v. Pin v. Frequency

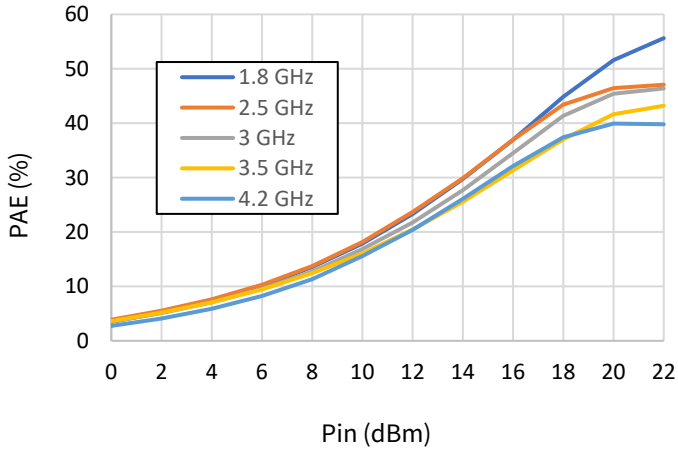


Figure 20: Id v. Pin v. Frequency

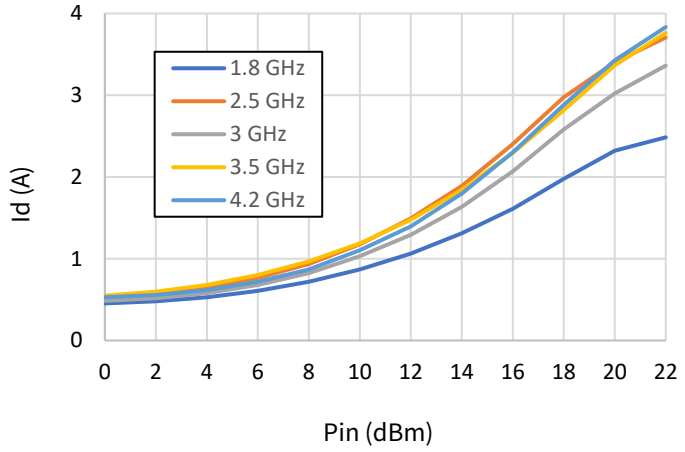


Figure 21: Ig v. Pin v. Frequency

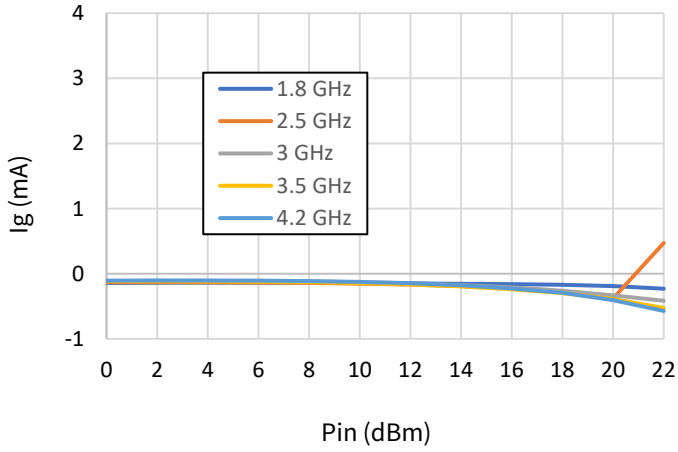
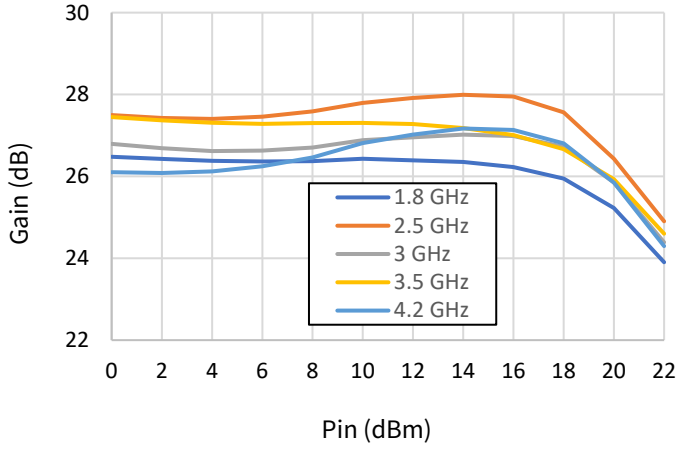


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 23: Pout v. Pin v. Temperature

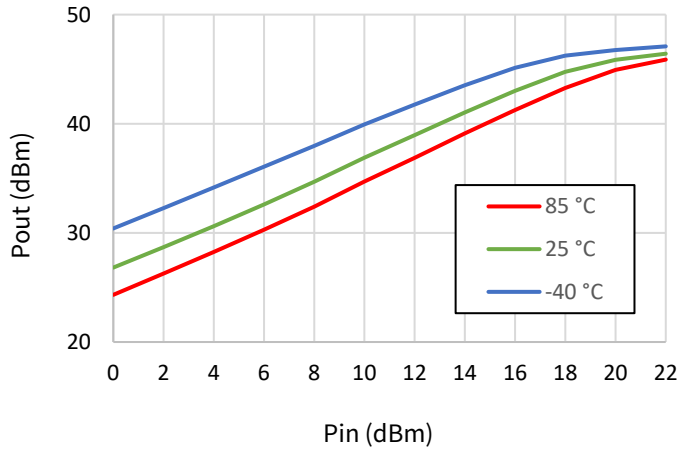


Figure 24: PAE v. Pin v. Temperature

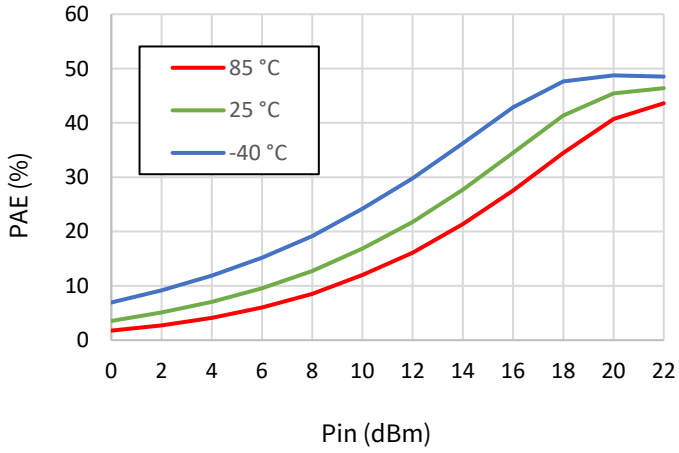


Figure 25: Id v. Pin v. Temperature

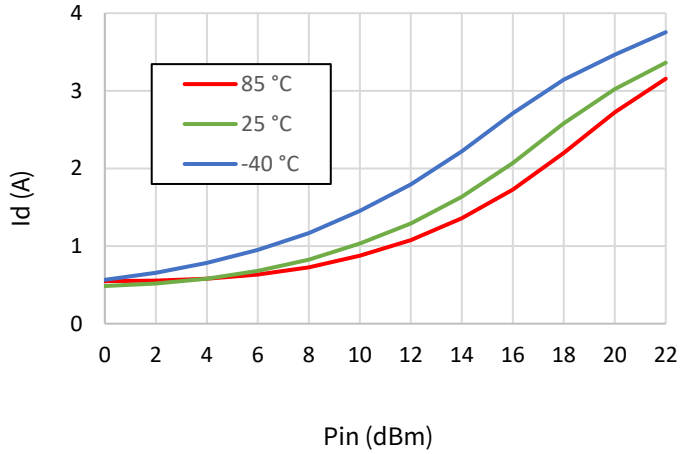


Figure 26: Ig v. Pin v. Temperature

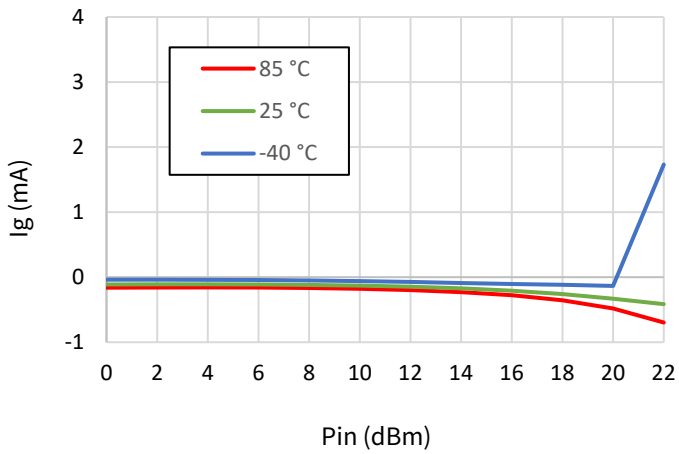
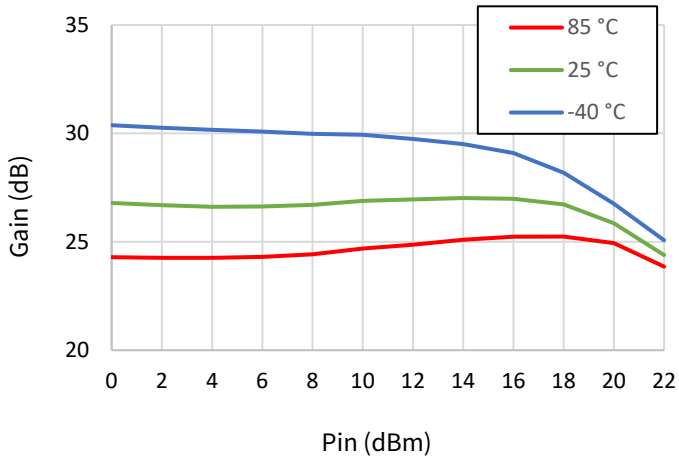


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 28: Pout v. Pin v. Vd

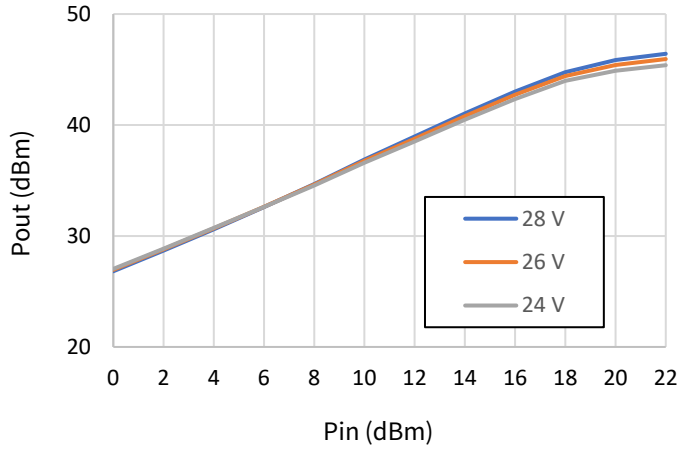


Figure 29: PAE v. Pin v. Vd

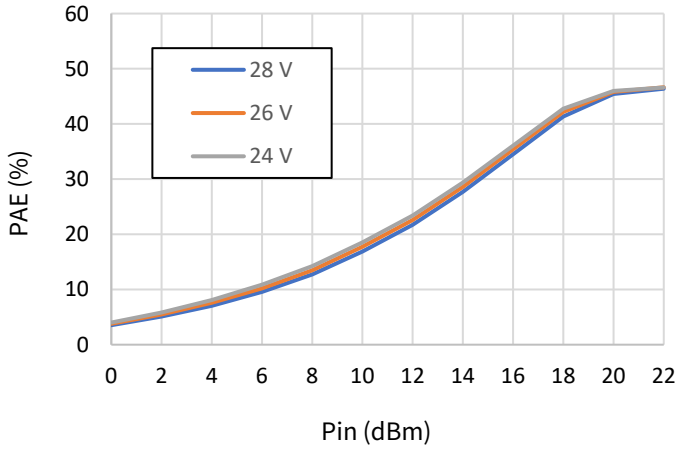


Figure 30: Id v. Pin v. Vd

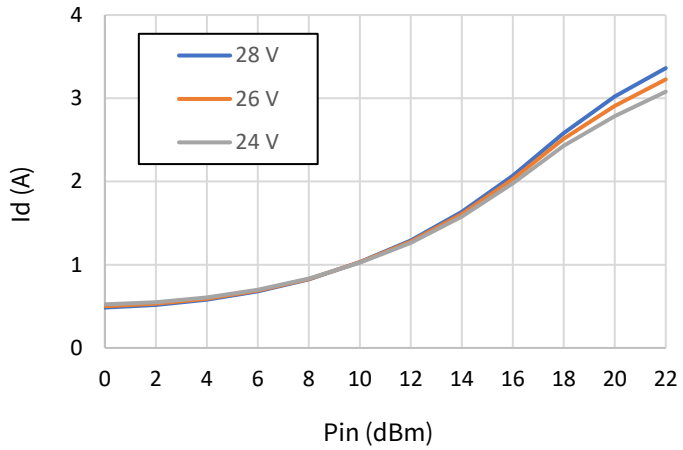


Figure 31: Ig v. Pin v. Vd

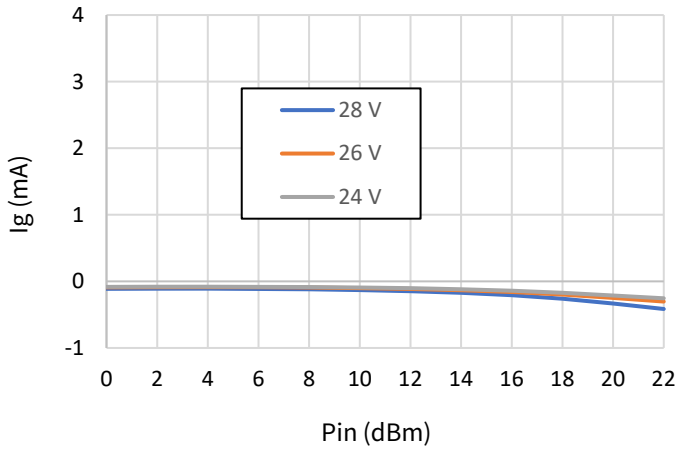
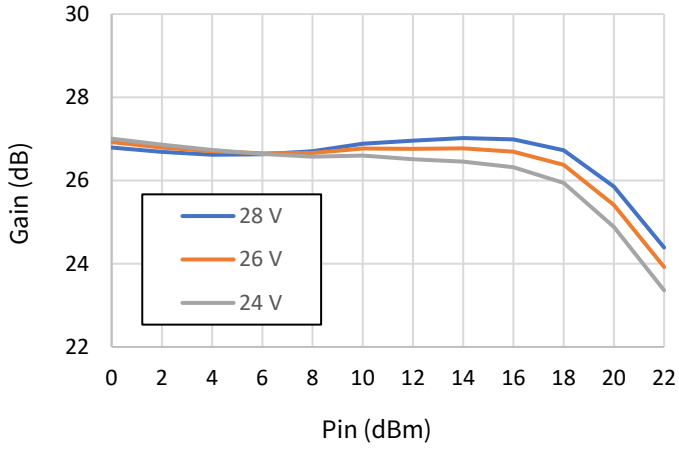


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 33: Pout v. Pin v. Idq

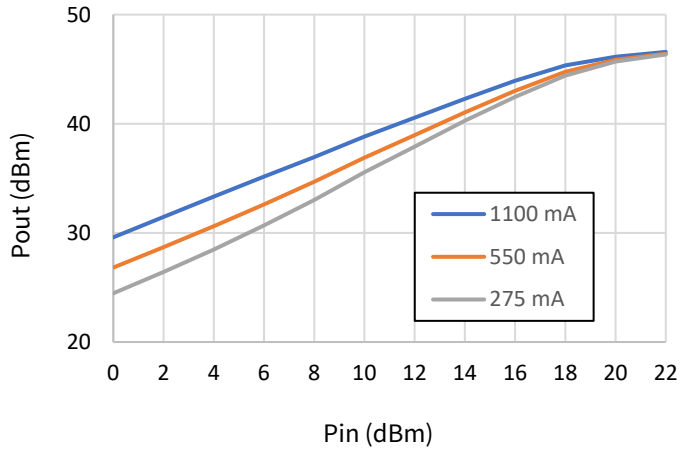


Figure 34: PAE v. Pin v. Idq

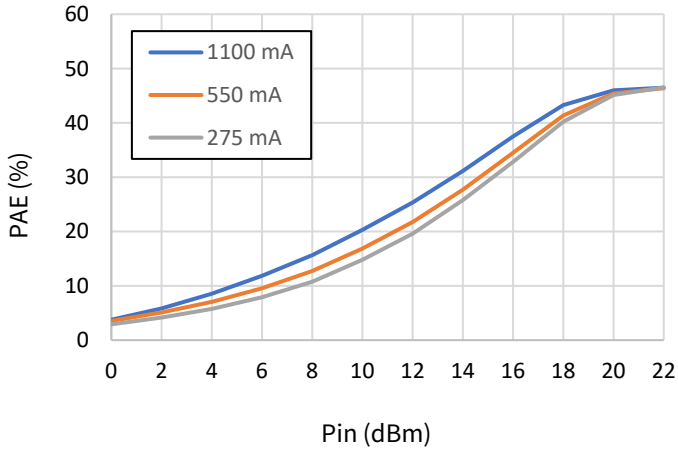


Figure 35: Id v. Pin v. Idq

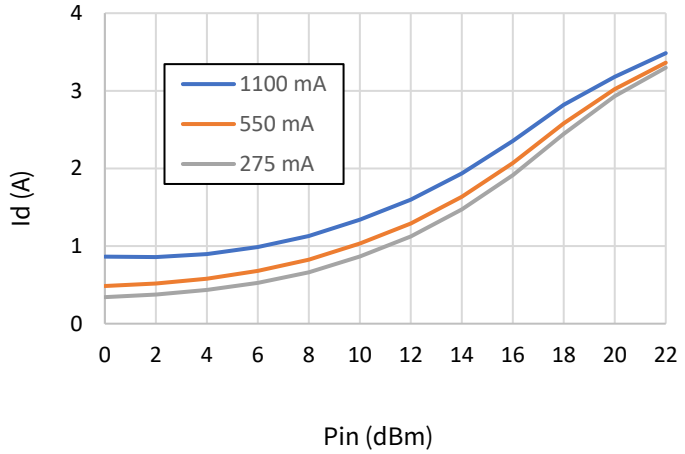


Figure 36: Ig v. Pin v. Idq

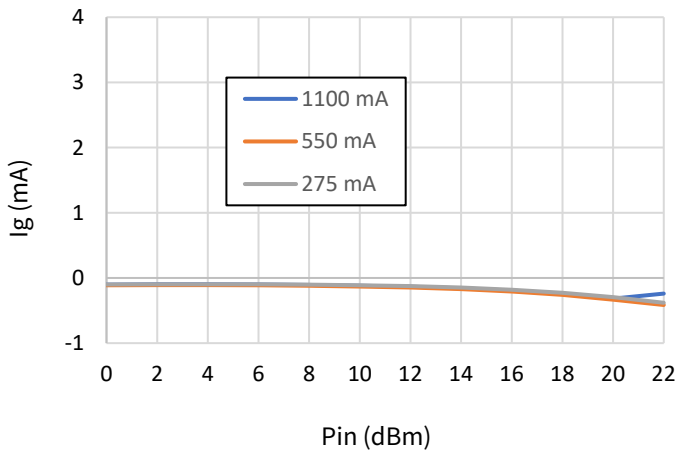
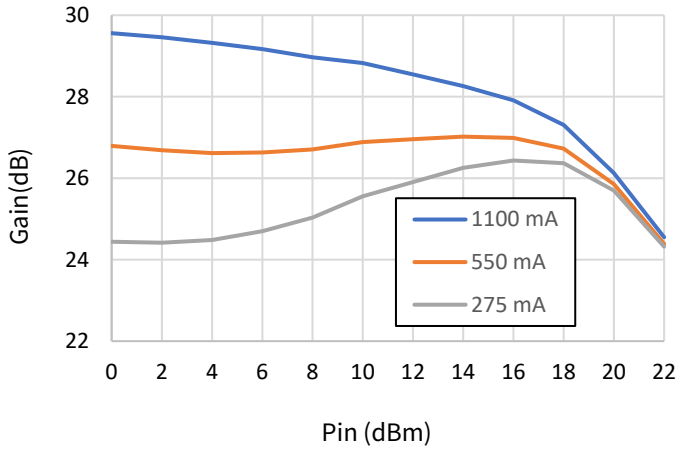


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = -20 dBm, T_{base}=25 °C

Figure 38: S21 v. Frequency v. Temperature

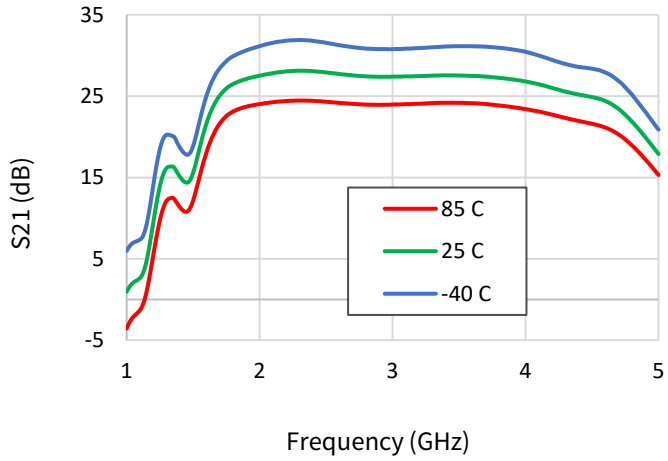


Figure 39: S21 v. Frequency v. Vd

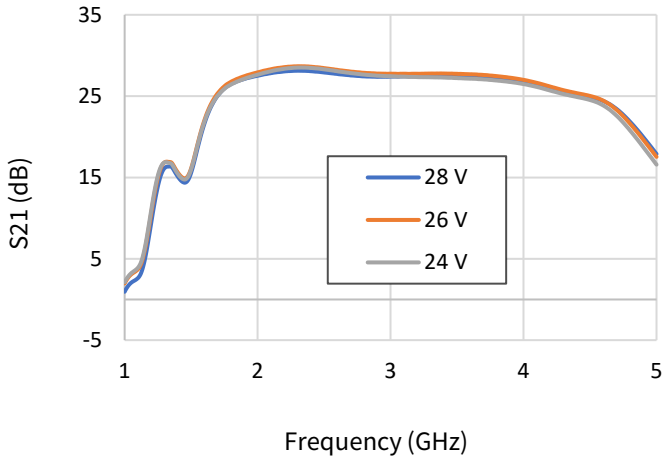


Figure 40: S11 v. Frequency v. Temperature

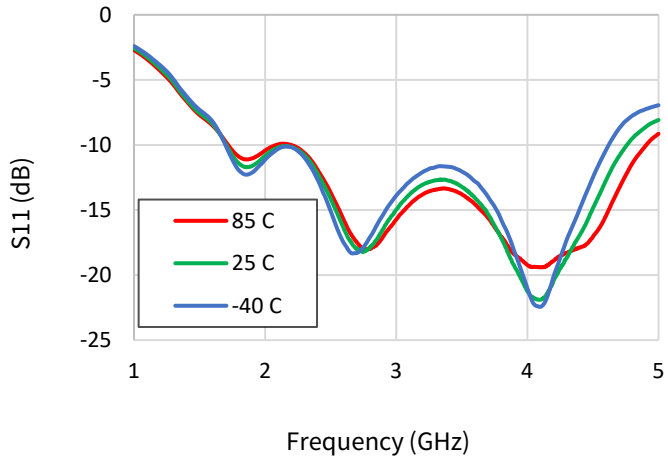


Figure 41: S11 v. Frequency v. Vd

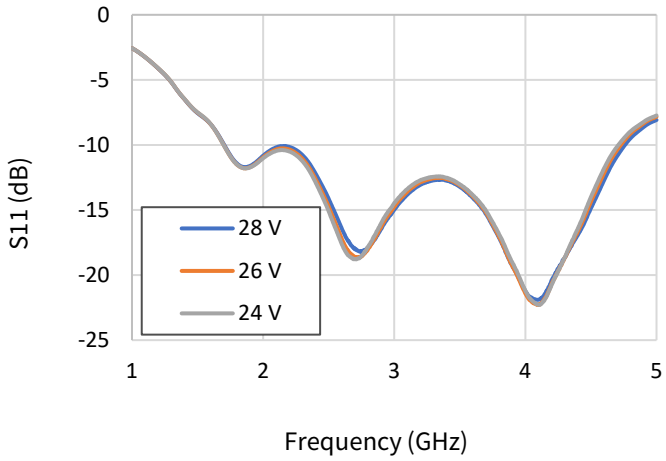


Figure 42: S22 v. Frequency v. Temperature

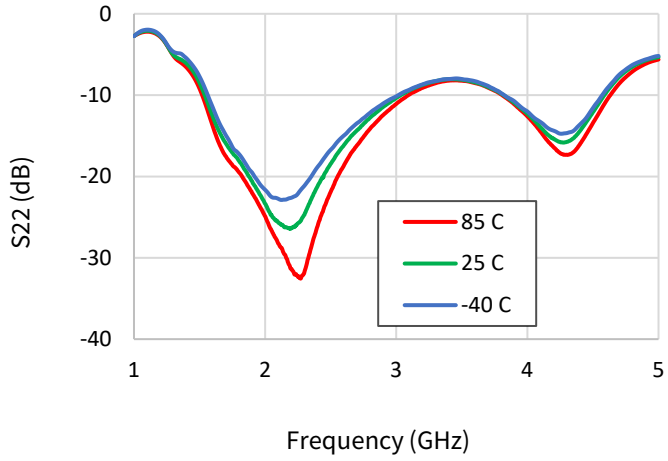
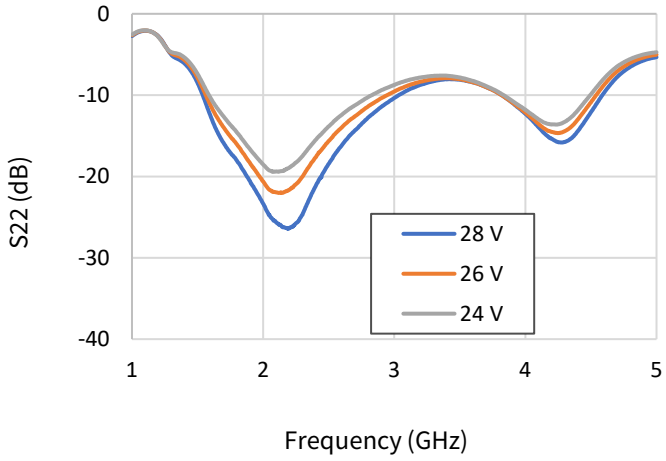


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = -20 dBm, T_{base}=25 °C

Figure 44: S21 v. Frequency v. Idq

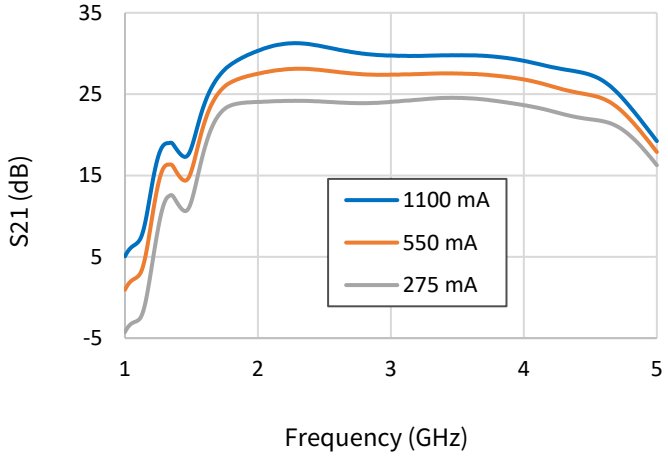


Figure 45: S11 v. Frequency v. Idq

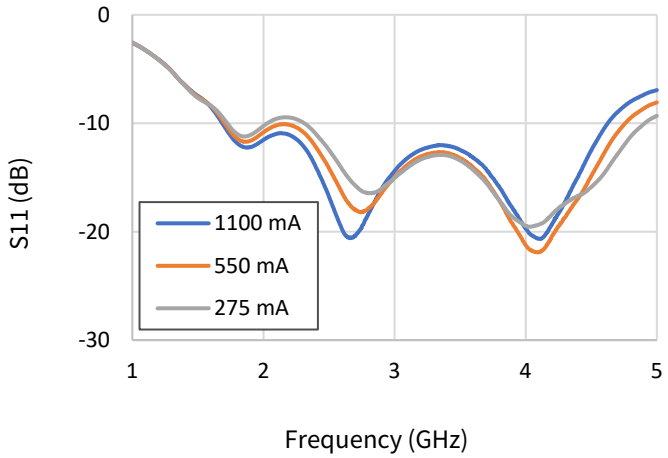
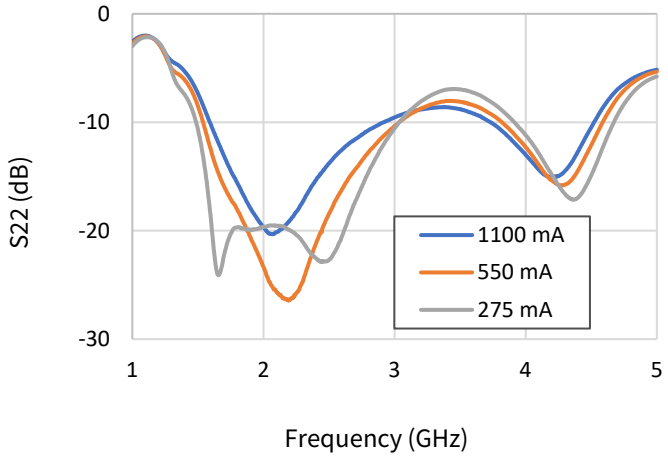


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=550mA, CW, Pin = 22 dBm, T_{base}=25 °C, Frequency: 3GHz

Figure 47: 2f v. Pout v. Temperature, 1.8 GHz

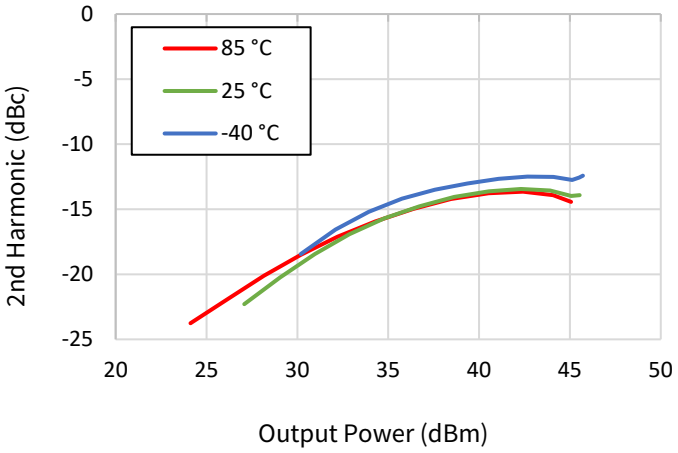


Figure 48: 2f v. Pout v. Vd, 1.8 GHz

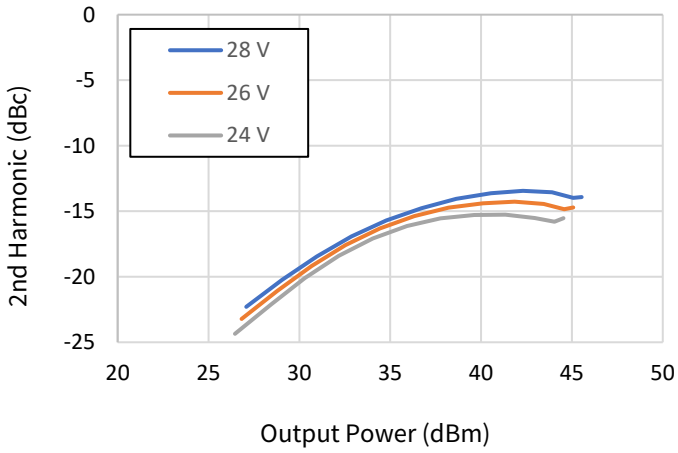


Figure 49: 2f v. Pout v. Temperature, 3.0 GHz

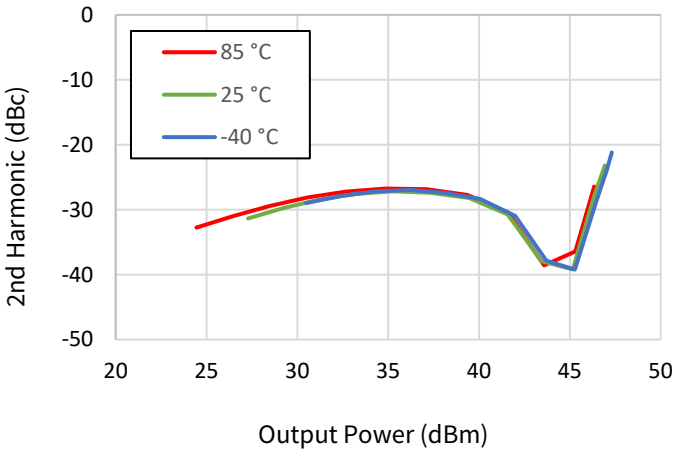


Figure 50: 2f v. Pout v. Vd, 3.0 GHz

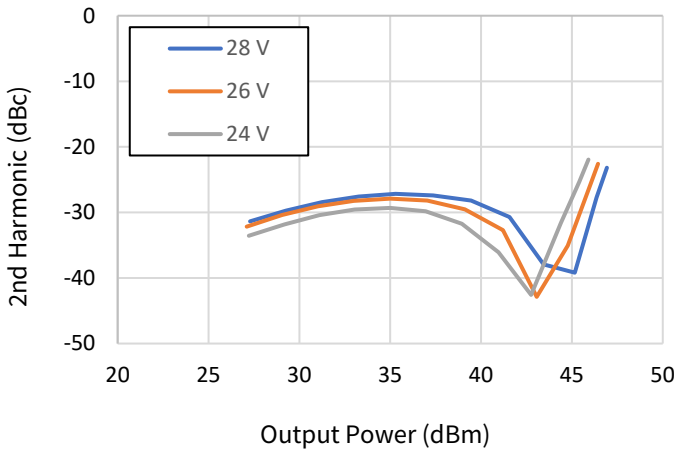


Figure 51: 2f v. Pout v. Temperature, 4.2 GHz

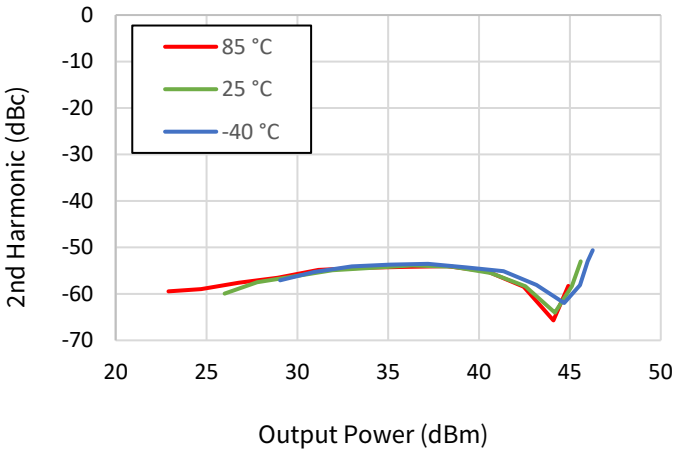
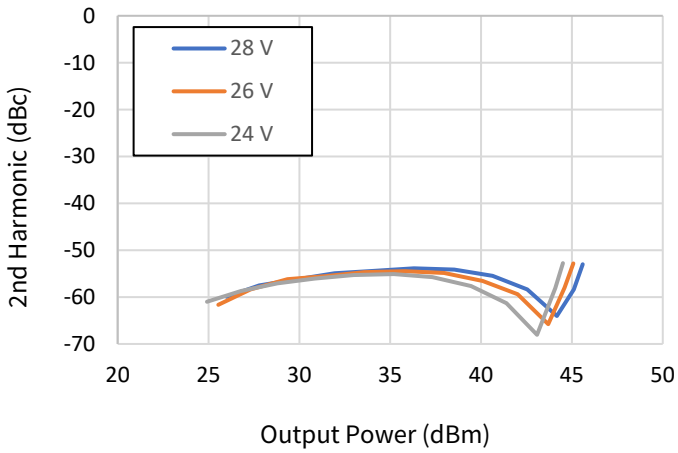


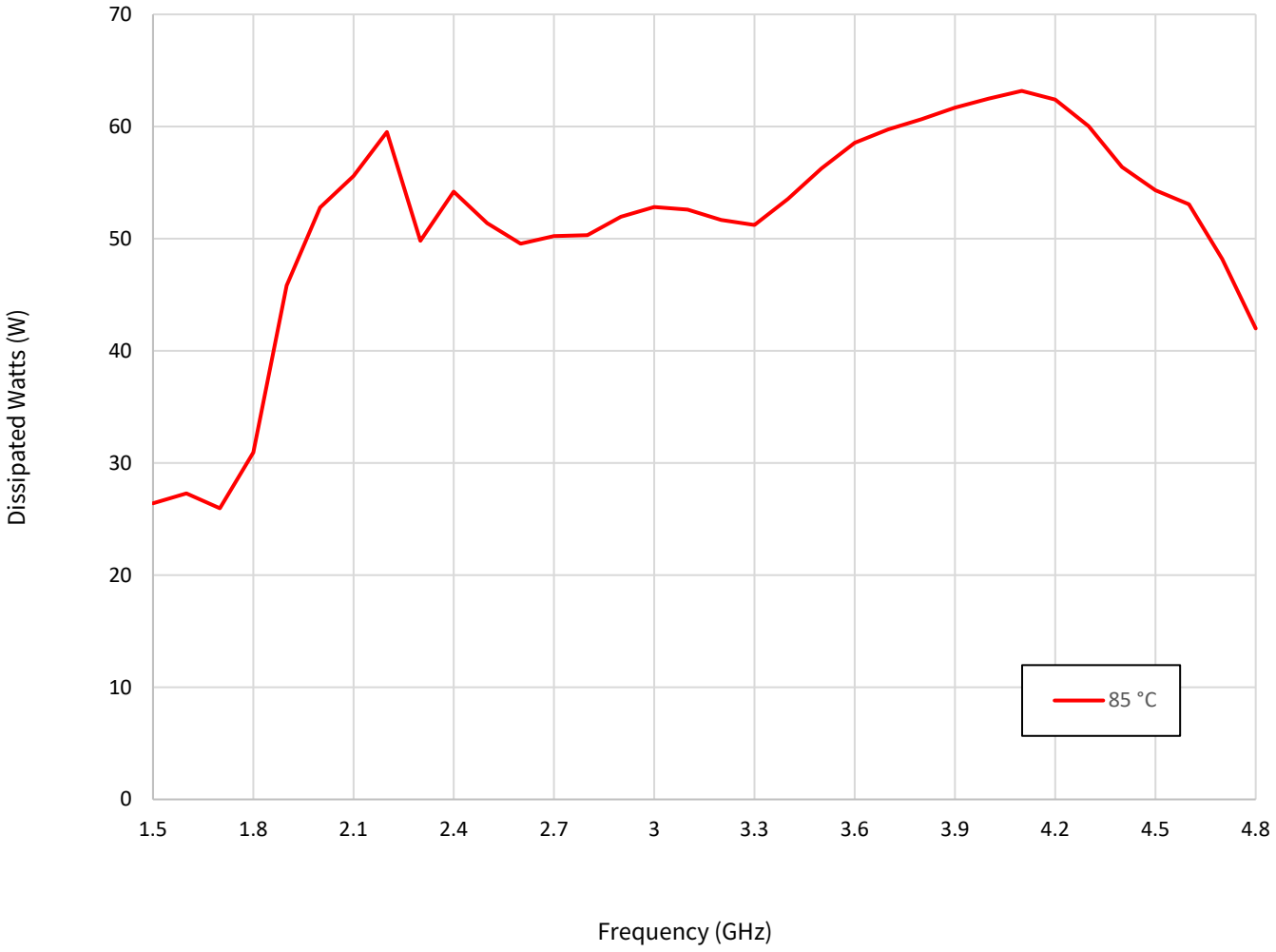
Figure 52: 2f v. Pout v. Vd, 4.2 GHz



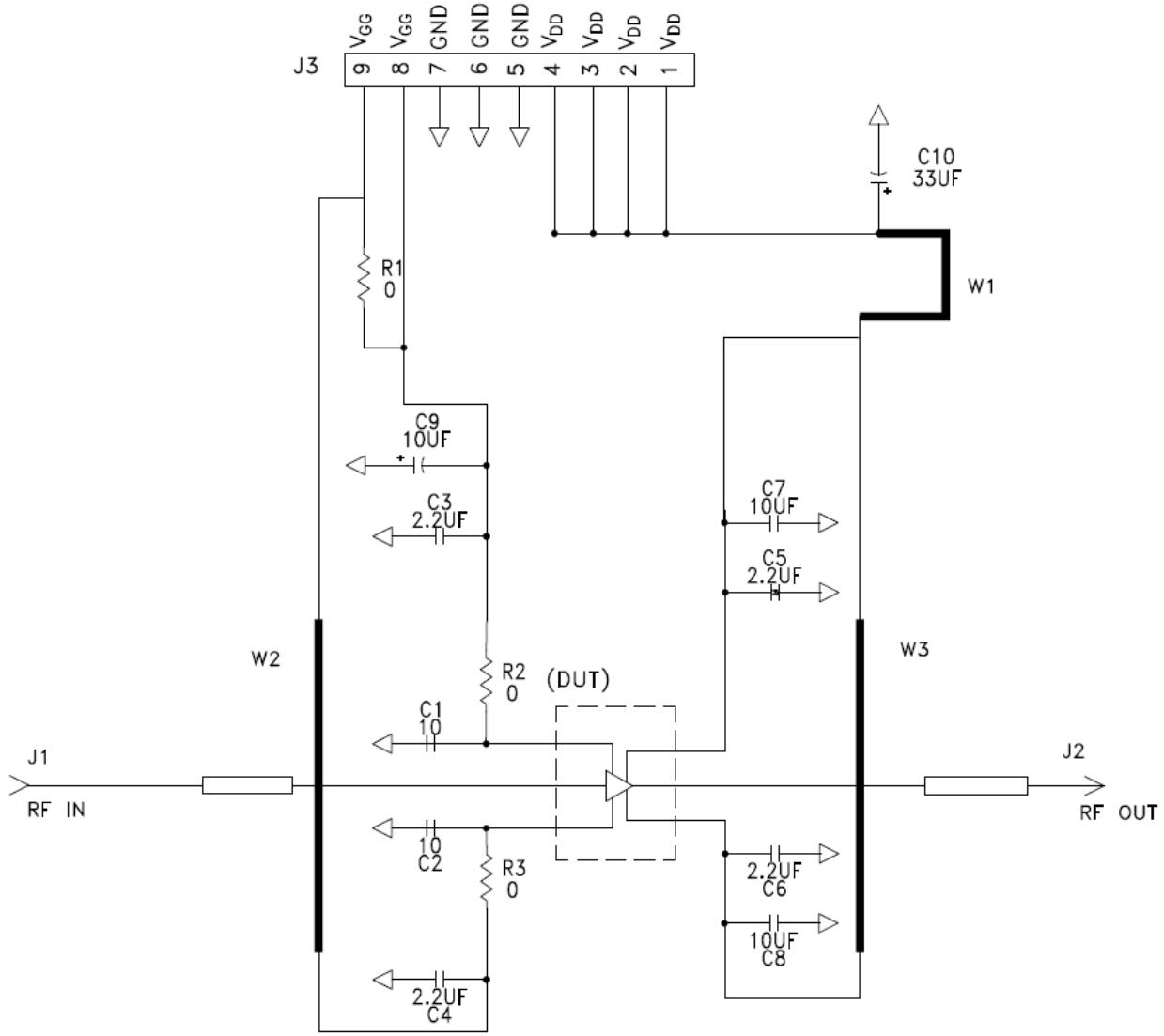
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	167.4°C	Freq = 3 GHz, V_d = 28 V, I_{dq} = 550 mA, I_{drive} = 3.1 A , P_{in} = 22 dBm, P_{out} = 45.12 dBm, P_{diss} = 54.3 W, T_{case} = 85°C, CW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8 °C/W	

Power Dissipation v. Frequency (Tcase = 85°C)



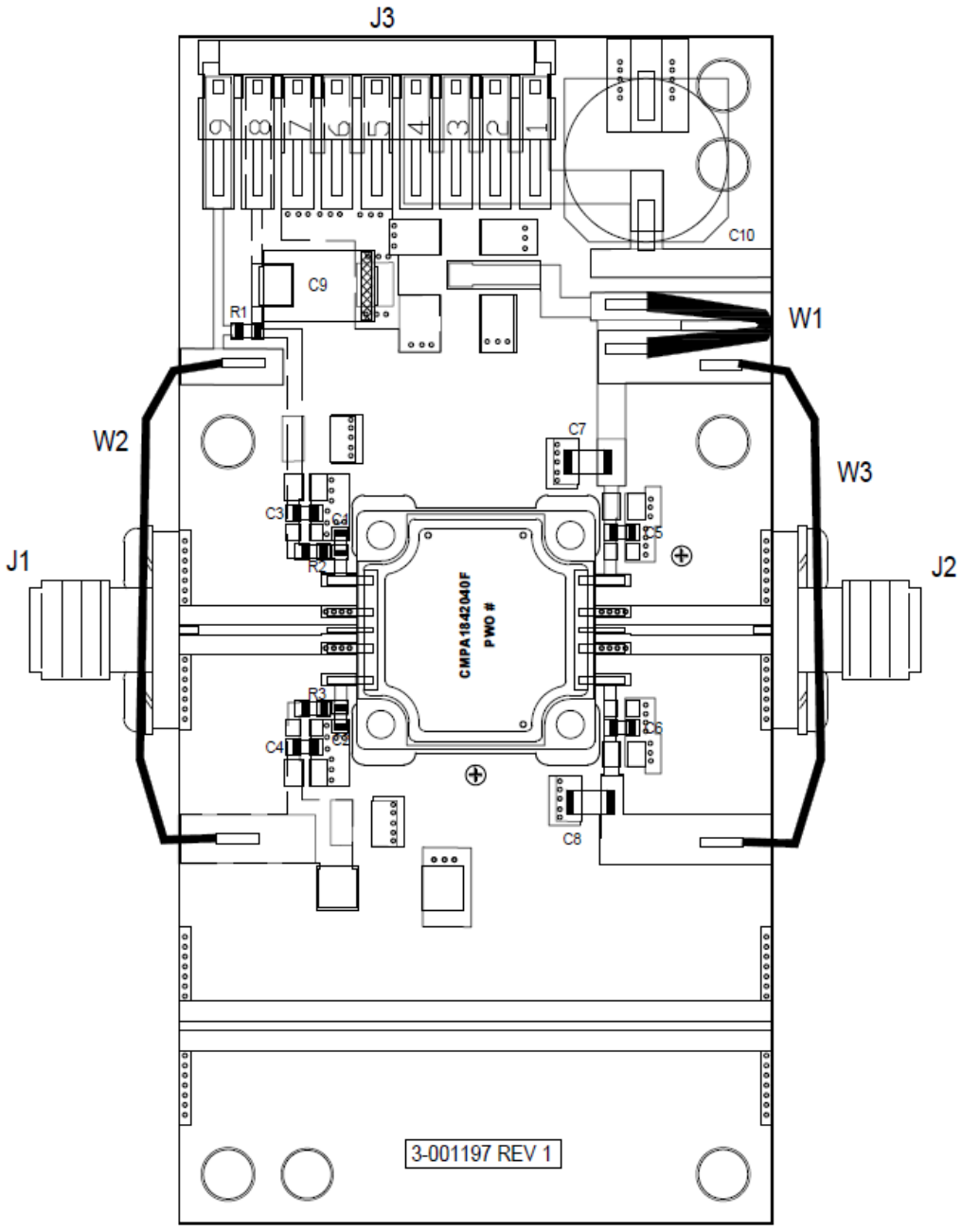
CMPA1842040F-AMP Evaluation Board Schematic Drawing



CMPA1842040F-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
R1,R2,R3	RES 0 Ohm, 0603	3
C1,C2	CAP, 10.0pF, +/-5%, 0603	2
C3,C4,C5,C6	CAP, 2.2UF, 50V, 0603	4
C7,C8	CAP, 10UF, 50V, 1206	2
C9	CAP 10UF 16V TANTALUM, 2312	1
C10	CAP, 33 UF, 20%, G CASE	1
J1,J2	SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
W1,W2,W3	WIRE	3
-	BASEPLATE, CU, 3.0 X 1.5 X 0.25 IN	1
-	EPOXY, ABLESTICK, CF 3350-004, 3x1.5	1
-	PCB 3.0” x 1.5” x 0.010” (RO3003, DK 3.0)	1

CMPA1842040F-AMP Evaluation Board Assembly Drawing



Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

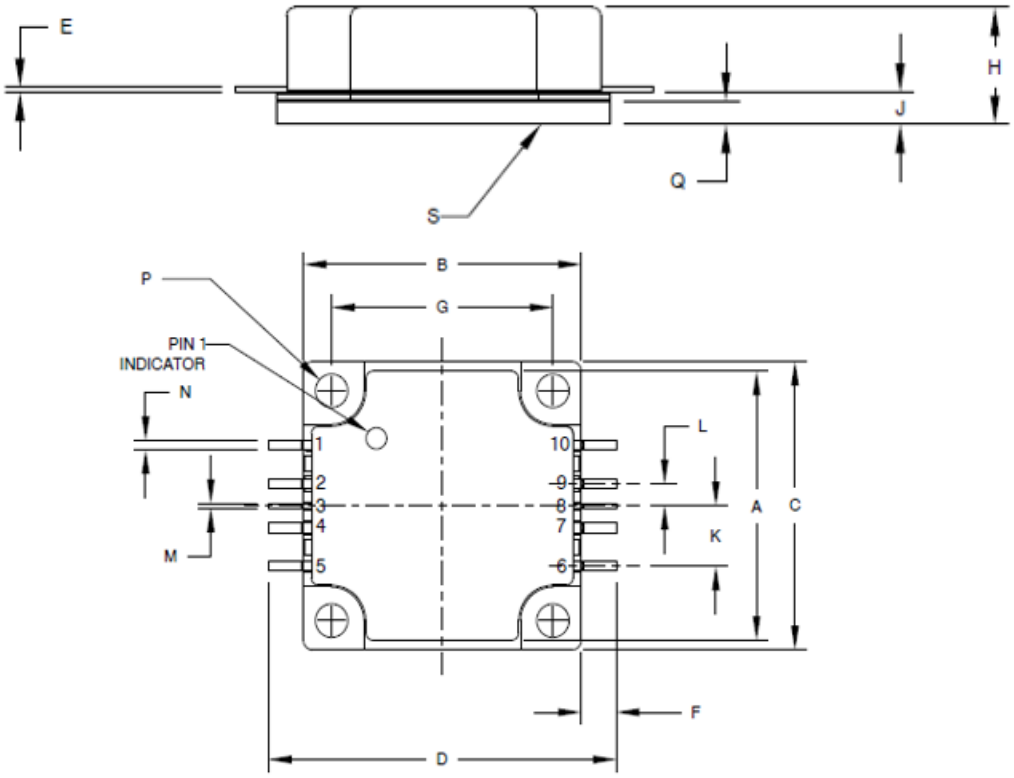
1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

Product Dimensions

DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.555	.560	.565	14.10	14.22	14.35
B	.595	.600	.605	15.11	15.24	15.37
C	.595	.600	.605	15.11	15.24	15.37
D	-	(.750)	-	-	(19.05)	-
E	.006	.008	.010	0.15	0.20	0.25
F	.065	.075	.085	1.66	1.91	2.16
G	.473	.478	.483	12.01	12.14	12.27
H	.191	.203	.215	4.86	5.16	5.46
J	.049	.056	.063	1.24	1.42	1.60
K	.121	.126	.131	3.07	3.20	3.33
L	.041	.046	.051	1.04	1.17	1.30
M	.005	.010	.015	0.13	.25	0.38
N	.015	.020	.025	0.38	.51	0.63
P	.065	.070	.075	1.65	1.78	1.90
Q	.038	.040	.042	0.97	1.02	1.07

NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. PINS:
   1 – 10 DEFINED BY PRODUCT
3. THE CONTENTS OF THIS DRAWING ARE INTENDED TO REPRESENT THE PRODUCT IN MARKETING GRAPHICS ONLY AND NOT INTENDED TO BE USED FOR ANY PRODUCTION OR INTERNAL QUALIFICATION PURPOSE.



PIN	DESC.	PIN	DESC.
1	VG	6	VD
2	GND	7	GND
3	RF IN (50Ω, DC Grounded)	8	RF OUT (50Ω)
4	GND	9	GND
5	VG	10	VD

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA1842040F	1.8 – 4.2 GHz, 45W GaN MMIC		
CMPA1842040F-AMP	Evaluation Board w/ PA	1 Each	

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