Phase Shifter, 6-Bit
6 - 18 GHz

CGY2392SUH/C1
Rev. V1

Features

- Insertion Loss: 10.8 dB @ 12 GHz
- Phase Shift Range: 360°
- RMS Phase Error: 1.7° @ 12 GHz
- RMS Amplitude Variation: 0.45 dB @ 12 GHz
- Input Return Loss: 12 dB
- Output Return Loss: 14 dB
- 0 / +5 V Control Lines
- Chip Size: 3500 x 3200 µm
- Tested, Inspected Known Good Die (KGD)
- Space and MIL-STD Available
- RoHS* Compliant

Applications

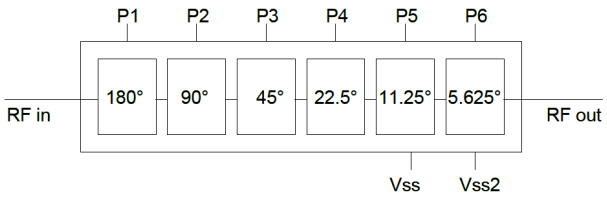
- Radar
- Telecommunication
- Instrumentation

Description

The CGY2392SUH/C1 is a high performance GaAs MMIC 6-Bit phase shifter operating from 6 - 18 GHz. This device has a nominal phase shifting range of 0 - 360° in 5.625° steps and has a low RMS Phase Error. It is part of a new 6 - 18 GHz chipset that is dedicated to Radar, Telecommunication and Instrumentation applications.

The die is manufactured using 0.18 µm gate length pHEMT process. The MMIC uses gold bonding pads, backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2392SUH/C1	DIE

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Measured On Wafer, Freq. = 6 - 18 GHz, V_{SS2} = -4.5 V, I_{SS2} = 8 mA, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	—	dB	—	10.7	—
Phase Range	—	°	—	360	—
Input Return Loss	@ RFIN	dB	—	15	—
Output Return Loss	@ RFOUT	dB	—	15	—
RMS Phase Error	—	°	—	2.5	—
RMS Attenuation Error	—	dB	—	0.5	—

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Phase Control Inputs	0 to +5.5 V
Source Supply Voltage When VSS2 pad is not used When VSS1 pad is not used	 -5.0 to +0.5 -6.0 to +0.5
Input Power	TBD dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Logic Truth Table (1/2)

Nominal Phase Shift	P1	P2	P3	P4	P5	P6
	180°	90°	45°	-22.5°	11.25°	5.625°
Reference State	0	0	0	0	0	0
Phase Shift Activated	1	1	1	1	1	1

Logic Truth Table (V)

Phase Shift (°)	P1	P2	P3	P4	P5	P6
	180°	90°	45°	-22.5°	11.25°	5.625°
0	0	0	0	0	0	0
5.625	0	0	0	0	0	1
11.25	0	0	0	0	1	0
16.875	0	0	0	0	1	1
22.5	0	0	0	1	0	0
28.125	0	0	0	1	0	1
33.75	0	0	0	1	1	0
39.375	0	0	0	1	1	1
45	0	0	1	0	0	0
50.625	0	0	1	0	0	1
56.25	0	0	1	0	1	0
61.875	0	0	1	0	1	1
67.5	0	0	1	1	0	0
73.125	0	0	1	1	0	1
78.75	0	0	1	1	1	0
84.375	0	0	1	1	1	1
90	0	1	0	0	0	0
95.625	0	1	0	0	0	1
101.25	0	1	0	0	1	0
106.875	0	1	0	0	1	1
112.5	0	1	0	1	0	0
118.125	0	1	0	1	0	1
123.75	0	1	0	1	1	0
129.375	0	1	0	1	1	1
135	0	1	1	0	0	0
140.625	0	1	1	0	0	1
146.25	0	1	1	0	1	0
151.875	0	1	1	0	1	1
157.5	0	1	1	1	0	0
163.125	0	1	1	1	0	1
168.75	0	1	1	1	1	0
174.375	0	1	1	1	1	1
180	1	0	0	0	0	0

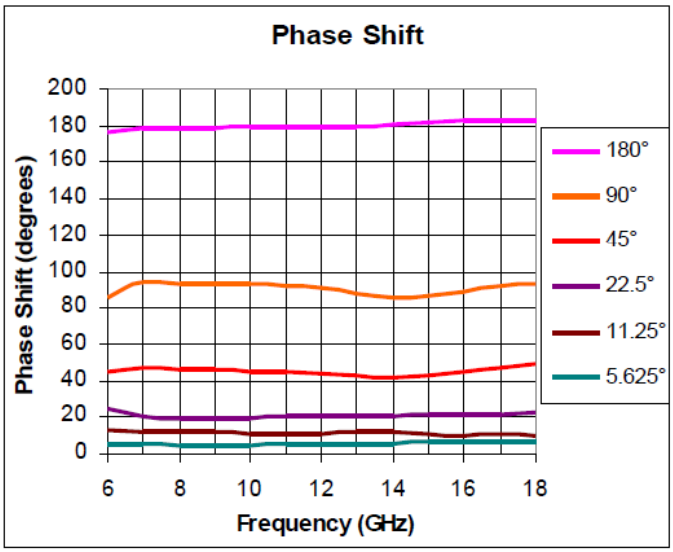
Logic Truth Table (2/2)

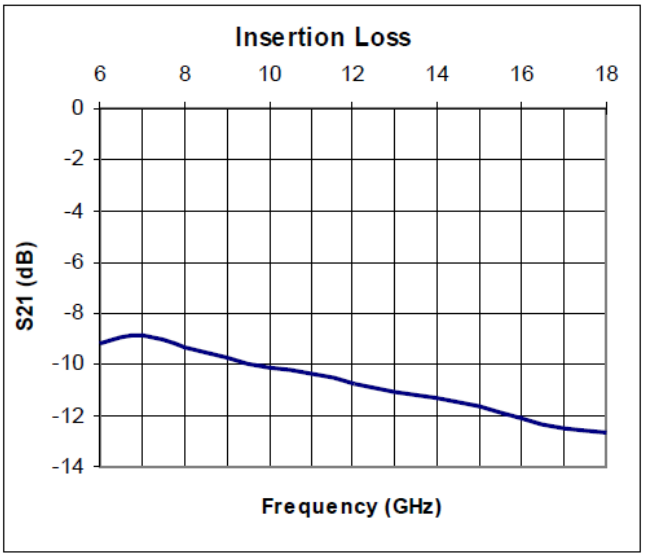
Phase Shift (°)	P1	P2	P3	P4	P5	P6
	180°	90°	45°	-22.5°	11.25°	5.625°
185.625	1	0	0	0	0	1
191.25	1	0	0	0	1	0
198.875	1	0	0	0	1	1
202.5	1	0	0	1	0	0
208.125	1	0	0	1	0	1
213.75	1	0	0	1	1	0
219.375	1	0	0	1	1	1
225	1	0	1	0	0	0
230.625	1	0	1	0	0	1
236.25	1	0	1	0	1	0
241.875	1	0	1	0	1	1
247.5	1	0	1	1	0	0
253.125	1	0	1	1	0	1
258.75	1	0	1	1	1	0
264.375	1	0	1	1	1	1
270	1	1	0	0	0	0
275.625	1	1	0	0	0	1
281.25	1	1	0	0	1	0
286.875	1	1	0	0	1	1
292.5	1	1	0	1	0	0
298.125	1	1	0	1	0	1
303.75	1	1	0	1	1	0
309.375	1	1	0	1	1	1
315	1	1	1	0	0	0
320.625	1	1	1	0	0	1
326.25	1	1	1	0	1	0
331.875	1	1	1	0	1	1
337.5	1	1	1	1	0	0
343.125	1	1	1	1	0	1
348.75	1	1	1	1	1	0
354.375	1	1	1	1	1	1

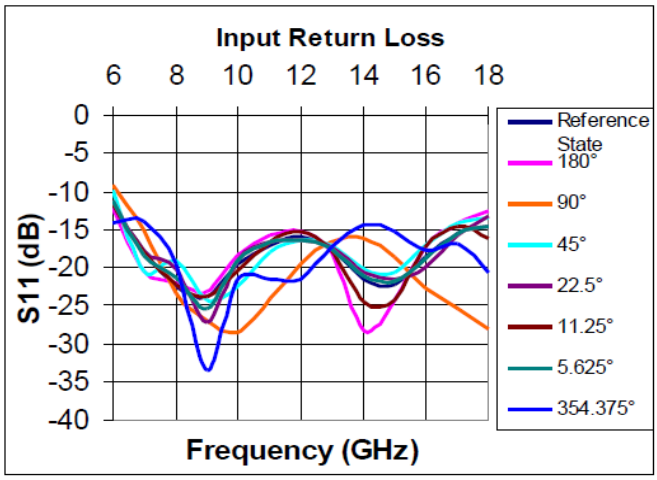
Control Voltage

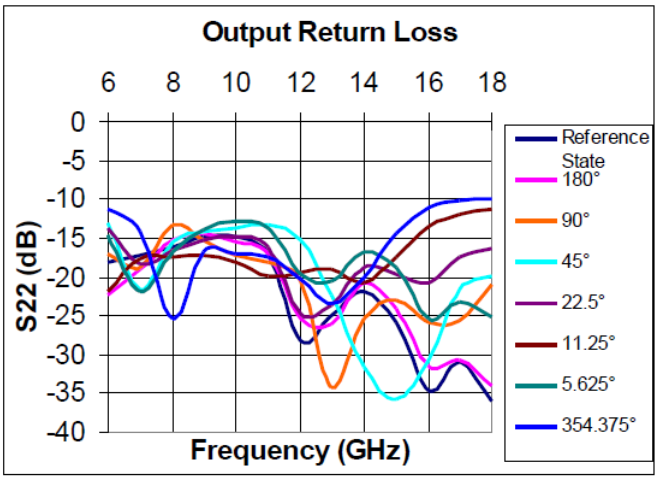
State	Min.	Max.	Unit
Low (0)	0	1	V
High (1)	4	6	V

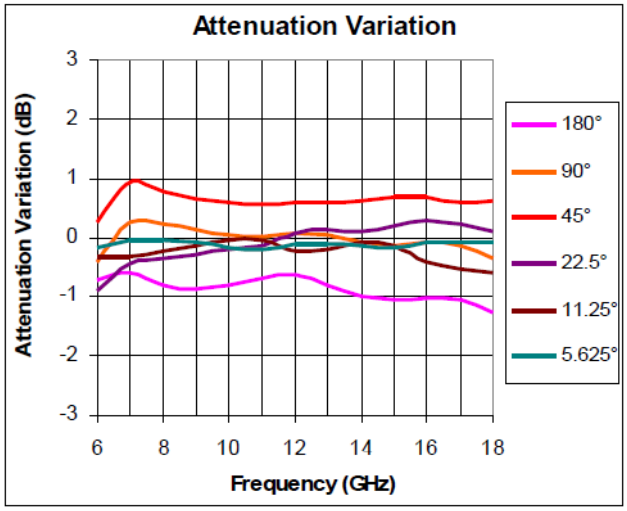
Typical Performance Curves: S-Parameters, On Wafer, V_{SS2} = -5 V



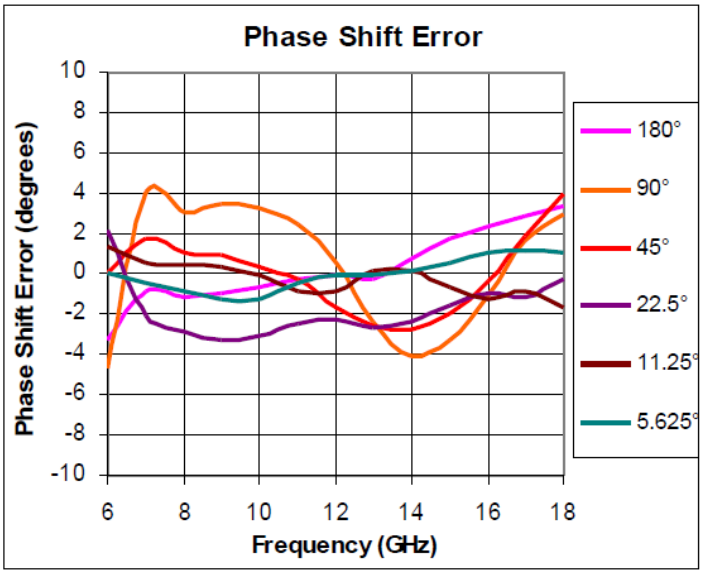


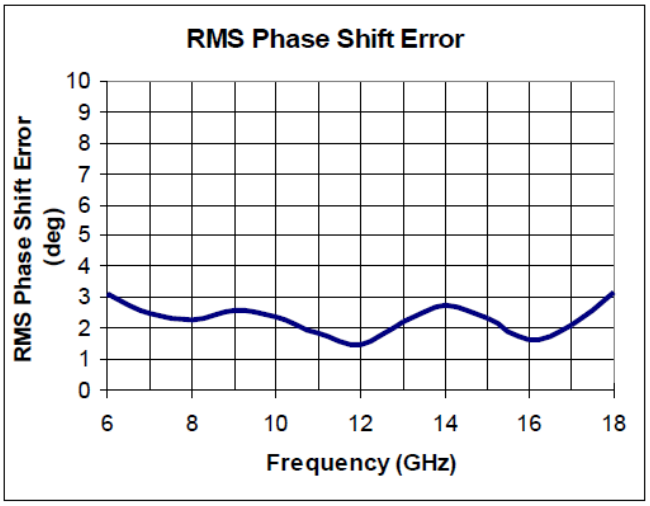


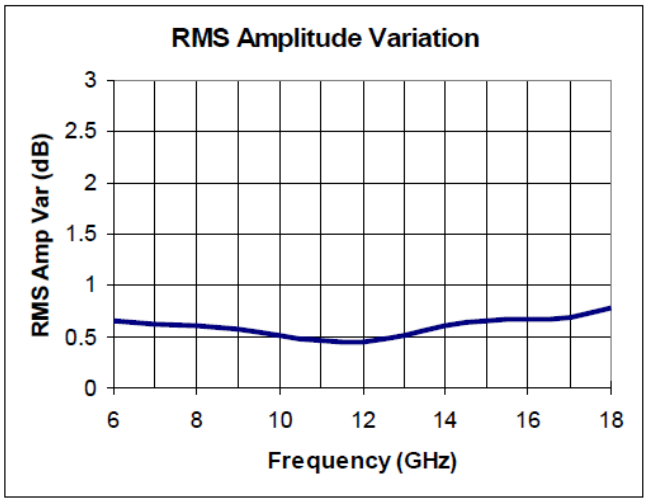




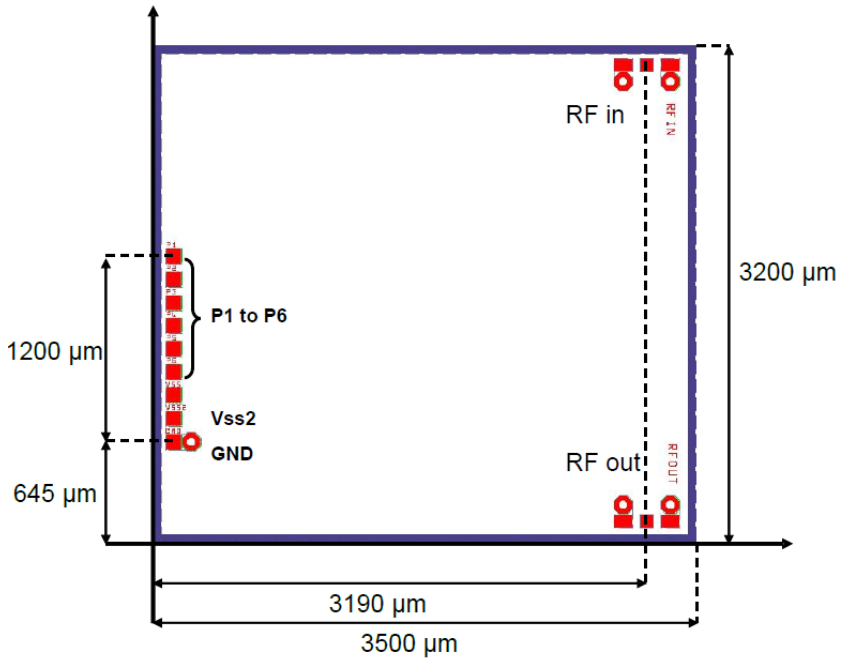
Typical Performance Curves: Phase Shifting / Attenuation Errors, VSS@ = -4.5 V, calculated with input/Output Inductance of 0.5 nH







Mechanical Information:



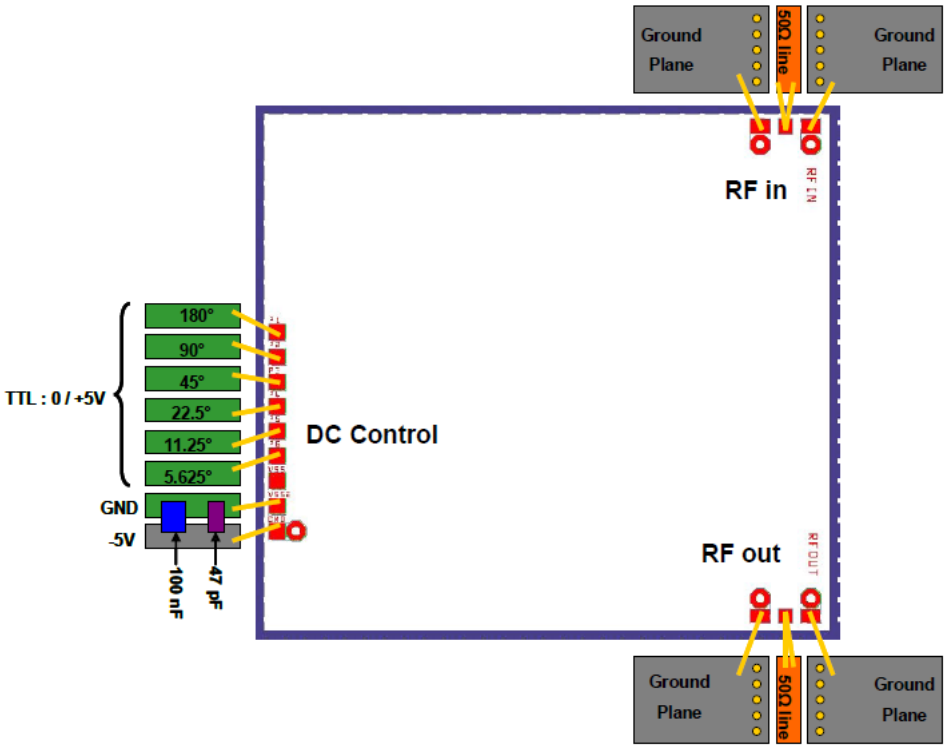
Chip Size = 3500 x 3200 µm (including the dicing street)
DC Pads = 100 x 100 µm, spacing = 150 µm, top metal = Au
RF Pads = 100 x 100 µm, pitch = 150 µm, top metal = Au
Chip Thickness = 100 µm

Pad Position[4,5]

Pad Name	Symbol	Coordinate		Description
		X	Y	
GND	DC Control	130	645	Ground (connected to MMIC back side metal)
VSS2		130	795	VSS2 power supply
VSS		130	945	VSS1 power supply
P6		130	1095	5.625° cell control
P5		130	1245	11.25° cell control
P4		130	1395	22.5° cell control
P3		130	1545	45° cell control
P2		130	1695	90° cell control
P1		130	1845	180° cell control
GND	RFIN	3040	3080	Ground (connected to MMIC back side metal)
RFIN		3190	3080	RF Input Port
GND		3340	3080	Ground (connected to MMIC back side metal)
GND	RFOUT	3040	130	Ground (connected to MMIC back side metal)
RFOUT		3190	130	RF Output Port
GND		3340	130	Ground (connected to MMIC back side metal)

4. X=0, Y=0 at bottom left corner. See Mechanical Information for more details.
5. Only V_{SS} or V_{SS2} is to be connected. For example: if V_{SS2} is used, V_{SS} must be left open.

Bonding Diagram & Assembly Information:



The RF interfacing bond wires or ribbon should be kept as short as possible.

The RF lines should be 300 µm wide or less to minimize discontinuities associated with the connection to the MMIC bond pads.

The power supply (VSS or VSS2) must be decoupled to the ground with capacitors as close as possible to the chip.

Decoupling Parts List

Part	V_{SS2} (or V_{SS})
Chip SMD capacitor 1	47 pF or 100 pF
Chip SMD capacitor 2	100 nF