Ka-Band Core Chip
26.5 - 30.5 GHz

CGY2351UH/C1
Rev. V1

Features

- Phase Shifter 6 bits: 360° max with 5.625° step
- Attenuation 5 bits: 22 dB max. 0.7 dB step
- RMS Phase Error: 4° all states
- RMS Amplitude Error: 0.5 dB all states
- Input Return Loss Matching: 14 dB
- Output Return Loss Matching: 13 dB
- Supply Voltage: +5 V & -5 V
- Total Current Consumption: 17 mA
- Chip Size: 4800 x 1600 µm
- Tested, Inspected Known Good Die (KGD)
- RoHS* Compliant

Applications

- Radar, Antennas
- Telecommunication
- Instrumentation

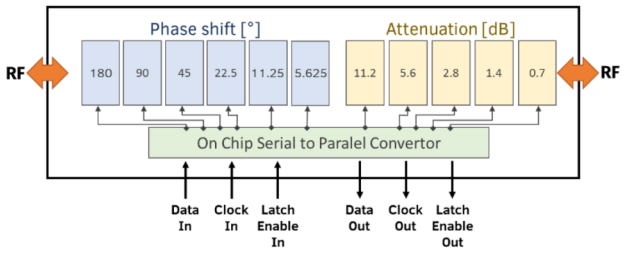
Description

The CGY2351UH/C1 is a high performance GaAs MMIC core chip operating in Ka-band. It follows the T/R architecture, is passive, and exhibits only 2 RF ports. It includes a 6-bit phase shifter and a 5-bits attenuator; it has a phase shift range of 360° with a 5.62° step and attenuation range of 22 dB with 0.7 dB step. It operate from 26.5 to 30.5 GHz.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using 0.18 µm gate length ED02AH pHEMT Technology. The MMIC uses gold bond pads and backside metallization. It is fully protected by a Silicon Nitride passivation layer to obtain the highest level of reliability. This technology has been evaluated for Space applications by the European Space Agency (ESA) and is on the European Preferred Parts List of ESA.

Block Diagram



Ordering Information

Part Number	Package
CGY2351UH/C1	On wafer measured die
CGY2351UH/C1/EK	Evaluation Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 26.5 - 30.5 GHz, V_{DN} = +5 V, V_{SN} = -5 V, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	—	dB	-17	-15	-13
Input Return Loss	—	dB	—	-14	-12
Output Return Loss	—	dB	—	-14	-12
Phase Shift Range	—	°	—	360	—
Phase Shift Step	—	°	—	5.625	—
Phase Shift RMS Error	27.5 GHz à 30 GHz	°	2	4	6
Attenuation Range	—	dB	—	21.7	—
Attenuation RMS Step	27.5 GHz à 30 GHz	dB	—	0.5	1.2
Input P1dB	VL = -2 V, all attenuation & phase shifter off	dBm	20.5	—	—
RMS Attenuation Error	Rx Mode Tx Mode	dB	—	0.2 0.5	0.4 0.6
Noise Figure	—	dB	—	5	6
Power Consumption	Rx Mode Tx Mode	mW	—	180 205	—
Input P1dB	Tx Mode	dBm	10.0	11.5	12.0

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Control I/O Pins Voltage VDN VSN	 0 V to +5.5 V -5.5 V to 0 V
Supply Voltage Positive Negative	 0 V to +5.5 V -5.5 V to -4.5 V
Supply Current Positive Negative	 3 - 8 mA 10 - 15 mA
Total Drain Current	100 mA
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

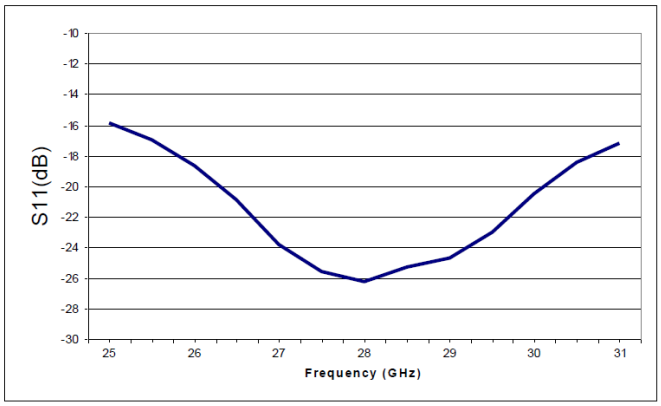
Handling Procedures

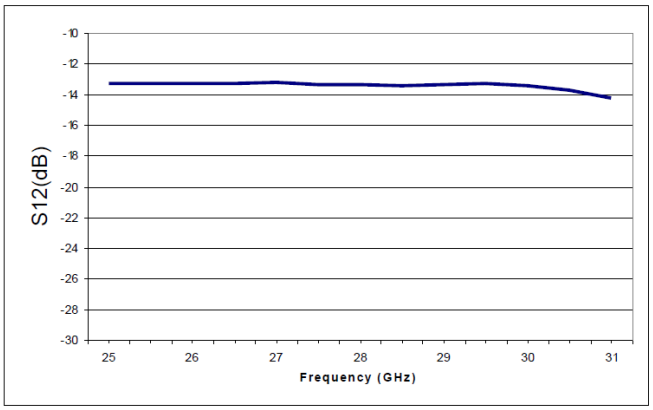
Please observe the following precautions to avoid damage:

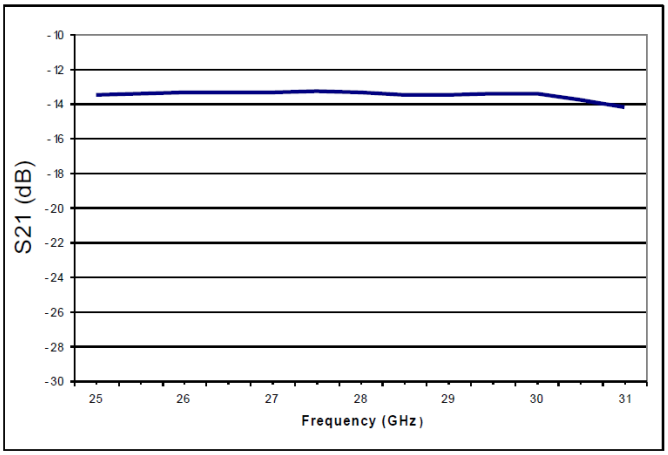
Static Sensitivity

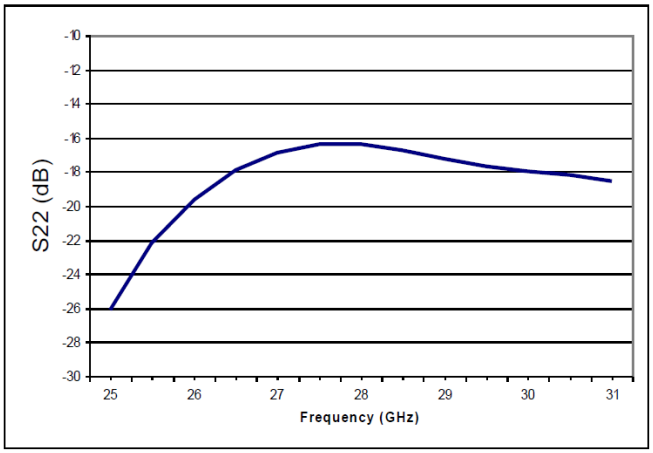
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: On Wafer Measurements









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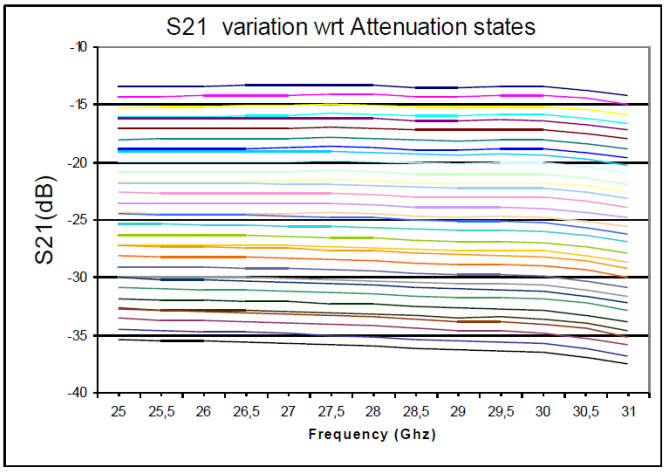
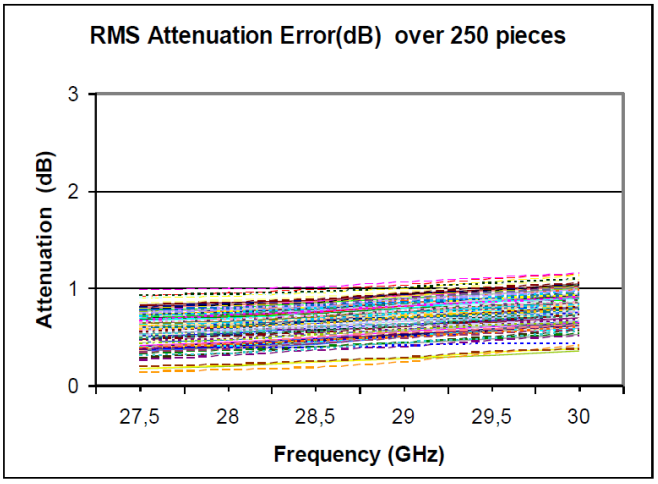
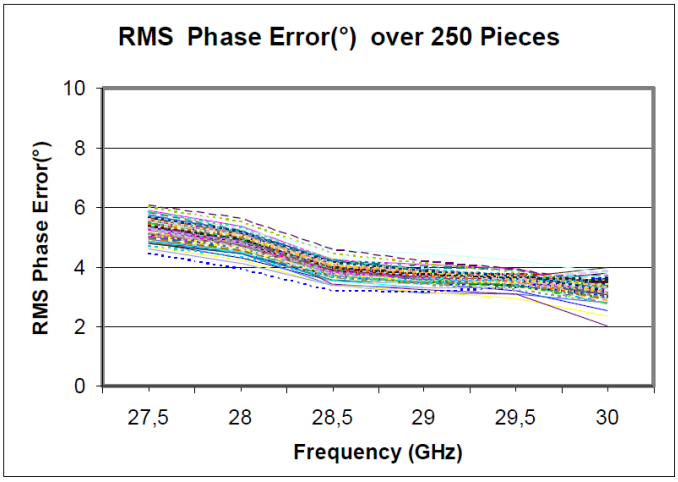


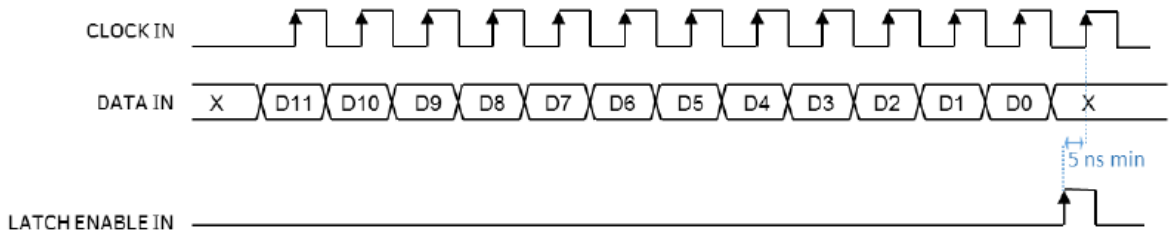




Bit Allocation

Bit #	Description	Theoretical Value
D0	Phase State Control	180°
D1		90°
D2		45°
D3		22.5°
D4		11.3°
D5		5.625°
D6	Attenuation State Control	-11.2 dB
D7		-5.6 dB
D8		-2.8 dB
D9		-1.4 dB
D10		-0.7 dB
D11	Enable Change on Latch Enable Pulse	0 / 1

Timing Diagram



Control Interface timing diagram

Data In is sampled at the rising edge of the *Clock In* signal.
Rising edge of LEI (Latch Enable In) must occur after all 12 bits are loaded.
Data In is transferred to the operating register (and Attenuator/Phase Shifter settings are changed) on the rising edge of *Latch Enable In* hardware line if the D11 bit (the first one to be sent) is equal to 1.

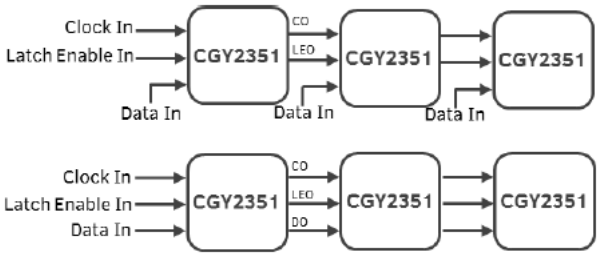
The Clock defines the speed of changing Attenuator/Phase Shift setting, the setting could be changed in 600 ns (if 20 MHz Clock) or 54 ns (if 240 MHz Clock).

In order to simplify the control of multiple devices using the same bit stream and to improve the resistance of the control to glitches, an additional control bit has been implemented in the control bit stream.

Bit D11 is a change enabled bit; the state of the CGY2351UH/C1 device can be changed only when D11=1 and the Latch Enable (In) hardware line is toggled (c.f. figure 1).

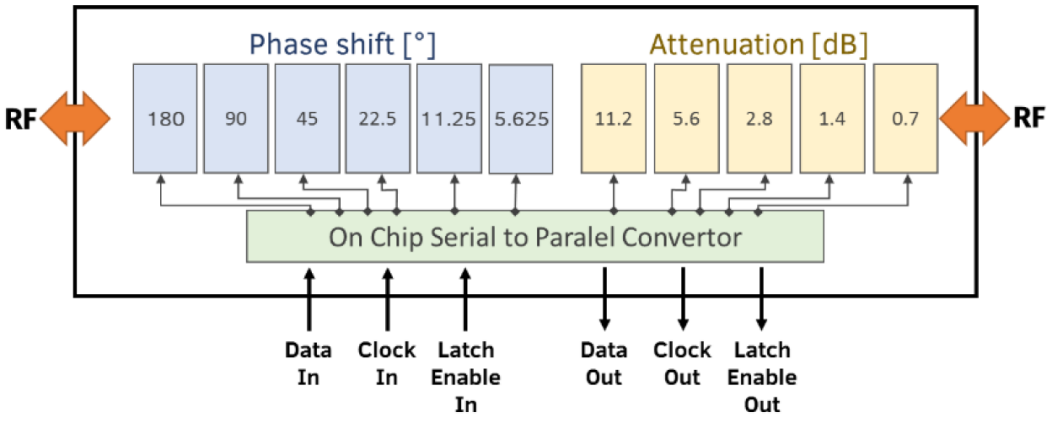
Setup and hold times should be greater than **5 ns**:
-For DI and LEI with respect to CI rising edge
-For LEI with respect to CI falling edge

In order to reduce wiring volume and weight in user application, the user could use multiple devices in a cascaded architecture as shown in the figure below.



Examples of Cascaded Core Chips

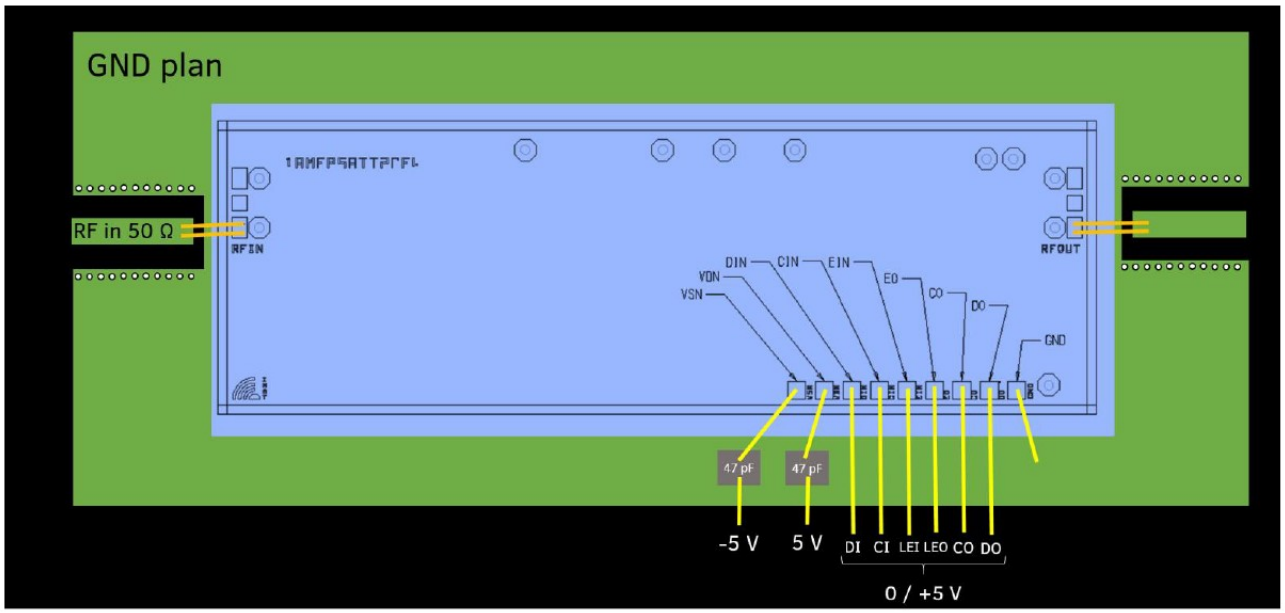
Block Diagram



Pin Configuration

Symbol	Description	Description
RF1	RFOUT	RF Port 1 (device is bidirectional)
RF2	RFIN	RF Port 2 (device is bidirectional)
VDN	VDD	Positive Supply Pad
VSN	VSN	Negative Supply Pad
DIN, CIN, EIN	DIN, CIN, EIN	SIPO Input (Data, Clock, Latch Enable)
DO, CO, EO	DO, CO, EO	SIPO Output (Data, Clock, Latch Enable)
GND	Backside	Ground

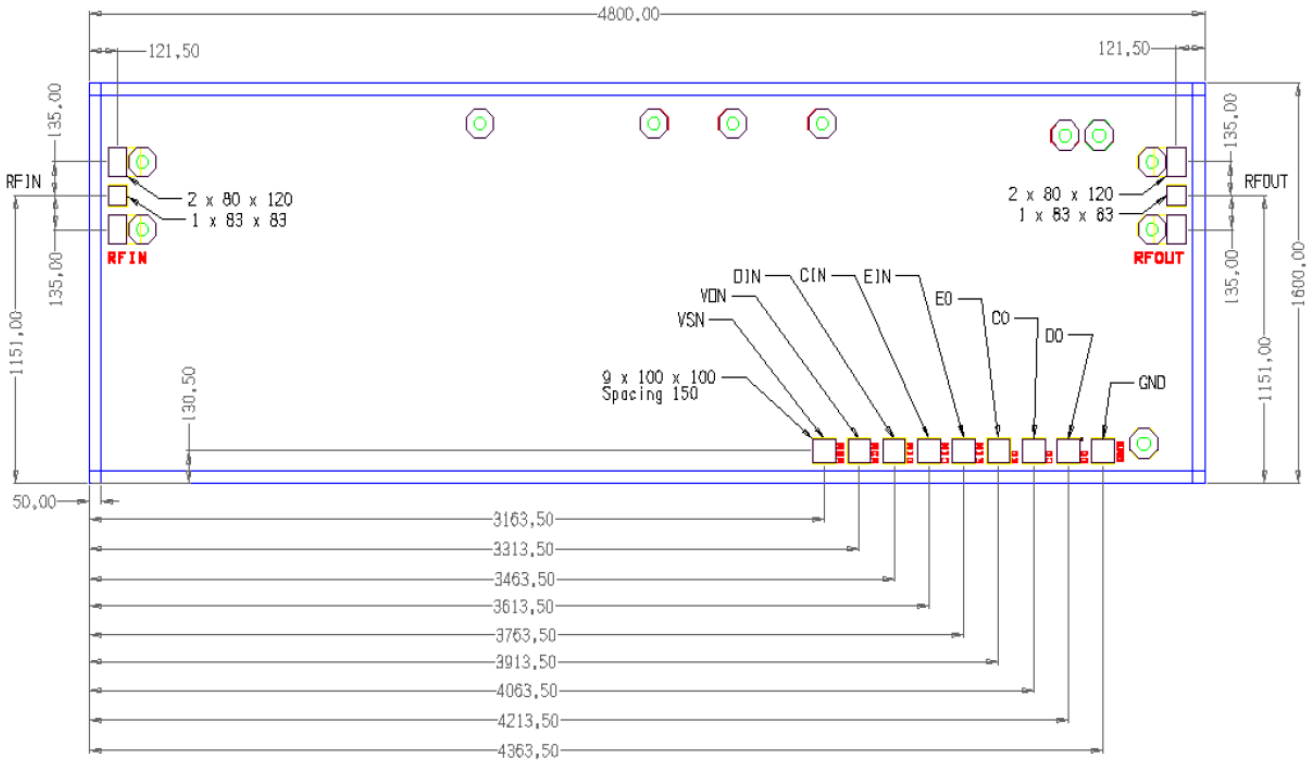
Bonding Diagram & Assembly Information



RF Bonding: 2 bonding's (wedge gold) with 25 µm in diameter and with a maximum length of 200 µm (150 µm recommended).

DC Bonding: 1 bonding with 25 µm in diameter can be used.

Mechanical Information (µm)



Chip Size = 4800 x 1600 µm (before wafer sawing)
DC Pads = 100 x 100 µm
Chip Thickness = 100 µm
Backside Metal = TiAu